THOMSON SEMICONDUCTORS

UAA4006A

SWITCH MODE POWER SUPPLY CONTROL CIRCUIT

The UAA4006A is a regulation and control device for fly-back switch mode power supplies using one external switching transistor.

- Includes oscillator, PWM and error amplifier
- Soft start
- Direct drive of the switching transistor
- Self-regulated positive base current (peak 1.5 A)
- Negative base current providing fast turn-off and allowing the best use of the safe operating area (peak 1.5 A)
- Switching transistor protected against saturation failure
- Instantaneous collector current limitation
- Positive power supply monitoring
- On chip thermal protection
- Adjustable minimum conducting time for use of a snubber circuit
- Internal reference voltage
- Start up with very low supply current

* Application note available AN027R1

ORDERING INFORMATION

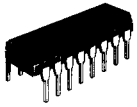
PART NUMBER	PACKAGE	
	DP	SP
UAA4006A	•	•

Example : UAA4006ADP

SWITCH MODE POWER SUPPLY CONTROL CIRCUIT

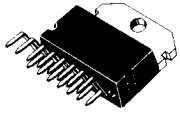
CASES

CB-79



DP SUFFIX
PLASTIC PACKAGE

CB-501



SP SUFFIX
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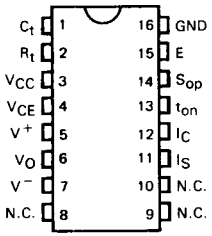
PIN ASSIGNMENTS

(Top view)

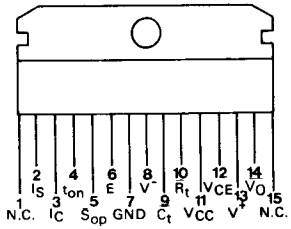
CB-79



C_t	: Oscillator timing capacitor
R_t	: Oscillator timing resistor
V_{CC}	: Supply voltage
V_{CE}	: $V_{CE(sat)}$ sensing
V^+	: Power stage positive supply
V_O	: Power stage output
V^-	: Power stage negative supply
I_S	: Secondary current monitoring input
I_C	: Primary current limit input
t_{on}	: $t_{on(max)}$ limit access
S_{op}	: Amplifier output
E	: Amplifier input
GND	: Ground

(Front view)

CB-501



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THOMSON COMPONENTS

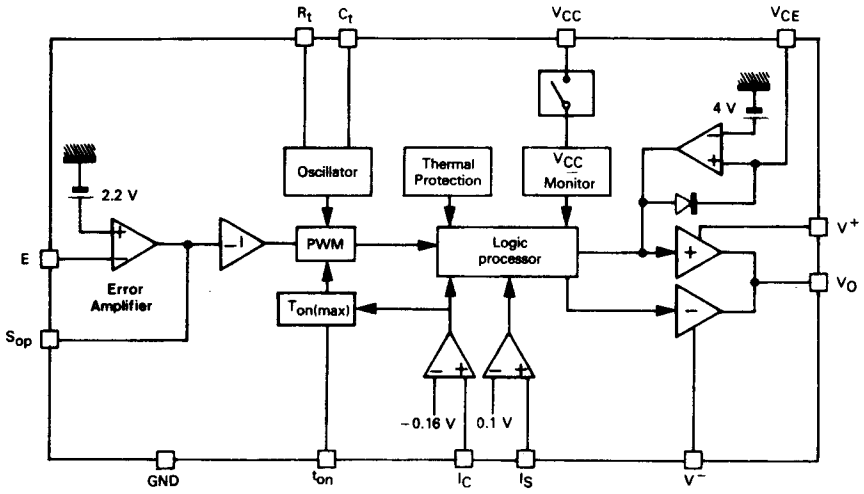
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	+15	V
Supply voltages (Power stage) Positive Negative	V^+ V^-	+15 −6	V V
Voltage between pins 11 and 13	$V^+ - V^-$	+18	V
Output current	I_O	±1.6	A
Current into input I_C (internal protection diodes)	–	±5	mA
Current into input I_S	–	±5	mA
Minimum value of resistance R_t	$R_{t(max)}$	18	kΩ
Junction temperature range	T_j	−40 to +150	°C
Storage temperature range	T_{stg}	−40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	CB-79	CB-501	Unit
Junction-ambient thermal resistance	$R_{th(j-a)}$	50	40	°C/W
Junction-case thermal resistance	$R_{th(j-c)}$	7	2.5	°C/W

BLOCK DIAGRAM



CASE	C_t	R_t	V_{CC}	V_{CE}	V^+	V_O	V^-	NC	I_S	I_C	t_{on}	S_{op}	E	GND
CB-79	1	2	3	4	5	6	7	8, 9, 10	11	12	13	14	15	16
CB-501	9	10	11	12	13	14	8	1, 15	2	3	4	5	6	7

CIRCUIT DESCRIPTION

OSCILLATOR

The oscillator provides a triangular waveform with a fall time much smaller than the rise time. The voltage swings between +1.5 V and about $V_{CC}/2$. The maximum operating frequency is 60 kHz, the period being given by $T_{osc} = 0.5 R_t C_t$ Resistor R_t adjusts the frequency, but determines also the value of $t_{on(min)}$ (see logic processor).

PULSE WIDTH MODULATOR (PWM)

The variable duty-cycle signal is elaborated by comparing the oscillator voltage (pin C_t) to the inverted error amplifier output voltage. Another comparator determines the maximum value of the duty-cycle by comparing the oscillator signal with the voltage on pin "t_{on}". If $V(t_{on}) = 0$, then the maximum duty-cycle is internally set to 0.9 T_{osc}, otherwise, the maximum duty-cycle is given by :

$$\left(\frac{t_{on}}{T_{osc}}\right)_{max} = 1 - \frac{R_{ton}}{2R_t}$$

(valid only if $R_{ton} > 0.2\ R_t$, where R_{ton} is the resistor inserted between t_{on} pin and ground).

CURRENT LIMITATION

A level lower than −0.15 V on pin I_C involves two actions :
- a direct action through the logic processor which stops the drive until the end of the oscillator period ;
- an indirect action through the t_{on} funtion. The change of state at the output of comparator I_C is applied to pin t_{on} as long as the overload current persists. By inserting capacitor C_B between pin t_{on} and V_{CC} (about 0.1 µF), the voltage at this point rises by a quantity ΔV proportional to the duration and the frequency of the overcurrent.

This will consequently lower the maximum conduction ratio, thus decreasing the frequency of the overcurrent. At the end of an overload condition, capacitor C_B slowly charges up through a 20k internal impedance, in order to return progressively to normal operation.

NOTE : If capacitor C_B is omitted, direct action will only be implemented.

SUPERVISION OF THE SECONDARY CURRENT

In order to avoid the magnetization of the transformer core in case of short-circuits or heavy overloads on the secondary winding, a new cycle of conduction can only begin after the secondary current has completly fallen to zero.
This task is accomplished by comparator I_S whose threshold is 0.1 V and detects the zero crossing of the secondary current.

PROTECTION AGAINST DESATURATION

If, because of a too low base current or a too heavy load, the collector to emitter voltage of the switching transistor rises above 4 V approximately, the output of comparator V_{CE} changes state, and the drive is interrupted.

ERROR AMPLIFIED

This is an operational amplifier whose open loop gain is about 1000. The input current are less than 3 µA, and the input offset voltage is lower than 5 mV.
The input common-mode voltage range is 0 V to (V_{CC} − 3 V). Due to an internal limitation the output source current of the amplifier can not exceed 2 mA.

START SWITCH

An internal switch is inserted between pin V_{CC} supply line and internal voltage.
During power-up, this switch closes when V_{CC} reaches +7.2 V. The leakage current (I_{CC})L is about 0.4 mA before the switch closes. This original feature enables starting the converter by means of a high value resistance directly connected between V_{CC} and the high supply voltage. The smoothing capacitor on V_{CC} supply provides the energy required for the start. The turn-off of the internal switch requires that V_{CC} falls below +6.2 V.

THERMAL PROTECTION

This protection becomes active when the junction temperature reaches +160°C.

LOGIC PROCESSOR

A logic unit processes the information coming from the fault detectors, and ensures that the output signal fulfils two conditions :

- No double pulsing with a period : the occurrence of a hault detection is memorized until the end of the period.
- To allow the discharge of a snubber network, the minimum width of the output pulse is set at a given value $t_{on(min)}$ by an internal monostable. If this monostable is not triggered, there will be no conduction. The duration $t_{on(min)}$ is programmable by resistor R_t using the relationship :

$$t_{on(min)}\ (\mu s) = 0.144\ R_t\ (k\Omega) - 2 \text{ @ } (V_{CC} = +12\ V)$$

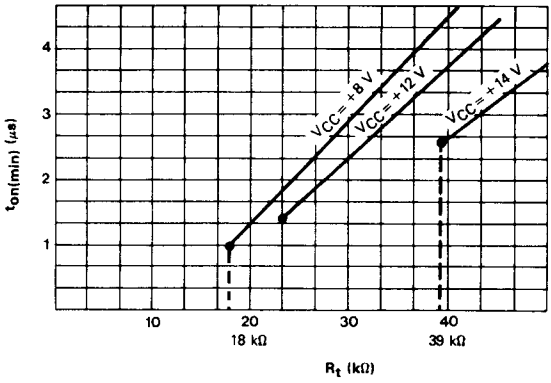
ELECTRICAL CHARACTERISTICS

$T_{amb} = +25°C$, $V_{CC} = \pm 10$ V, $V^- = -5$ V
(Unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	–	–	14	V
Rise supply voltage threshold	V_{CCR}	6.5	7.2	7.9	V
Fall supply voltage threshold	V_{CCF}	5.3	6.0	6.7	V
Hysteresis on V_{CC} threshold	ΔV_{CC}	1	1.2	1.7	V
Current I_{CC} (V_{CC} under threshold voltage)	–	–	0.4	1	mA
Supply current ($V_{CC} = +10$ V)	I_{CC}	–	10	–	mA
Positive supply voltage (Power stage)	V^+	4	–	15	V
Negative supply voltage (Power stage)	V^-	−6	–	−1	V
Threshold of input I_C	$I_{C(th)}$	−0.176	−0.16	−0.144	V
I_C input current ($V_{(I_C)} = 0$ V)	–	–	5	20	µA
Threshold of input I_S	$I_{S(th)}$	0.065	0.1	0.135	V
I_S input current ($V_{(I_S)} = 0$ V)	–	–	5	20	µA
Error amplifier open-loop gain	A_V	60	–	–	dB
Error amplifier offset voltage	V_{IO}	–	5	–	mV
Internal reference voltage	$V_{(ref)}$	2.1	2.2	2.3	V
Oscillator frequency $f_{osc} = \frac{1}{T_{osc}}$	f_{osc}	–	$2/R_tC_t$	60	kHz
Value of resistance R_t ($V_{CC} = +14$ V) (See figure 1) ($V_{CC} = +8$ V)	R_t	39 18	50 50	100 100	kΩ
Output current ($V^+ - V_S = 3$ V, $V_S - V^- = 3$ V)	I_O	±1.5	–	–	A
V_{CE} comparator threshold voltage	$V_{CE(th)}$	3.6	4	4.4	V
$t_{on(min)}$ adjustment range ($V_{CC} = +14$ V) (See figure 1) ($V_{CC} = +8$ V)	–	4 1	– –	8 13	µs
Max duty cycle : $\left(\frac{t_{on}}{T_{osc}}\right)_{max}$ ($R_{t_{on}} > 0.2\ R_t$) - Note 1 ($R_{t_{on}} < 0.2\ R_t$)	– –	– –	$1 - \frac{R_{t_{on}}}{2R_t}$ 0.9	– –	– –
Oscillator frequency drift with temperature ($V_{CC} = 12$ V)	–	–	0.02	0.05	%/°C
Oscillator frequency drift with V_{CC}	–	–	0.2	0.5	%/V

Note 1 : $R_{t_{on}}$ externally connected between pin "t_{on}" and GND
R_t externally connected between pin "R_t" and GND

FIGURE 1 - $t_{on(min)}$ ADJUSTMENT RANGE



OUTPUT STAGE

ON-state

The positive stage achieves a very efficient drive of the switching transistor.
Its features are essentially :

- Direct drive (neither inductor, nor tranformer) ;
- The transistor stays in a quasi-saturation mode, and thus has a reduced storage time ;
- The drive energy is strictly limited to the required amount ;
- Easy implementation.

K_1 is closed to turn the positive stage on. The maximum value of the positive base current is determined by the external limitation resistor R (between V_{CC} and V^+).
Diode D maintains Q in a quasi-saturation mode : the more Q is saturated, the more diode D will shunt an important part of the drive current I_{B1}, through diode D_1.
Resistor R_B has a low value (about 1 Ω), and is used to stabilize the regulation loop. For a good efficiency of the negative drive, the value of this resistor should be as low as possible.
Integrated Darlington T_1 is able to supply a peak current of 1.5 A with a 2 V saturation voltage.
The voltage V_{CE} on transistor Q is :
$V_{CE} = V_D + R_B I_{B1}$

OFF-state

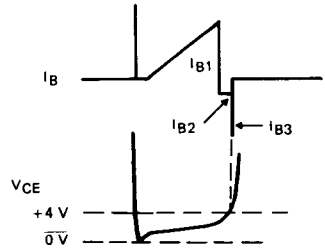
The turn off is accomplished in two steps :

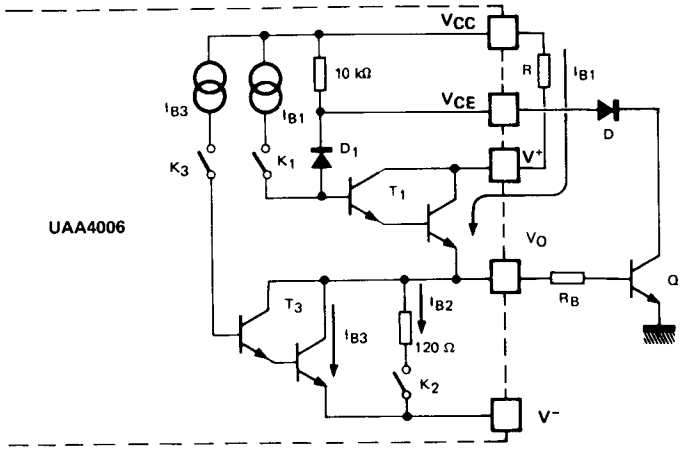
- an immediate action through K_2 which connects the base of the switching transistor to the negative supply through a 120 Ω integrated resistor (current I_{B2}) :
- a detayed action through K_3 which is closed only after the desaturation of the external transistor. This is detected by comparator V_{CE}, when the collector to emitter voltage reaches 4.5 V.

Darlington T_3 can supply 1.5 A with a 2 V saturation voltage (current I_{B3}).

NOTE : The negative drive I_{B3} for the removal of the stored charges is delayed in order to limit the slope dI_B/dt at the on-off transition. A high dI_B/dt might indeed lead to a destructive overheating of the base-collector junction (see "The power transistor in its environment" published by Thomson-CSF Division Semiconducteurs Discrets).

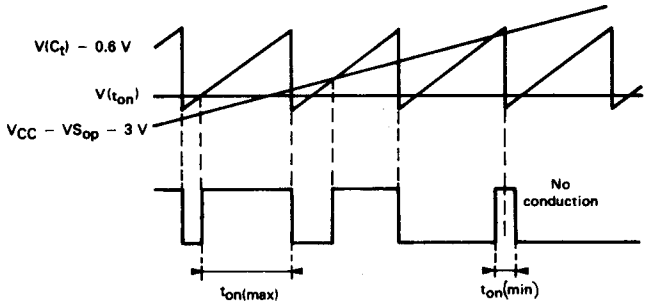
SELF REGULATED BASE CURRENT $I_B = f(V_{CE})$



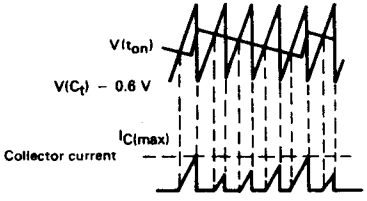


TYPICAL WAVEFORMS

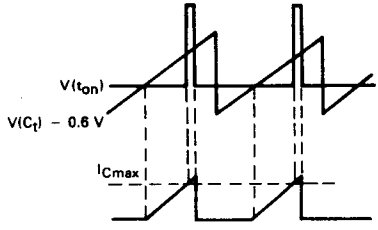
LIMITS OF THE DUTY CYCLE



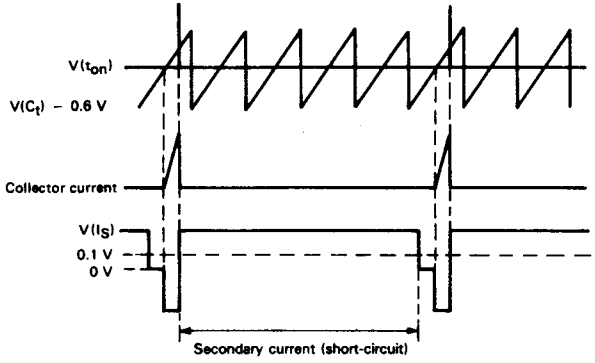
CURRENT LIMITATION



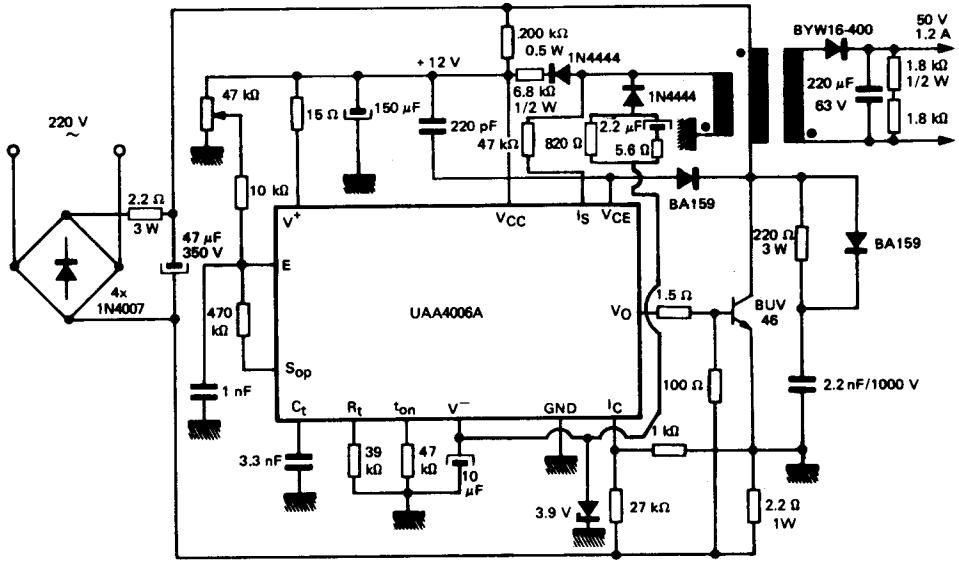
WITH C_B CAPACITOR



WITHOUT C_B CAPACITOR

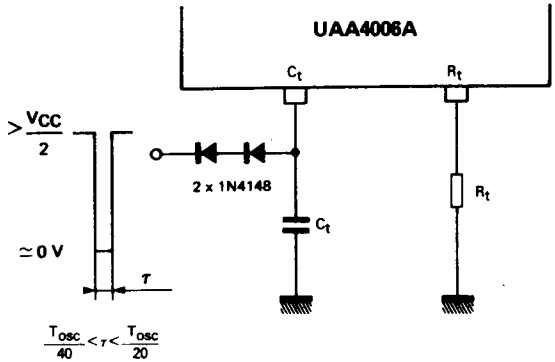


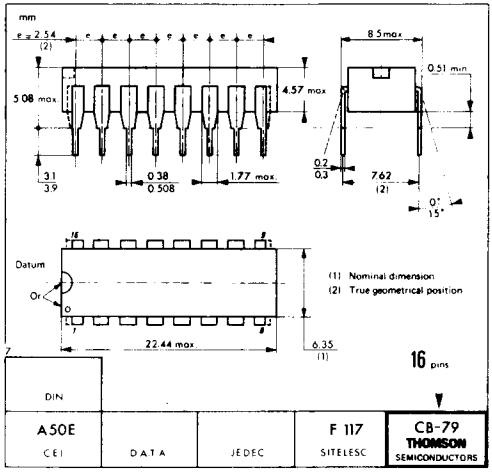
50 W FLY-BACK CONVERTER



EXTERNAL SYNCHRONIZATION

The oscillator may be synchronized to an external frequency f_{ext} so that : $f_{osc} < f_{ext} < 1.2\ f_{osc}$





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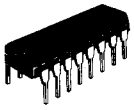
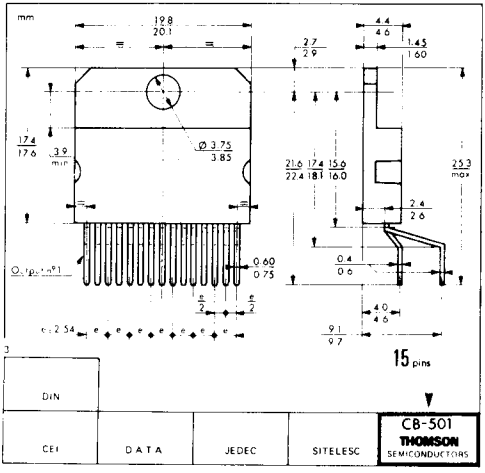


DP SUFFIX
PLASTIC PACKAGE



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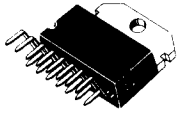

SP SUFFIX
PLASTIC PACKAGE

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Please inquire with our sales offices about the availability of the different packages.