

M5L 2111A P, S; P-2, S-2; P-4, S-4**1024-BIT (256-WORD BY 4-BIT) STATIC RAM****DESCRIPTION**

This is a family of 256-word by 4-bit static RAMs, fabricated with the N-channel silicon-gate MOS process and designed for simple interfacing. These devices operate on a single 5V supply, as does TTL, and are directly TTL-compatible.

The input and output terminals are common, and an OD terminal is provided.

FEATURES

Parameter	M5L 2111AP,S-2	M5L 2111AP,S	M5L 2111AP,S-4
Access time (max)	250ns	350ns	450ns
Cycle time (min)	250ns	350ns	450ns

- Low power dissipation: 150 μ W/bit (typ)
- Single 5V power supply
- Data holding at 1.5V supply voltage (optional)
- No clocks or refreshing required
- All inputs and outputs are directly TTL-compatible
- All outputs are three-state, with OR-tie capability
- Simple memory expansion by chip select input
- Common data inputs and outputs
- Interchangeable with Intel's 2111A series in pin configuration and electrical characteristics

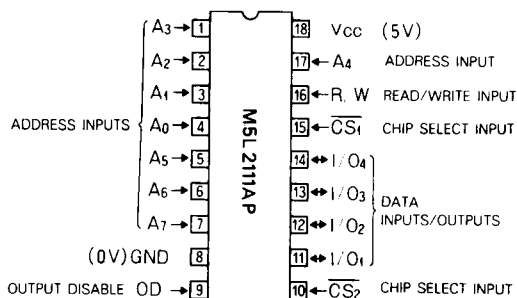
APPLICATION

- Small-capacity memory units

FUNCTION

These devices provide common data input and output terminals. During a write cycle, when a location is designated by address signals $A_0 \sim A_7$, the OD signal is kept high to keep the I/O terminals in the input mode, signal R/W goes low, and the data of the IN signal at that time is written.

During a read cycle, when a location is designated by address signals $A_0 \sim A_7$, the OD signal is kept low to keep

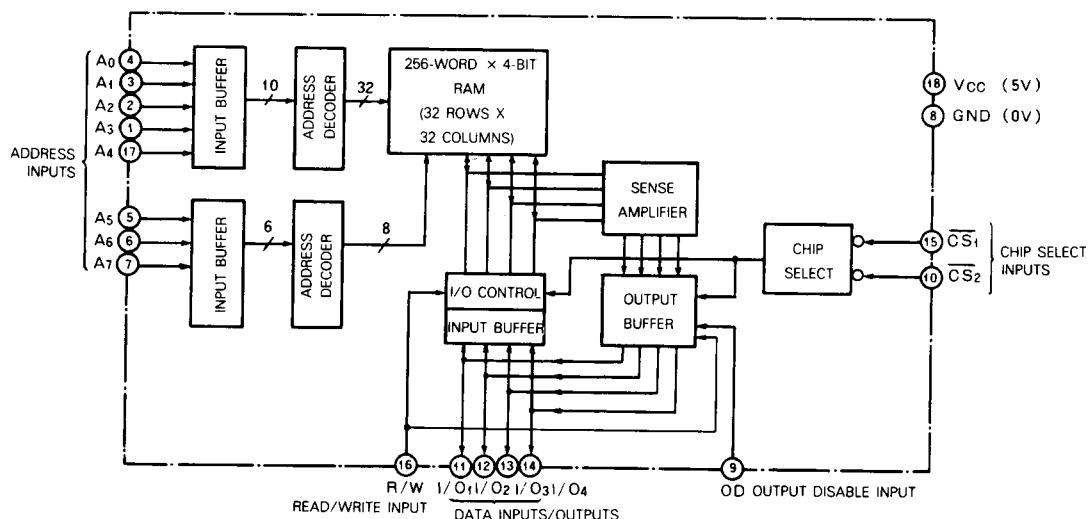
PIN CONFIGURATION (TOP VIEW)

**Outline 18P1 (M5L 2111A P)
18S1 (M5L 2111A S)**

the I/O terminals in the output mode, signal R/W goes high, and the data of the designated address is available at the I/O terminals.

When signal $\overline{CS}_1$ or $\overline{CS}_2$ is high, the chip is in the non-selectable state, disabling both reading and writing. In this case the output is in the floating (high-impedance) state, useful for OR-ties with other output terminals.

The memory data can be held at a supply voltage of 1.5V, enabling battery back-up operation during power failure and power-down operation in the standby mode.

BLOCK DIAGRAM

M5L 2111A P, S; P-2, S-2; P-4, S-4

1024-BIT (256-WORD BY 4-BIT) STATIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V _{CC}	Supply voltage	With respect to GND	-0.3 ~ 7	V
V _I	Input voltage		-0.3 ~ 7	V
V _O	Output voltage		-0.3 ~ 7	V
P _d	Maximum power dissipation	M5L 2111A P	700	mW
		M5L 2111A S	1000	mW
T _{opr}	Operating free-air ambient temperature, range	T _a = 25°C	0 ~ 70	°C
T _{stg}	Storage temperature range	M5L 2111A P	-40 ~ 125	°C
		M5L 2111A S	-65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = 0 ~ 10°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V _{CC}	Supply voltage	4.75	5	5.25	V
V _{IL}	Low-level input voltage	0		0.8	V
V _{IH}	High-level input voltage	2.2		V _{CC}	V

ELECTRICAL CHARACTERISTICS (T_a = 0 ~ 70°C, V_{CC} = 5V ± 5%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V _{IH}	High-level input voltage		2.2		V _{CC}	V
V _{IL}	Low-level input voltage		0		0.8	V
V _{OH}	High-level output voltage	I _{OH} = -200 μA	2.4			V
V _{OL}	Low-level output voltage	I _{OL} = 3.5 mA			0.45	V
I _I	Input current	V _I = 0 ~ 5.25 V			10	μA
I _{OZH}	Off-state high-level output current	V _I (CS ₁) = 2.2 V, V _O = 2.4 V ~ V _{CC}			10	μA
I _{OZL}	Off-state low-level output current	V _I (CS ₁) = 2.2 V, V _O = 0.4 V			-10	μA
I _{CC}	Supply current from V _{CC}	V _I = 5.25 V (all inputs), output open, T _a = 25°C		30	60	mA
C _I	Input capacitance, all inputs	V _I = GND, f = 1 MHz, 25 mVrms		3	5	pF
C _O	Output capacitance	V _O = GND, f = 1 MHz, 25 mVrms		8	12	pF

Note 1: Current flowing into an IC is positive; out is negative.

SWITCHING CHARACTERISTICS (For Read Cycle) (T_a = 0 ~ 70°C, V_{CC} = 5V ± 5%, unless otherwise noted) (Note 2)

Symbol	Parameter	M5L 2111A P,S-2			M5L 2111A P,S			M5L 2111A P,S-4			Unit
		Limits			Limits			Limits			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t _{C(AD)}	Read cycle time	250			350			450			ns
t _{a(AD)}	Address access time			250			350			450	ns
t _{a(CS)}	Chip select access time			180			180			180	ns
t _{a(OD)}	Output disable access time			130			150			150	ns
t _{PXZ}	Output disable time (Note 3)			100			100			100	ns
t _{DV(AD)}	Data valid time with respect to address	40			40			40			ns

Note 2: Test conditions: Input pulse V_{IH} = 2.2 V, V_{IL} = 0.8 V, t_r = t_f = 20 ns, reference level = 1.5 V, load = 2TTL, C_L = 100 pF.

Note 3: t_{PXZ} is with respect to CS₁, CS₂, or OD, whichever occurs first.

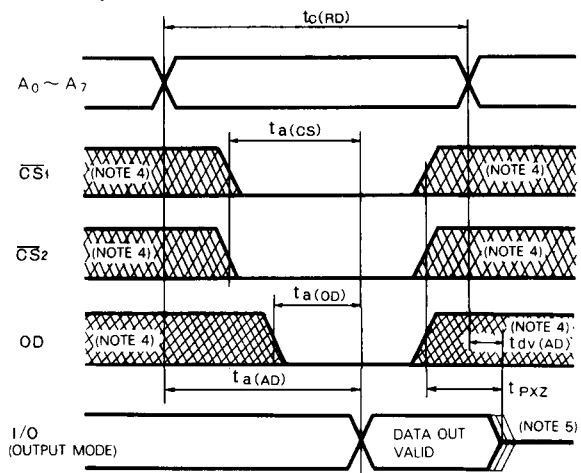
TIMING REQUIREMENTS (For Write Cycle) (T_a = 0 ~ 70°C, V_{CC} = 5V ± 5%, unless otherwise noted) (Note 2)

Symbol	Parameter	M5L 2111A P, S-2			M5L 2111A P, S			M5L 2111A P, S-4			Unit
		Limits			Limits			Limits			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t _C (WR)	Write cycle time	170			220			270			ns
t _w (WR)	Write pulse width	150			200			250			ns
t _{SU} (AD)	Address setup time with respect to write	20			20			20			ns
t _{wr}	Write recovery time	0			0			0			ns
t _{SU} (OD)	Output disable setup time with respect to data in	20			20			20			ns
t _{SU} (DA)	Data setup time	100			150			170			ns
t _H (DA)	Data hold time	0			0			0			ns
t _{SU} (CS)	Chip select setup time	150			200			250			ns

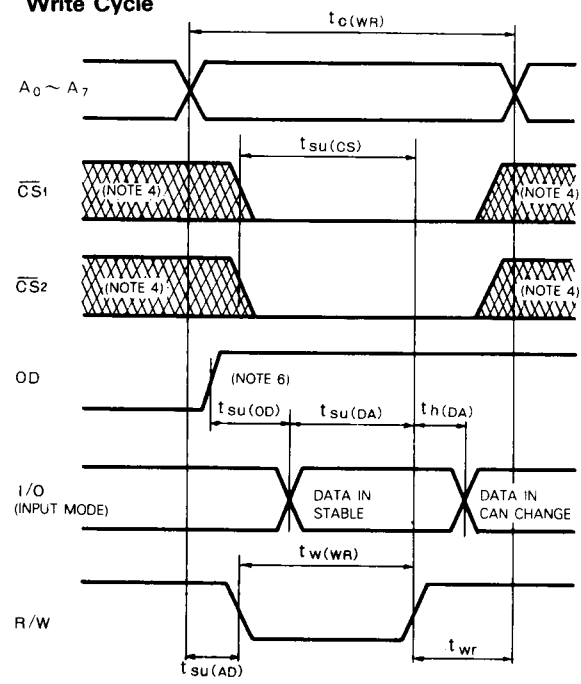
M5L 2111A P, S; P-2, S-2; P-4, S-4

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TIMING DIAGRAM Read Cycle



Write Cycle



Note 4: Hatching indicates the state is unknown

5: Indicates that during this period the data out is invalid for this definition of $t_{dv}(AD)$ and is in the floating state for this definition of t_{PxZ} .

6: The input signals from the external circuits should not be applied to the I/O terminals, for during this period they are in output mode.

POWER-DOWN OPERATION (OPTIONAL) These characteristics are guaranteed only under custom specifications.

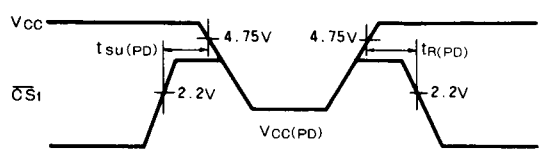
Electrical Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{CC(PD)}$	Power-down supply voltage		1.5			V
$V_I(\overline{CS}1)$	Power-down chip select input voltage	$2.2\text{V} \leq V_{CC(PD)} \leq V_{CC}$	2.2			V
		$1.5\text{V} \leq V_{CC(PD)} \leq 2.2\text{V}$	$V_{CC(PD)}$			V
$I_{CC(PD1)}$	Power-down supply current from V_{CC}	$V_{CC} = 1.5\text{V}$, all inputs = 1.5V		15	30	mA
$I_{CC(PD2)}$	Power-down supply current from V_{CC}	$V_{CC} = 2.0\text{V}$, all inputs = 2.0V		20	40	mA

Timing Requirements ($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power-down setup time		0			ns
$t_{R(PD)}$	Power-down recovery time		$t_c(RD)$			ns

Timing Diagram



MITSUBISHI LSI's
M5L 2111A P, S; P-2, S-2; P-4, S-4

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TYPICAL CHARACTERISTICS

