

MN3101

Clock Generator / Driver MN 3101 for BBD's

General Description

The MN3101 is a CMOS integrated circuit designed to generate low impedance two clock phases required for driving BBD's. In addition, the MN3101 provides the optimum V_{GG} for BBD's* when the MN3101 is used with BBD's on a common V_{DD} supply. The self-contained oscillator can be controlled by an external RC circuit, but an external oscillator can also be used. The clock frequency is 1/2 of the oscillation frequency.

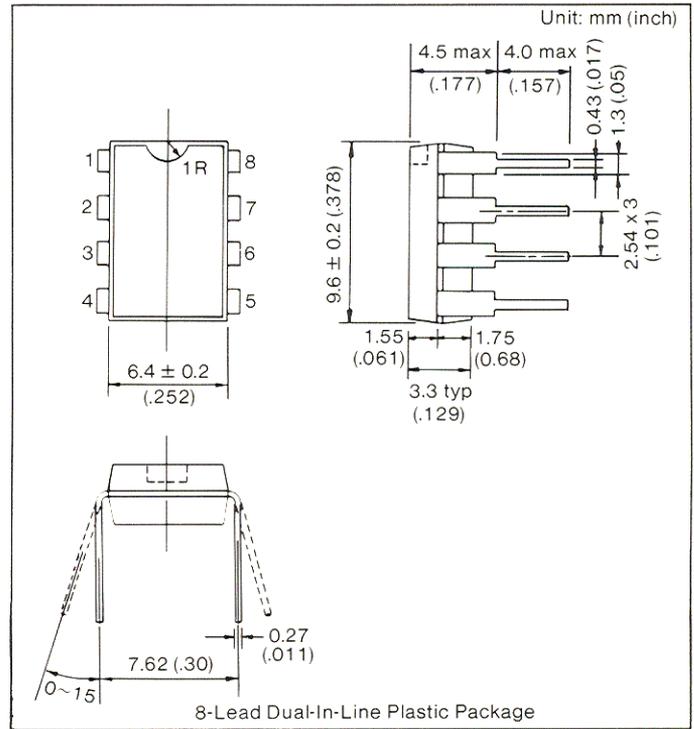
*PANASONIC's BBD product range: MN3001, MN3002, MN3003, MN3004, MN3005, MN3006, MN3007, MN3008, MN3009, MN3010, MN3011, MN3012. Note: The MN3003 is provided with an internal oscillator.

Features:

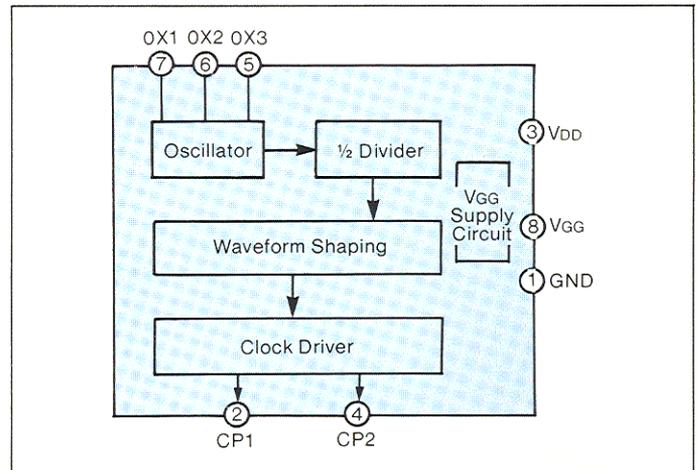
- BBD direct driving capability – up to two MN3005 types (equivalent to 8192 stages).
- Either internal or external oscillator can be used
- Two phases (1/2 duty) output
- Provided with V_{GG} supply circuit
- Operates on a single power supply: $-8 \sim -16V$
- 8-lead dual-in-line plastic package

Application

- BBD clock generator/driver



Block Diagram



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Supply Voltage	V _{DD}	-18~+0.3 *	V
Input Terminal Voltage	V _I	V _{DD} -0.3~+0.3 *	v
Output Terminal Voltage	V _O	V _{DD} -0.3~+0.3 *	V
Power Dissipation	P _D	200	mW
Operating Temperature	T _{opr}	-10~+70	°C
Storage Temperature	T _{stg}	-30~+125	°C

*With respect to GND = OV.

Operating Conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	V _{DD}	GND = OV	-8	-15	-16	V

Electrical Characteristics (Ta = 25°C, V_{DD} = -15V, GND = OV)

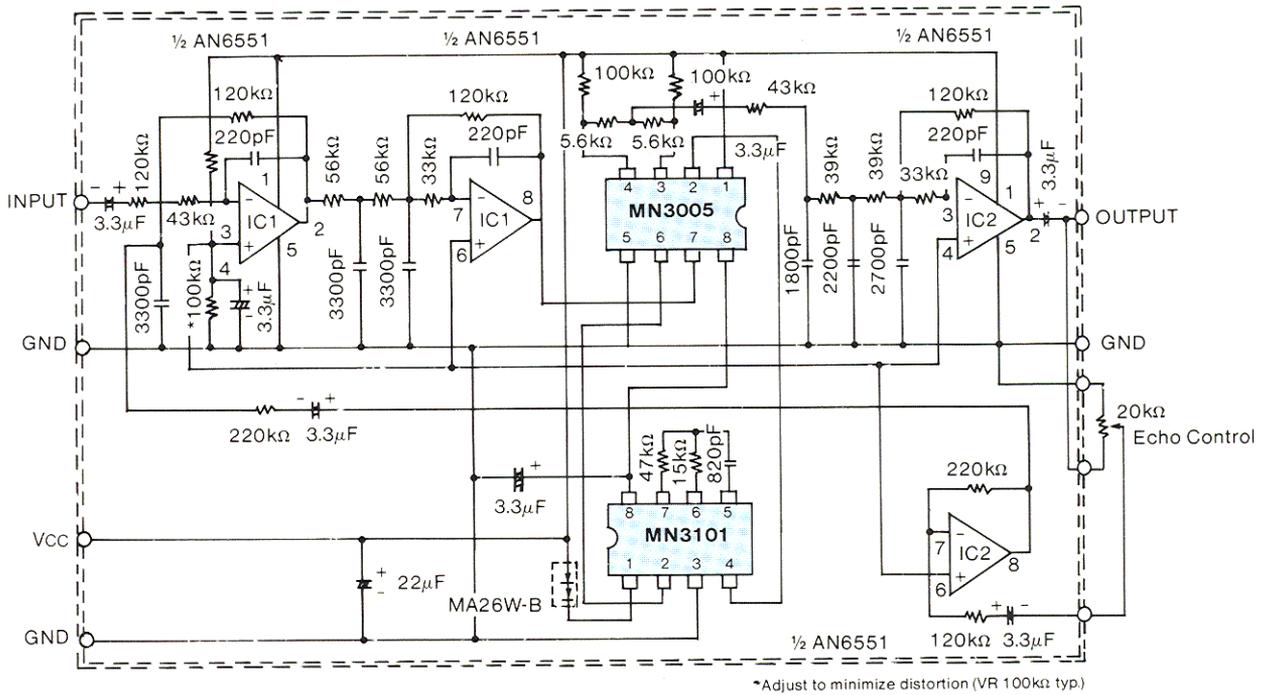
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Current	I _{DD}	Without load		3		mA
Power Consumption	P _{tot}	Clock output 40kHz		45		mW
OX1 Input Terminal						
Input Voltage "H" Level	V _{IH}		0		-1	V
Input Voltage "L" Level	V _{IL}		V _{DD} +1		V _{DD}	V
Input Leakage Current	I _{LK}	V _I = 0~-15V			30	μA
OX2 Output Terminal						
Output Current "H" Level	I _{OH1}	V _O = -1.0V	0.6			mA
Output Current "L" Level	I _{OL1}	V _O = -14V	0.5			mA
Output Leakage Current	I _{LOL1}	V _O = V _{DD}			30	μA
Output Leakage Current	I _{LOH1}	V _O = GND			30	μA
OX3 Output Terminal						
Output Current "H" Level	I _{OH2}	V _O = -1.0V	1.5			mA
Output Current "L" Level	I _{OL2}	V _O = -14V	2.0			mA
Output Leakage Current	I _{LOL2}	V _O = V _{DD}			30	μA
Output Leakage Current	I _{LOH2}	V _O = GND			30	μA
CP1, CP2 Output Terminal						
Output Current "H" Level	I _{OH3}	V _O = -1.0V	10			mA
Output Current "L" Level	I _{OL3}	V _O = -14V	10			mA
Output Leakage Current	I _{LOL3}	V _O = V _{DD}			30	μA
Output Leakage Current	I _{LOH3}	V _O = GND			30	μA
VGG Output Terminal*						
Output Voltage	V _{GG OUT}			-14.0		V

*This terminal outputs VGG voltage particularly suitable for the BBD's manufactured by PANASONIC. The voltage is not necessarily suitable for the manufacturer's products.

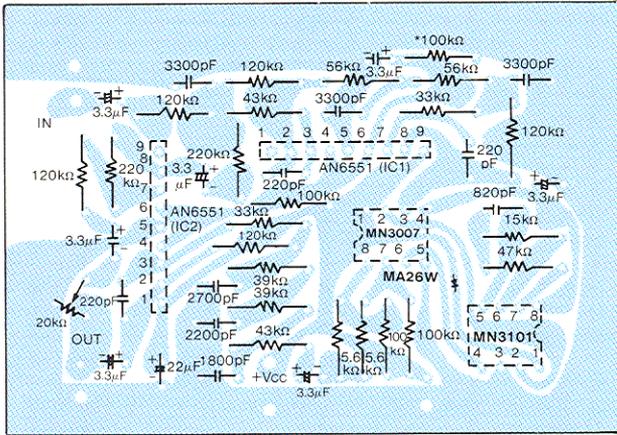
The V_{GG OUT} changes depending on V_{DD}. The relationship between V_{GG OUT} and V_{DD} is as follows:

V_{GG OUT} = 14/15 V_{DD}

Application Circuit Example 1 – Echo Effect Generation Circuit With The MN3005



Printed Circuit Board Layout (Actual Size)



Quick Reference Data for The MN3005

Item	Symbol	Value	Unit
Supply Voltage	VDD, VGG	-15, VDD + 1	V
Signal Delay Time	tD	20.48 ~ 204.8	msec.
Total Harmonic Distortion	THD	1	%
Signal to Noise Ratio	S/N	75	dB

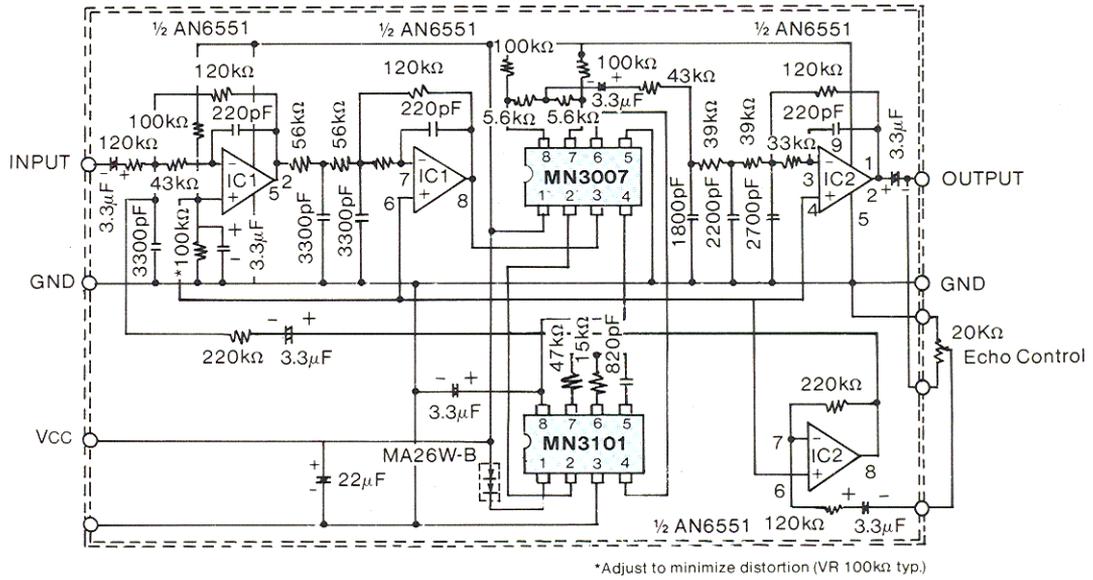
Quick Reference Data for the AN6551

Item	Symbol	Value	Unit
Supply Voltage	VCC	15	V
	VEE	-15	V
Input Bias Current	IB	500max.	nA
Voltage Gain	Gv	100typ.	dB
Noise Voltage Referred to Input	Vni	2.5typ.	µVrms
Maximum Output Voltage	Vo(max.)	±13typ.	V
Common-Mode Rejection Ratio	CMR	90typ.	dB
Supply Voltage Rejection	SVR	30typ.	µV/V

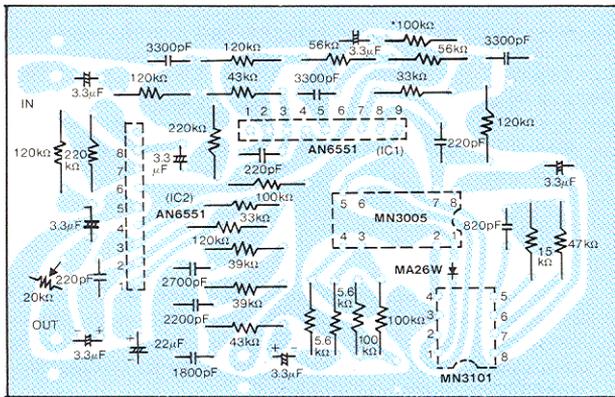
Electrical Characteristics of The Application Circuit Using The MN3005 (VCC = 9V, Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Current	ICC			8	10	mA
Total Power Consumption	Ptot			70		mW
Signal Delay Time	tD	fcp = 18 ± 2kHz	100	113	128	msec
Cutoff Frequency	fco			2		kHz
Input Signal Swing	Vi	THD = 2.5%			500	mVrms
Insertion Loss	Li	fi = 1kHz, Vi = 300mV	-2	0	2	dB
Total Harmonic Distortion	THD	Fi = 1kHz, Vi = Vi(max.) -6dB		0.5	1	%
Output Noise Voltage	Vno	Vi = 0V			0.35	mVrms
Signal to Noise Ratio	S/N	Vs Vi(max.) = 500mVrms	60			dB

Application Circuit Example 2 – Echo Effect Generation Circuit With The MN3007



Printed Circuit Board Layout (Actual Size)



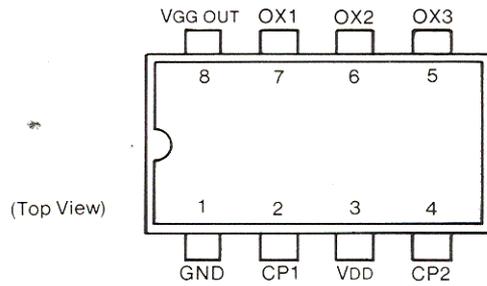
Quick Reference Data for The MN3007

Item	Symbol	Value	Unit
Supply Voltage	VDD, VGG	-15, V _{DD} +1	V
Signal Delay Time	t _D	5.12 ~ 51.2	msec.
Total Harmonic Distortion	THD	0.3	%
Signal to Noise Ratio	S/N	88	dB

Electrical Characteristics of The Application Circuit Using The MN3007 (V_{CC} = 9V, T_a = 25°C)

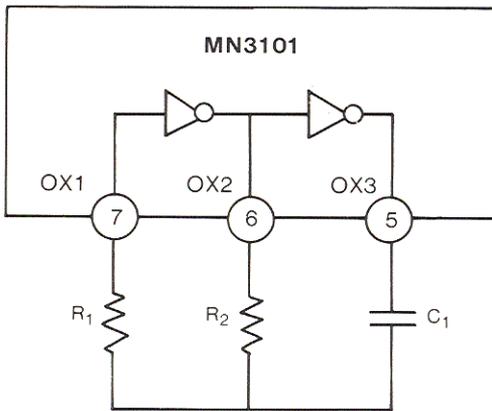
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Current	I _{CC}			8	10	mA
Total Power Consumption	P _{tot}			70		mW
Signal Delay Time	t _D	f _{cp} = 14 ± 2kHz	32	37	43	msec
Cutoff Frequency	f _{co}			2		kHz
Input Signal Swing	V _i	THD = 2.5%			500	mVrms
Insertion Loss	L _i	f _i = 1kHz, V _i = 300mV	-2	0	2	dB
Total Harmonic Distortion	THD	f _i = 1kHz, V _i = V _{i(max)} -6dB		0.5	1	%
Output Noise Voltage	V _{no}	V _i = OV			0.35	mVrms
Signal to Noise Ratio	S/N	V _s V _{i(max)} = 500mVrms	60			dB

Terminal Assignments



Pin No.	Symbol	I/C	Functions	
1	GND	Supply	Grounding	
2	CP1	O	Outputs 1/2 duty cycle clock pulse at frequency 1/2 of an oscillation frequency, having an opposite phase relationship with respect to CP2.	
3	V _{DD}	Supply	-15V supply voltage input.	
4	CP2	O	Outputs clock pulse having an opposite phase relationship with respect to CP1.	
5	OX3	O	Internal Oscillation: C R network connection to the pins (See oscillator circuit example)	External Oscillation: An external oscillation input to OX1. with OX2 and OX3 open.
6	OX2	O		
7	OX1	I		
8	V _{GG} OUT	O	-14V output (When V _{DD} = 15V) The relationship between V _{DD} and V _{GG} OUT is: $V_{GG\ OUT} = 14/15 V_{DD}$	

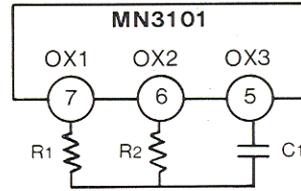
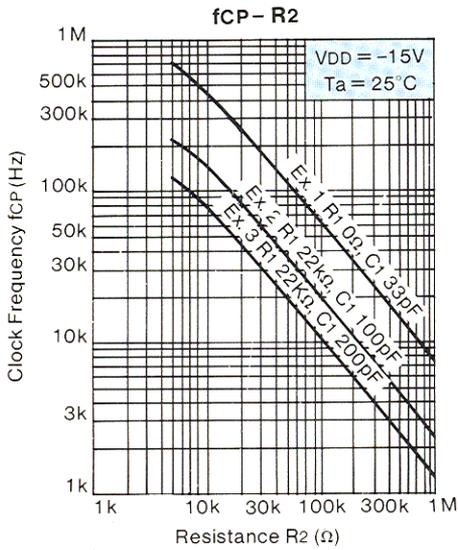
Oscillator Circuit Example



The internal oscillation circuit of the MN3101 consists of a 2-stage inverter. The oscillation frequency is established by the time constant of C₁ and R₂. The following table shows examples of C₁, R₁ and R₂ values. F_{CP} - R₂ characteristics example is shown in Figure 1.

Example \ Constant	R ₁ (Ω)	R ₂ (Ω)	C ₁ (pF)	f _{osc} ** (kHz)	F _{CP} * (kHz)
Example 1	0	5k~1M	33	15~1500	7.5~750
Example 2	22k	5k~1M	100	5.2~440	2.6~220
Example 3	22k	5k~1M	200	1.4~280	0.7~140

*Clock output frequency for CP1 or CP2.
 **Oscillation frequency for OX1, OX2, and OX3.



Maximum Clock Frequency

The maximum clock frequency is limited by device power dissipation and load capacitance. The power consumption of the devices increases as the clock frequency or load capacitance is increased (See Fig. 2). Therefore, a proper clock frequency and load capacitance value must be chosen so that the maximum allowable power dissipation of 200mW for the MN3101 is not exceeded.

Fig. 3 shows the relationship between the maximum frequency and load capacitance for 150mW power dissipation. The maximum clock frequency can be increased without increasing the power consumption when a resistor is connected to each clock output terminal (See Fig. 2 and 3). The series resistor consumes a part of the power required for driving the load capacitance and help reduce the power dissipated in the device.

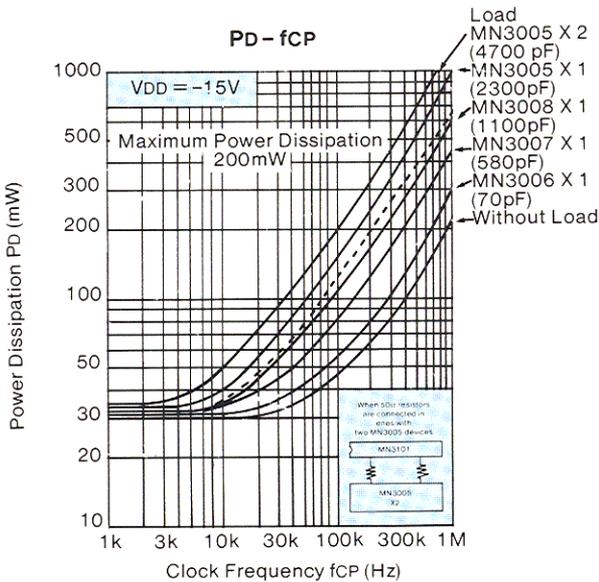


Fig. 2 Power Consumption vs Clock Frequency

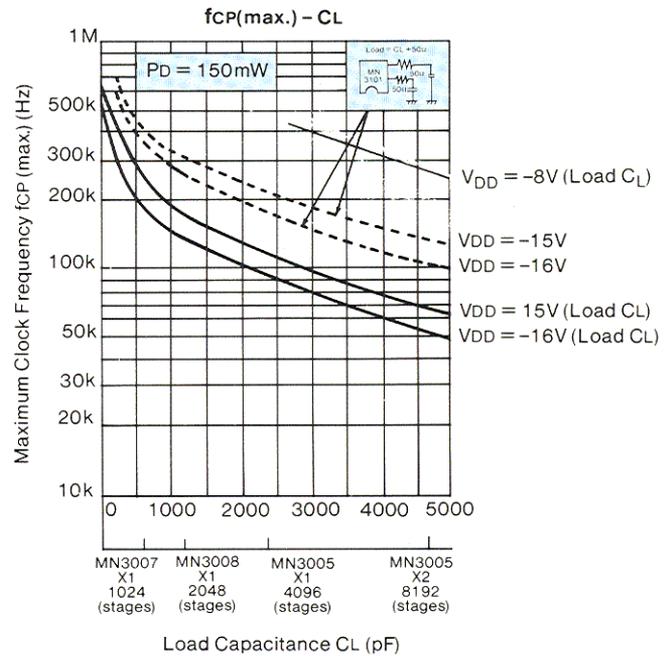


Fig. 3 Maximum Clock Frequency vs Load Capacitance at 150mW Power Consumption