1024 WORD x 4 BIT STATIC RAM

# TMM2114AP-12
# TMM2114AP-15

## DESCRIPTION

The TMM2114AP is a 4,096 bits static random access memory organized as 1024 words by 4 bits and operates from a single 5V power supply. Toshiba's high performance device technology provides both high speed and low power features with maximum operating current of 60mA and maximum access time of 120ns/150ns. The memories with 6Tr. cells are fully static in operation and require no clocks or refresh periods. Therefore the TMM2114AP is most suitable for use in microcomputer peripheral memory where high performance, lower cost, simple interfacing are required.

The TMM2114AP is fabricated with N channel silicon gate depletion load type MOS technology by ion implantation for high speed, high performance and high reliability.

The chip is moulded in the standard 18 pin plastic package with 0.3 inch width.

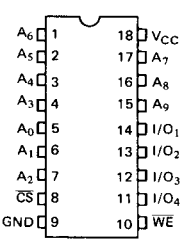
## FEATURES

- 1024 Word x 4 Bit organization
- Fully static operation
- Single 5V supply voltage
- All inputs and outputs: Directly TTL compatible
- Three state output: Wired OR capability
- Common data inputs and outputs
- 2114A type pin compatible
- Fast Access time and Low Operating Current (Max.)

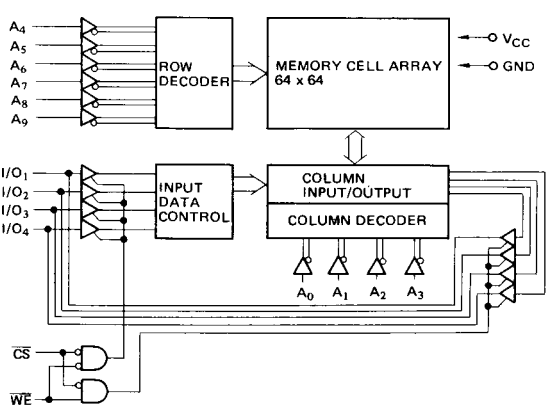
| | TMM2114AP-12 | TMM2114AP-15 |
|---|---|---|
| $t_{ACC(ns)}$ | 120 | 150 |
| $I_{CC(mA)}$ | 60 | 60 |

- Input protected: All inputs have protection against static charge.

## PIN CONNECTION (TOP VIEW)




## BLOCK DIAGRAM




## PIN NAMES

| | |
|---|---|
| $A_0 \sim A_3$ | Column Address Inputs |
| $A_4 \sim A_9$ | Row Address Inputs |
| $I/O_1 \sim I/O_4$ | Data Input/Output |
| $\overline{CS}$ | Chip Select Input |
| $\overline{WE}$ | Write Enable Input |
| $V_{CC}$ | Supply Voltage |
| GND | Ground |

## TRUTH TABLE

| $\overline{CS}$ | $\overline{WE}$ | $D_{IN}$ | $D_{OUT}$ | MODE |
|---|---|---|---|---|
| H | * | * | High Impedance | Non-decode |
| L | H | * | Data Output | Read |
| L | L | H/L | Data Input | Write |

* L or H

## MAXIMUM RATINGS

| SYMBOL | ITEM | RATING | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply Voltage | −0.5 ~ 7.0 | V |
| $V_{I/O}$ | Input/Output Voltage | −0.5 ~ 7.0 | V |
| $T_{OPR}$ | Operating Temperature | 0 ~ 70 | °C |
| $T_{STG}$ | Storage Temperature | −55 ~ 150 | °C |
| $T_{SOLDER}$ | Soldering Temperature · Time | 260 · 10 | °C · sec |
| $P_D$ | Power Dissipation (Ta = 70°C) | 850 | mW |

## DC RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | 2.0 | – | $V_{CC}$+1.0 | V |
| $V_{IL}$ | Input Low Voltage | −0.5 | – | 0.8 | V |
| $V_{CC}$ | Supply Voltage | 4.5 | 5 | 5.5 | V |

## DC CHARACTERISTICS (Ta = 0 ~ 70°C)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP.* | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_{IL}$ | Input Leakage Current | $V_{IN}$ = 0V ~ 5.5V | −10 | – | 10 | μA |
| $V_{OH}$ | Output High Voltage | $I_{SOURCE}$ = −1.0mA | 2.4 | – | – | V |
| $V_{OL}$ | Output Low Voltage | $I_{SINK}$ = 2.1mA | – | – | 0.4 | V |
| $I_{LO}$ | Output Leakage Current | $\overline{CS}$ = $V_{IH}$ or $\overline{WE}$ = $V_{IL}$<br>$V_{OUT}$ = 0.0V ~ 5.5V | −10 | – | 10 | μA |
| $I_{CC}$ | Supply Current | $I_{OUT}$ = 0mA | – | – | 60 | mA |

* Ta = 25°C, $V_{CC}$ = 5V

## AC CHARACTERISTICS (Ta = 0 ~ 70°C, $V_{CC}$ = 5V ± 10%, 1-TTL Gate & $C_L$ = 100pF, $t_r$, $t_f$ ≦ 10 ns)

### READ CYCLE

| SYMBOL | PARAMETER | TMM2114AP-12 | | | TMM2114AP-15 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN. | TYP.* | MAX. | MIN. | TYP.* | MAX. | |
| $t_{RC}$ | Read Cycle Time | 120 | – | – | 150 | – | – | ns |
| $t_{ACC}$ | Access Time | – | – | 120 | – | – | 150 | ns |
| $t_{CO}$ | Chip Select Time | – | – | 70 | – | – | 70 | ns |
| $t_{CX}$ | Output Active from $\overline{CS}$ | 10 | – | – | 10 | – | – | ns |
| $t_{OD}$ | Deselect Time | 0 | – | 35 | 0 | – | 40 | ns |
| $t_{OH}$ | Output Hold From Address Change | 20 | – | – | 20 | – | – | ns |

* Ta = 25°C, $V_{CC}$ = 5V

### WRITE CYCLE

| SYMBOL | PARAMETER | TMM2114AP-12 | | | TMM2114AP-15 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN. | TYP.* | MAX. | MIN. | TYP.* | MAX. | |
| $t_{WC}$ | Write Cycle Time | 120 | – | – | 150 | – | – | ns |
| $t_{WP}$ | Write Pulse Width | 70 | – | – | 90 | – | – | ns |
| $t_{WR}$ | Write Recovery Time | 0 | – | – | 0 | – | – | ns |
| $t_{ODW}$ | Output High Z From $\overline{WE}$ | 0 | – | 35 | 0 | – | 40 | ns |
| $t_{DS}$ | Data Setup Time | 70 | – | – | 90 | – | – | ns |
| $t_{DH}$ | Data Hold Time | 0 | – | – | 0 | – | – | ns |
| $t_{AW}$ | Address to Write Setup Time | 0 | – | – | 0 | – | – | ns |

* Ta = 25°C, $V_{CC}$ = 5V

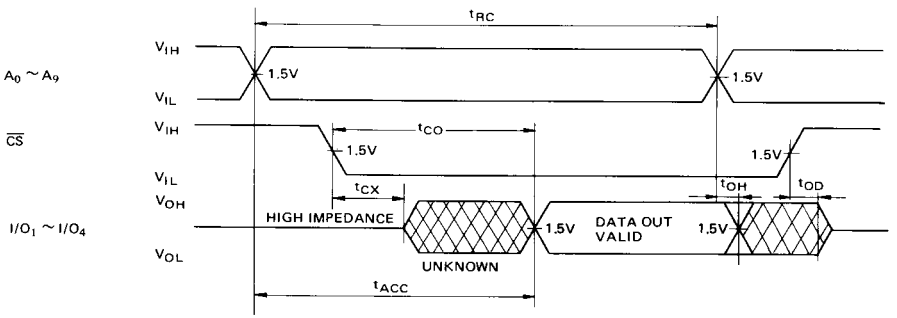
### CAPACITANCE (Ta = 25°C, f = 1MHz)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = AC Ground | – | – | 5 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = AC Ground | – | – | 10 | pF |

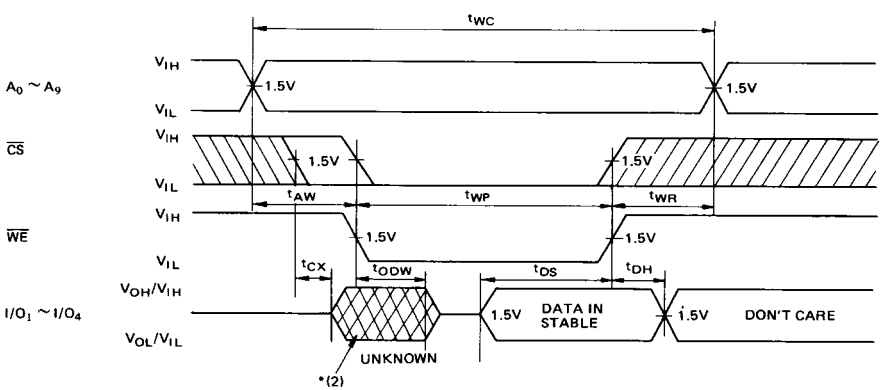
Note: This parameter is periodically sampled and not 100% tested.

## TIMING WAVEFORMS

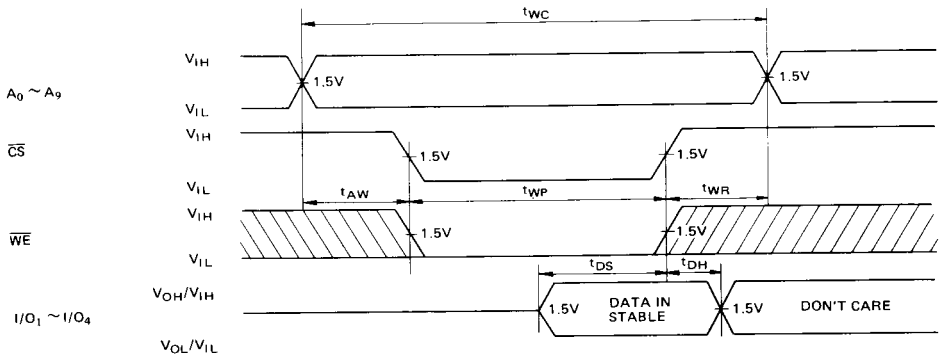
- **READ CYCLE**




- **WRITE CYCLE [1] *(1)**



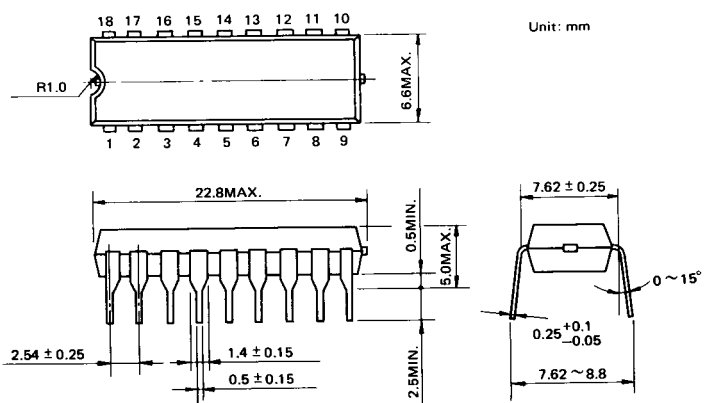
- **WRITE CYCLE [2] *(1)**




Note *(1): A write occurs during the overlap of a low $\overline{CS}$ and low $\overline{WE}$.
And twp is specified as the logical 'AND' of $\overline{CS}$ and $\overline{WE}$.

*(2): If the $\overline{CS}$ low transition occurs simultaneously with or latter from $\overline{WE}$ low transition, the output buffers remain in a high impedance state in this period.

## OUTLINE DRAWINGS




Note: All dimensions are in millimeters. Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 18 leads.