N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in a TO-18 envelope. Designed primarily as a line current interrupter in telephone sets, it can also be applied in other applications such as in relays, line and high-speed transformer drivers etc.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200 V
Drain current (DC)	I_D	max.	350 mA
Total power dissipation up to T_{case} = 25 °C	P_{tot}	max.	1.5 W
Drain-source ON-resistance I_D = 400 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	4.5 Ω 6.0 Ω
Transfer admittance I_D = 400 mA; V_{DS} = 25 V	$\|Y_{fs}\|$	min. typ.	140 mS 350 mS

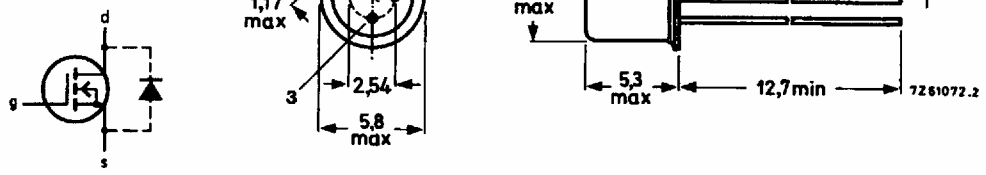
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-18.

Pinning

1 = source
2 = gate
3 = drain



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	350 mA
Drain current (peak)	I_{DM}	max.	1.4 A
Total power dissipation up to			
T_{amb} = 25 °C	P_{tot}	max.	0.4 W
T_{case} = 25 °C	P_{tot}	max.	1.5 W
Storage temperature range	T_{stg}	−55 to +	150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	310 K/W
From junction to case	$R_{th\ j\text{-}c}$	=	83 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage			
I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	200 V
Drain-source leakage current			
V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	200 nA
V_{DS} = 200 V; V_{GS} = 0	I_{DSS}	typ.	100 nA
		max.	10 μA
Gate-source leakage current			
V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100 nA
Gate threshold voltage			
I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min.	0.8 V
		max.	2.8 V
Drain-source ON-resistance			
I_D = 400 mA; V_{GS} = 10 V	R_{DSon}	typ.	4.5 Ω
		max.	6.0 Ω
Transfer admittance			
I_D = 400 mA; V_{DS} = 25 V	$\lvert y_{fs} \rvert$	min.	140 mS
		typ.	350 mS
Input capacitance at f = 1 MHz;			
V_{DS} = 25 V; V_{GS} = 0	C_{iss}	typ.	45 pF
		max.	60 pF
Output capacitance at f = 1 MHz;			
V_{DS} = 25 V; V_{GS} = 0	C_{oss}	typ.	15 pF
		max.	25 pF
Feedback capacitance at f = 1 MHz;			
V_{DS} = 25 V; V_{GS} = 0	C_{rss}	typ.	3.5 pF
		max.	10 pF
Switching times (see Figs 2 and 3)			
I_D = 300 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ.	5 ns
		max.	15 ns
	t_{off}	typ.	15 ns
		max.	25 ns

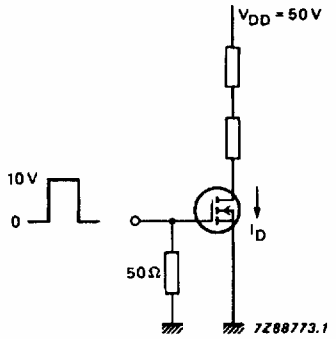


Fig. 2 Switching time test circuit.

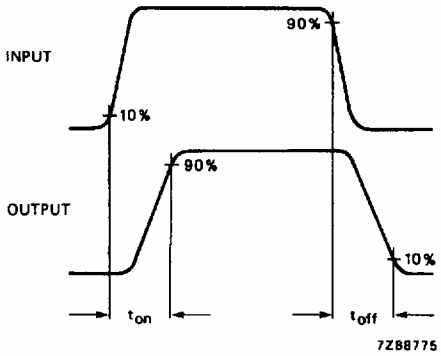


Fig. 3 Input and output waveforms.