MOTOROLA

MC8T14
MC8T24

TRIPLE LINE RECEIVERS WITH HYSTERESIS

SILICON MONOLITHIC
INTEGRATED CIRCUIT

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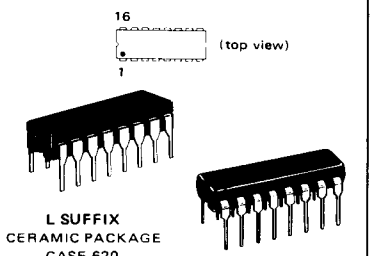
TRIPLE LINE RECEIVERS WITH HYSTERESIS

. . . specifically designed to meet the input/output specifications for IBM 360/370 Systems (IBM specification GA 22-6974-0). Each receiver incorporates hysteresis to provide high noise immunity and also high input impedance to minimize loading on the related driver.

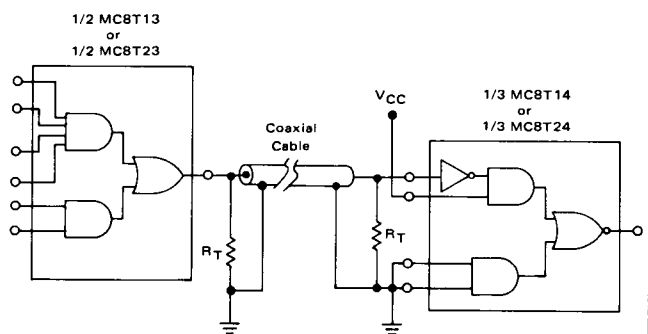
- Each Channel Can Be Independently Strobed
- High Speed – $t_{PLH} = t_{PHL} = 20$ ns
- Input Gating Provided on Each Line
- Operates on a Single +5.0 V Power Supply
- Fully Compatible with MTTL or MDTL Logic Systems
- Input Hysteresis Results in High Noise Immunity



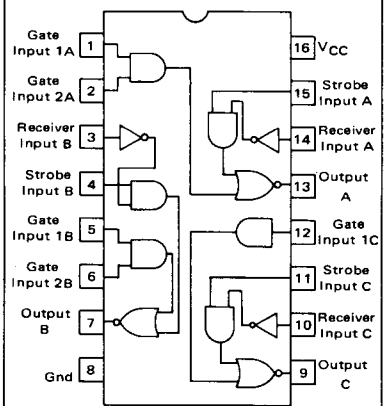
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

TYPICAL APPLICATION



PIN CONNECTIONS



TRUTH TABLE

Inputs				Output
Receiver	Strobe	Gate 1	Gate 2	
X	X	H	H	L
L	H	X	X	L
H	X	L	X	H
X	L	L	X	H
H	X	X	L	H
X	L	X	L	H

Where:
L = Low Logic State
H = High Logic State
X = Don't Care

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Receiver Input Voltage (V_{CC} = 0)	$V_{I(R)}$	7.0 6.0	Vdc
Strobe or Gate Input Voltage	$V_{I(S) \text{ or } (G)}$	5.5	Vdc
Output Voltage	V_O	7.0	Vdc
Output Current	I_O	±100	mA
Power Dissipation (Package Limitation) Ceramic Package Derate above 25°C	P_D	 1000 6.7	 mW mW/°C
Plastic Package Derate above 25°C		830 6.7	mW mW/°C
Junction Temperature Ceramic Package Plastic Package	T_J	 175 150	°C
Operating Ambient Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, 4.75 ≤ V_{CC} ≤ 5.25 V and 0°C ≤ T_A ≤ 75°C)

Characteristic	Symbol	MC8T14 Min	MC8T14 Typ	MC8T14 Max	MC8T24 Min	MC8T24 Typ	MC8T24 Max	Unit
Gate or Strobe Input Voltage — High Logic State	$V_{IH(G) \text{ or } (S)}$	2.0	–	–	2.0	–	–	V
Gate or Strobe Input Voltage — Low Logic State	$V_{IL(G) \text{ or } (S)}$	–	–	0.8	–	–	0.8	V
Receiver Input Voltage — High Logic State	$V_{IH(R)}$	2.0	–	–	1.7	–	–	Vdc
Receiver Input Voltage — Low Logic State	$V_{IL(R)}$	–	–	0.8	–	–	0.7	Vdc
Receiver Input Hysteresis (1) (V_{CC} = 5.0 V, T_A = 25°C, $V_{IL(G)}$ = 0, $V_{IH(S)}$ = 4.5 V)	$V_{H(R)}$	0.3	0.5	–	0.2	0.4	–	V
Input Clamp Voltage (V_{CC} = 5.0 V, T_A = 25°C, I_I = -12 mA) (Strobe or Gate Inputs)	$V_{IC(G) \text{ or } (S)}$	–	–	1.5	–	–	1.5	V
Input Breakdown Voltage (V_{CC} = 5.0 V, I_I = 10 mA) (Strobe or Gate Inputs)	$V_{I(G) \text{ or } (S)}$	5.5	–	–	5.5	–	–	V
Receiver Input Current — High Logic State ($V_{IH(R)}$ = 3.8 V) ($V_{IH(R)}$ = 3.11 V) ($V_{IH(R)}$ = 7.0 V) ($V_{IH(R)}$ = 6.0 V, V_{CC} = 0 V)	$I_{IH(R)}$	 – – – –	 – – – –	 0.17 – – –	 – – – –	 – – – –	 – 0.17 5.0 5.0	mA
Gate or Strobe Input Current — High Logic State ($V_{IH(S)}$ = 4.5 V, $V_{IH(R)}$ = 3.11 V) ($V_{IH(G)}$ = 4.5 V)	$I_{IH(G) \text{ or } (S)}$	 – –	 – –	 40 40	 – –	 – –	 40 40	μA
Gate or Strobe Input Current — Low Logic State ($V_{IL(G) \text{ or } (S)}$ = 0.4 V, $V_{IL(R)}$ = 0 V)	$I_{IL(G) \text{ or } (S)}$	-0.1	–	-1.6	-0.1	–	-1.6	mA
Output Voltage — High Logic State ($V_{IH(R)}$ = 2.0 V, $V_{IH(S)}$ = 2.0 V, $V_{IL(G)}$ = 0.8 V, I_{OH} = -800 μA) ($V_{IH(R)}$ = 0.8 V, $V_{IL(S)}$ = 0.8 V, $V_{IL(G)}$ = 0.8 V, I_{OH} = -800 μA) ($V_{IH(R)}$ = 1.7 V, $V_{IH(S)}$ = 2.0 V, $V_{IL(G)}$ = 0.8 V, I_{OH} = -800 μA) ($V_{IH(R)}$ = 0.7 V, $V_{IL(S)}$ = 0.8 V, $V_{IL(G)}$ = 0.8 V, I_{OH} = -800 μA)	V_{OH}	 2.6 2.6 – –	 3.5 3.5 – –	 – – – –	 – – 2.6 2.6	 – – 3.4 3.4	 – – – –	V
Output Voltage — Low Logic State ($V_{IL(R)}$ = 0.8 V, $V_{IH(S)}$ = 2.0 V, $V_{IL(G)}$ = 0.8 V, I_{OL} = 16 mA) ($V_{IL(R)}$ = 0.8 V, $V_{IL(S)}$ = 0.8 V, $V_{IH(G)}$ = 2.0 V, I_{OL} = 16 mA) ($V_{IL(R)}$ = 0.7 V, $V_{IH(S)}$ = 2.0 V, $V_{IL(G)}$ = 0.8 V, I_{OL} = 16 mA) ($V_{IL(R)}$ = 0.7 V, $V_{IL(S)}$ = 0.8 V, $V_{IH(G)}$ = 2.0 V, I_{OL} = 16 mA)	V_{OL}	 – – – –	 – – – –	 0.4 0.4 – –	 – – – –	 – – – –	 – – 0.4 0.4	V
Output Short-Circuit Current (2) ($V_{IH(R)}$ = 3.8 V, $V_{IL(G)}$ = 0 V, $V_{IL(S)}$ = 0, V_{CC} = 5.0 V, T_A = 25°C) ($V_{IH(R)}$ = 3.11 V, $V_{IL(G)}$ = 0 V, $V_{IL(S)}$ = 0 V, V_{CC} = 5.0 V, T_A = 25°C)	I_{OS}	 -50 –	 – –	 -100 –	 – -50	 – –	 – -100	mA
Power Supply Current (V_{CC} = 5.25 V, T_A = 25°C)	I_{CC}	–	60	72	–	60	72	mA

(1) The Input Hysteresis is defined as the difference the input voltage at which the output begins to go from the high logic state to the low logic state and the input voltage which causes the output to begin to go from the low logic state to the high logic state.

(2) Only one output may be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted.)

Parameter	Symbol	MC8T14, MC8T24			Unit
		Min	Typ	Max	
Propagation Delay Time – Receiver Input to High Logic State Output	$t_{PLH(R)}$	–	20	30	ns
Propagation Delay Time Receiver Input to Low Logic State Output	$t_{PHL(R)}$	–	20	30	ns
Propagation Delay Time Strobe Input to High Logic State Output	$t_{PLH(S)}$	–	–	–	ns
Propagation Delay Time Strobe Input to Low Logic State Output	$t_{PHL(S)}$	–	–	–	ns
Propagation Delay Time Gate Input to High Logic State Output	$t_{PLH(G)}$	–	–	–	ns
Propagation Delay Time Gate Input to Low Logic State Output	$t_{PHL(G)}$	–	–	–	ns

FIGURE 1 – RECEIVER PROPAGATION DELAY TIMES $t_{PLH(R)}$ and $t_{PHL(R)}$ TEST CIRCUIT AND WAVEFORMS

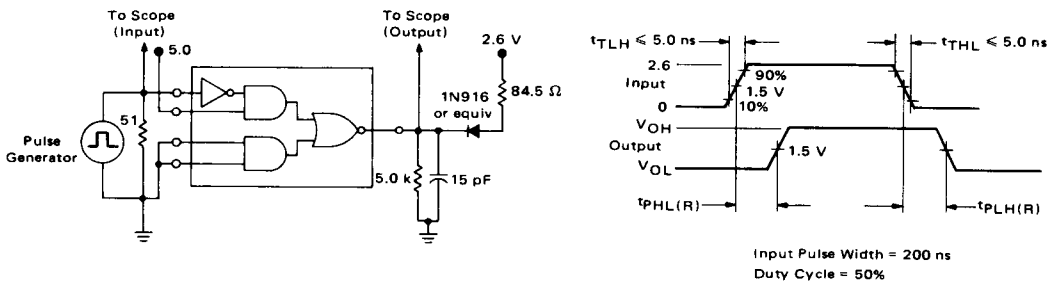


FIGURE 2 – GATE AND STROBE PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS

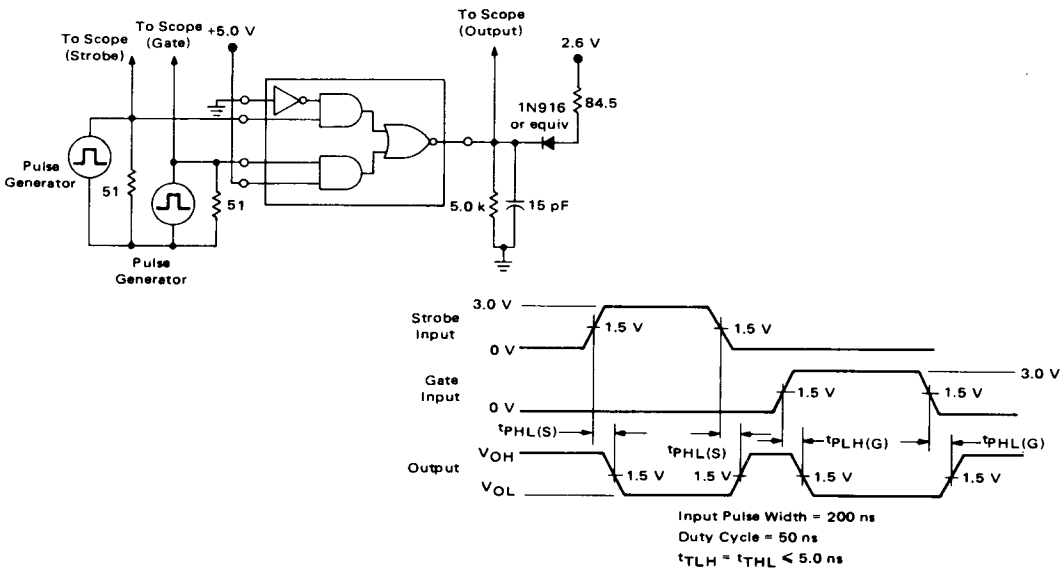


FIGURE 3 – TYPICAL RECEIVER HYSTERESIS CHARACTERISTIC

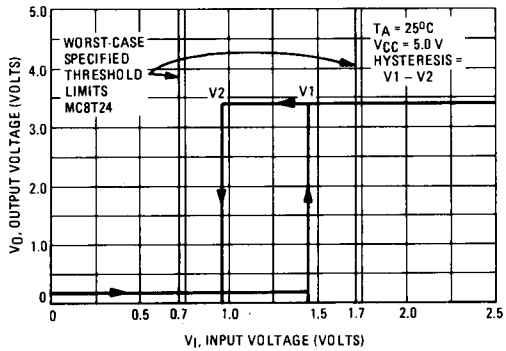
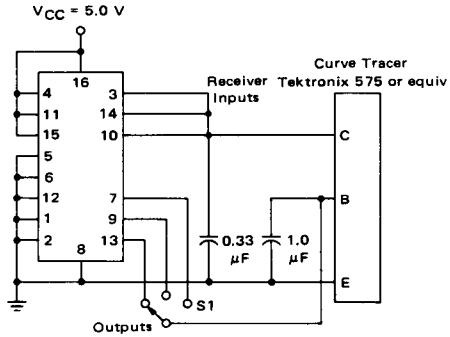
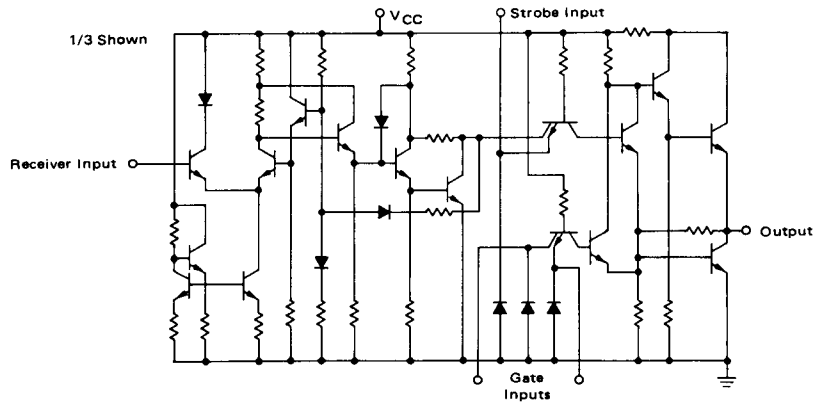


FIGURE 4 – HYSTERESIS TEST CIRCUIT



REPRESENTATIVE CIRCUIT SCHEMATIC



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