

100156



Not Intended For New Designs

T-46-07-01

# 100156 Mask-Merge/Latch

## General Description

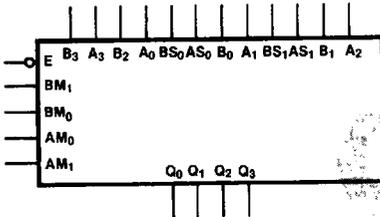
The 100156 merges two 4-bit words to form a 4-bit output word. The  $AM_n$  enable allows the merge of A into B by one, two or three places (per the  $AS_n$  value) from the left. The  $BM_n$  enable similarly allows the merge of B into A from the left (per the  $BS_n$  value). The B merge overrides the A merge when both are enabled. This means A first merges into B and B then merges into the A merge. If the B address is

equal to or greater than the A address, then outputs are forced to B.

The merge outputs feed four latches, which have a common enable ( $\bar{E}$ ) input. All inputs have a 50 k $\Omega$  (typical) pull-down resistor tied to  $V_{EE}$ .

**Ordering Code:** See Section 6

## Logic Symbol



TL/F/9861-3

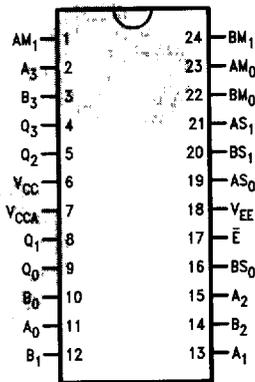
Pin Names	Description
$\bar{E}$	Latch Enable Input (Active LOW)
$A_0-A_3$	A Data Inputs
$B_0-B_3$	B Data Inputs
$AM_0, AM_1$	A Merge Enable Inputs
$BM_0, BM_1$	B Merge Enable Inputs
$AS_0, AS_1$	A Address Inputs
$BS_0, BS_1$	B Address Inputs
$Q_0-Q_3$	Data Outputs

**Note:**

When  $\bar{E}$  is HIGH,  $Q_n$  outputs do not change.  
When  $\bar{E}$  is LOW,  $Q_n = A$  or B depending on which is selected.

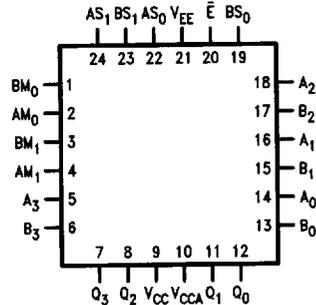
## Connection Diagrams

24-Pin DIP



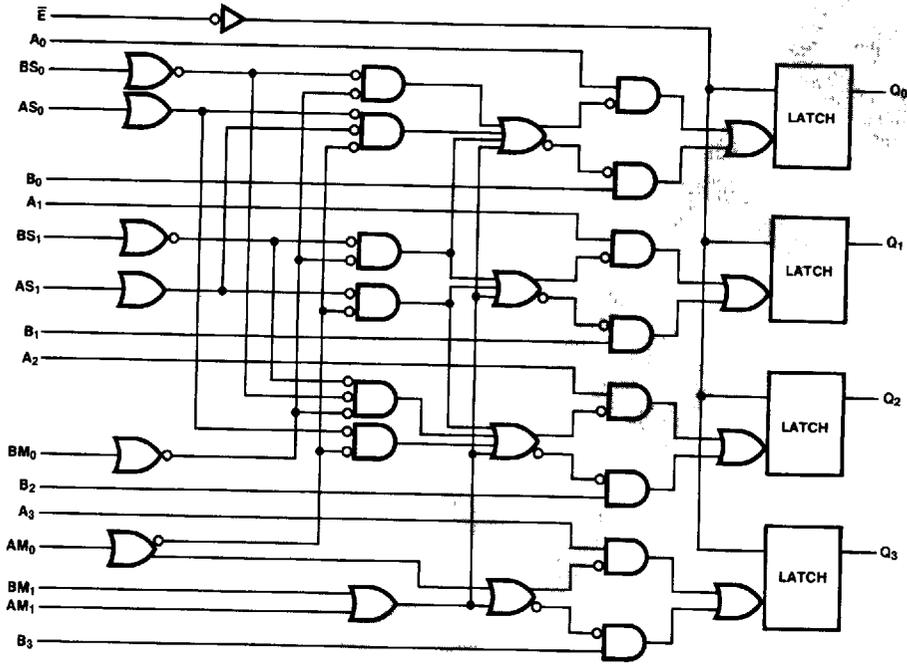
TL/F/9861-1

24-Pin Quad Cerpak



TL/F/9861-2

Logic Diagram



TL/F/9861-5

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**Truth Table**

Inputs									Outputs				Remarks	
Merge Enables				Addresses					E	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>		Q <sub>3</sub>
BM <sub>1</sub>	BM <sub>0</sub>	AM <sub>1</sub>	AM <sub>0</sub>	BS <sub>1</sub>	BS <sub>0</sub>	AS <sub>1</sub>	AS <sub>0</sub>							
X	X	H	X	X	X	X	X	L	B <sub>0</sub>	B <sub>1</sub>	B <sub>2</sub>	B <sub>3</sub>	Select B	
H	X	X	X	X	X	X	X	L	B <sub>0</sub>	B <sub>1</sub>	B <sub>2</sub>	B <sub>3</sub>		
L	L	L	L	X	X	X	X	L	A <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	Select A	
L	L	L	H	X	X	L	L	L	B <sub>0</sub>	B <sub>1</sub>	B <sub>2</sub>	B <sub>3</sub>	Merge A → B	
L	L	L	H	X	X	H	L	L	A <sub>0</sub>	A <sub>1</sub>	B <sub>2</sub>	B <sub>3</sub>		
L	L	L	H	X	X	H	H	L	A <sub>0</sub>	A <sub>1</sub>	B <sub>2</sub>	B <sub>3</sub>		
L	L	L	H	X	X	H	H	L	A <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	B <sub>3</sub>		
L	H	L	L	L	L	X	X	L	A <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	Merge B → A	
L	H	L	L	L	H	X	X	L	B <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>		
L	H	L	L	H	L	X	X	L	B <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>		
L	H	L	L	H	H	X	X	L	B <sub>0</sub>	B <sub>1</sub>	B <sub>2</sub>	A <sub>3</sub>		
L	H	L	H	L	L	L	H	L	A <sub>0</sub>	B <sub>1</sub>	B <sub>2</sub>	B <sub>3</sub>	Merge A → B	
L	H	L	H	L	L	H	L	L	A <sub>0</sub>	A <sub>1</sub>	B <sub>2</sub>	B <sub>3</sub>		
L	H	L	H	L	L	H	H	L	A <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	B <sub>3</sub>		
L	H	L	H	L	H	H	L	L	B <sub>0</sub>	A <sub>1</sub>	B <sub>2</sub>	B <sub>3</sub>	Merge A → B then Merge B → A	
L	H	L	H	L	H	H	H	L	B <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	B <sub>3</sub>		
L	H	L	H	L	H	H	H	L	B <sub>0</sub>	B <sub>1</sub>	A <sub>2</sub>	B <sub>3</sub>		
L	H	L	H	H	H	H	H	L	B <sub>0</sub>	B <sub>1</sub>	B <sub>2</sub>	B <sub>3</sub>	B Address ≥ A Address	
L	H	L	H	H	H	H	L	L	B <sub>0</sub>	B <sub>1</sub>	B <sub>2</sub>	B <sub>3</sub>		
L	H	L	H	H	H	H	L	L	B <sub>0</sub>	B <sub>1</sub>	B <sub>2</sub>	B <sub>3</sub>		
L	H	L	H	H	H	L	L	L	B <sub>0</sub>	B <sub>1</sub>	B <sub>2</sub>	B <sub>3</sub>		
L	H	L	H	H	L	L	H	L	B <sub>0</sub>	B <sub>1</sub>	B <sub>2</sub>	B <sub>3</sub>		
L	H	L	H	H	L	L	L	L	B <sub>0</sub>	B <sub>1</sub>	B <sub>2</sub>	B <sub>3</sub>		
L	H	L	H	L	H	L	L	L	B <sub>0</sub>	B <sub>1</sub>	B <sub>2</sub>	B <sub>3</sub>		
L	H	L	H	L	L	L	L	L	B <sub>0</sub>	B <sub>1</sub>	B <sub>2</sub>	B <sub>3</sub>		
X	X	X	X	X	X	X	X	H	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	Latch	
Before Start	At Start	After End	At End											

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Don't Care

### Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature -65°C to +150°C  
 Maximum Junction Temperature (T<sub>J</sub>) +150°C

Case Temperature under Bias (T<sub>C</sub>) 0°C to +85°C  
 V<sub>EE</sub> Pin Potential to Ground Pin -7.0V to +0.5V  
 Input Voltage (DC) V<sub>EE</sub> to +0.5V  
 Output Current (DC Output HIGH) -50 mA  
 Operating Range (Note 2) -5.7V to -4.2V

### DC Electrical Characteristics

V<sub>EE</sub> = -4.5V, V<sub>CC</sub> = V<sub>CCA</sub> = GND, T<sub>C</sub> = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V <sub>OH</sub>	Output HIGH Voltage	-1025	-955	-880	mV	V <sub>IN</sub> = V <sub>IH</sub> (Max) or V <sub>IL</sub> (Min)	Loading with 50Ω to -2.0V
V <sub>OL</sub>	Output LOW Voltage	-1810	-1705	-1620			
V <sub>OH</sub> C	Output HIGH Voltage	-1035			mV	V <sub>IN</sub> = V <sub>IH</sub> (Min) or V <sub>IL</sub> (Max)	Loading with 50Ω to -2.0V
V <sub>OL</sub> C	Output LOW Voltage			-1610			
V <sub>IH</sub>	Input HIGH Voltage	-1165		-880	mV	Guaranteed HIGH Signal for All Inputs	
V <sub>IL</sub>	Input LOW Voltage	-1810		-1475	mV	Guaranteed LOW Signal for All Inputs	
I <sub>IL</sub>	Input LOW Current	0.50			μA	V <sub>IN</sub> = V <sub>IL</sub> (Min)	

### DC Electrical Characteristics

V<sub>EE</sub> = -4.2V, V<sub>CC</sub> = V<sub>CCA</sub> = GND, T<sub>C</sub> = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V <sub>OH</sub>	Output HIGH Voltage	-1020		-870	mV	V <sub>IN</sub> = V <sub>IH</sub> (Max) or V <sub>IL</sub> (Min)	Loading with 50Ω to -2.0V
V <sub>OL</sub>	Output LOW Voltage	-1810		-1605			
V <sub>OH</sub> C	Output HIGH Voltage	-1030			mV	V <sub>IN</sub> = V <sub>IH</sub> (Min) or V <sub>IL</sub> (Max)	Loading with 50Ω to -2.0V
V <sub>OL</sub> C	Output LOW Voltage			-1595			
V <sub>IH</sub>	Input HIGH Voltage	-1150		-870	mV	Guaranteed HIGH Signal for All Inputs	
V <sub>IL</sub>	Input LOW Voltage	-1810		-1475	mV	Guaranteed LOW Signal for All Inputs	
I <sub>IL</sub>	Input LOW Current	0.50			μA	V <sub>IN</sub> = V <sub>IL</sub> (Min)	

### DC Electrical Characteristics

V<sub>EE</sub> = -4.8V, V<sub>CC</sub> = V<sub>CCA</sub> = GND, T<sub>C</sub> = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V <sub>OH</sub>	Output HIGH Voltage	-1035		-880	mV	V <sub>IN</sub> = V <sub>IH</sub> (Max) or V <sub>IL</sub> (Min)	Loading with 50Ω to -2.0V
V <sub>OL</sub>	Output LOW Voltage	-1830		-1620			
V <sub>OH</sub> C	Output HIGH Voltage	-1045			mV	V <sub>IN</sub> = V <sub>IH</sub> (Min) or V <sub>IL</sub> (Max)	Loading with 50Ω to -2.0V
V <sub>OL</sub> C	Output LOW Voltage			-1610			
V <sub>IH</sub>	Input HIGH Voltage	-1165		-880	mV	Guaranteed HIGH Signal for All Inputs	
V <sub>IL</sub>	Input LOW Voltage	-1830		-1490	mV	Guaranteed LOW Signal for All Inputs	
I <sub>IL</sub>	Input LOW Current	0.50			μA	V <sub>IN</sub> = V <sub>IL</sub> (Min)	

**Note 1:** Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Parametric values specified at -4.2V to -4.8V

**Note 3:** The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

**Note 4:** Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

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### DC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-4.8V$  unless otherwise specified,  $V_{CC} = V_{CCA} = GND$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$I_{IH}$	Input HIGH Current $A_n, B_n, BM_n, AM_n, BS_n, AS_n, \bar{E}$			265	$\mu A$	$V_{IN} = V_{IH}(Max)$
$I_{EE}$	Power Supply Current	-235	-161	-107	$mA$	Inputs Open

### Ceramic Dual-In-Line Package AC Electrical Characteristics

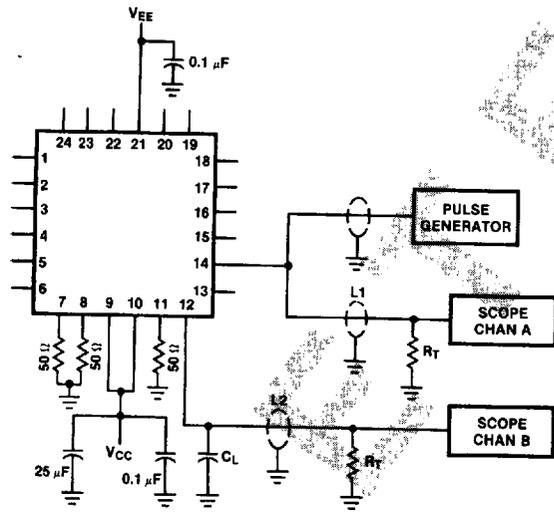
$V_{EE} = -4.2V$  to  $-4.8V$ ,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay $A_n, B_n$ to Outputs (Transparent Mode)	0.45	1.90	0.50	1.80	0.50	2.00	ns	Figures 1 and 2
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\bar{E}$ to Outputs	1.00	2.50	1.00	2.40	1.00	2.50	ns	
$t_{PLH}$ $t_{PHL}$	Propagation Delay $AM_n, BM_n, AS_n, BS_n$ to Outputs (Transparent Mode)	1.20	3.70	1.20	3.70	1.20	3.80	ns	
$t_{TLH}$ $t_{THL}$	Transition Time 20% to 80%, 80% to 20%	0.45	1.90	0.45	1.80	0.45	1.90	ns	
$t_S$	Setup Time $A_n, B_n$ $AM_n, BM_n, AS_n, BS_n$	0.80 2.90		0.80 2.90		0.80 2.90		ns	Figure 3
$t_H$	Hold Time $A_n, B_n$ $AM_n, BM_n, AS_n, BS_n$	2.10 0.80		2.10 0.80		2.10 0.80		ns	
$t_{pw(L)}$	Pulse Width LOW $\bar{E}$	2.00		2.00		2.00		ns	Figure 2

### Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-4.8V$ ,  $V_{CC} = V_{CCA} = GND$

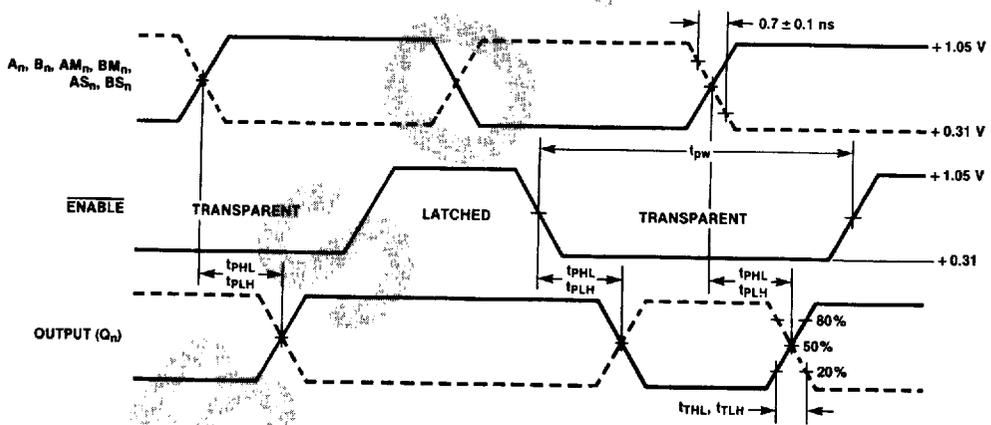
Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay $A_n, B_n$ to Outputs (Transparent Mode)	0.45	1.70	0.50	1.60	0.50	1.80	ns	Figures 1 and 2
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\bar{E}$ to Outputs	1.00	2.30	1.00	2.20	1.00	2.30	ns	
$t_{PLH}$ $t_{PHL}$	Propagation Delay $AM_n, BM_n, AS_n, BS_n$ to Outputs (Transparent Mode)	1.20	3.50	1.20	3.50	1.20	3.60	ns	
$t_{TLH}$ $t_{THL}$	Transition Time 20% to 80%, 80% to 20%	0.45	1.80	0.45	1.70	0.45	1.80	ns	
$t_S$	Setup Time $A_n, B_n$ $AM_n, BM_n, AS_n, BS_n$	0.70 2.80		0.70 2.80		0.70 2.80		ns	Figure 3
$t_H$	Hold Time $A_n, B_n$ $AM_n, BM_n, AS_n, BS_n$	2.00 0.70		2.00 0.70		2.00 0.70		ns	
$t_{pw(L)}$	Pulse Width LOW $\bar{E}$	2.00		2.00		2.00		ns	Figure 2



**Notes:**  
 $V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$   
 $L1$  and  $L2$  = equal length  $50\Omega$  impedance lines  
 $R_T = 50\Omega$  terminator internal to scope  
 Decoupling  $0.1\mu F$  from GND to  $V_{CC}$  and  $V_{EE}$   
 All unused outputs are loaded with  $50\Omega$  to GND  
 $C_L$  = Fixture and stray capacitance  $\leq 3\text{ pF}$   
 Pin numbers shown are for flatpak; for DIP see logic symbol

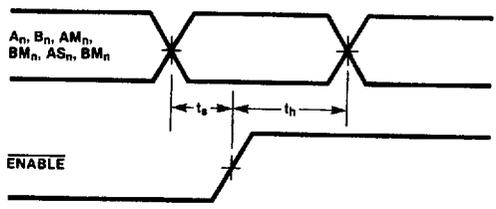
TL/F/9861-6

FIGURE 1. AC Test Circuit



TL/F/9861-7

FIGURE 2. Enable Timing



TL/F/9861-8

**Notes:**  
 $t_s$  is the minimum time before the transition of the enable that information must be present at the designated input.  
 $t_h$  is the minimum time after the transition of the enable that information must remain unchanged at the designated input.

FIGURE 3. Data Setup and Hold Times