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A Schlumberger Company

11C70 Master-Slave D-Type Flip-Flop

11C ECL Product

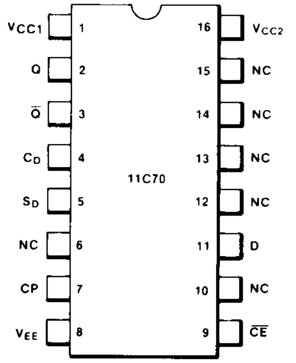
Description

The 11C70 is a high-speed ECL D-Type Master-Slave Flip-Flop capable of toggle rates over 650 MHz. Designed primarily for communications and instrumentation, it can also be used in other digital applications and is fully compatible with 10K ECL. Asynchronous Direct Set and Direct Clear inputs are provided which override the clock.

The circuit is voltage-compensated, which makes output levels and input thresholds insensitive to V_{EE} variations. This also allows operation with ECL supply voltage V_{EE} of -5.2V or with TTL supply V_{CC} of +5.0V. Each input has an internal 50KΩ pull-down resistor, which allows unused inputs to be left open. Open emitter-follower outputs accomodate a variety of loading and terminating schemes. The 11C70 is pin-compatible with the Motorola MC1670 but is a higher-frequency replacement.

Connection Diagram

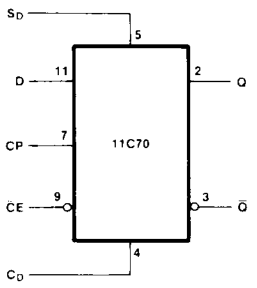
16-Pin DIP (Top View)



Pin Names

$\overline{CE}$	Clock Enable (Active LOW)
CP	Clock Pulse
D	Data Input
Q, $\overline{Q}$	Outputs
S_D	Direct Set
C_D	Direct Clear

Logic Symbol



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

Ordering Information

Package	Outline	Order Code
Ceramic DIP	4J	DC

Absolute Maximum Ratings Above which the useful life may be impaired

Storage Temperature	-65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Supply Voltage Range	-7.0V to GND
Input Voltage (DC)	V_{EE} to GND
Output Current (DC Output HIGH)	-50 mA
Operating Range	-5.7V to -4.7V
Lead Temperature (Soldering 10 sec.)	300°C

Guaranteed Operating Ranges

Supply Voltage (V_{EE})			Ambient Temperature (T_A)
Min	Typ	Max	
-5.7V	-5.2V	-4.7V	0°C to +75°C

DC Characteristics: V_{EE} = -5.2V, V_{CC} = GND

Symbol	Characteristic	Min	Typ	Max	Unit	T_A	Condition
V_{OH}	Output Voltage HIGH	-1000		-840	mV	0°C	V_{IN} = V_{IHA} or V_{ILB} per Truth Table loading 50Ω to -2V
		-960		-810		+25°C	
		-900		-720		+75°C	
V_{OL}	Output Voltage LOW	-1870		-1665	mV	0°C	
		-1850		-1620		+25°C	
		-1850		-1595		+75°C	
V_{OHC}	Output Voltage HIGH	-1020			mV	0°C	V_{IN} = V_{IHB} or V_{ILA} for D Input Loading 50Ω to -2V
		-980				+25°C	
		-920				+75°C	
V_{OLC}	Output Voltage LOW			-1615	mV	0°C	
				-1600		+25°C	
				-1575		+75°C	
V_{IH}	Input Voltage HIGH	-1135		-840	mV	0°C	Guaranteed Input Voltage HIGH for All Inputs
		-1095		-810		+25°C	
		-1035		-720		+75°C	
V_{IL}	Input Voltage LOW	-1870		-1500	mV	0°C	Guaranteed Input Voltage LOW for All Inputs
		-1850		-1485		+25°C	
		-1830		-1460		+75°C	
I_{IH}	Input Current HIGH				μA	+25°C	V_{IN} = V_{IHA}
	Clock Input			250			
	Data Input			270			
	S_D and C_D			550			
I_{IL}	Input Current LOW	0.5			μA	+25°C	V_{IN} = V_{IHB}
I_{EE}	Power Supply Current	-48			mA	+25°C	All Inputs Open

AC Characteristics: V_{EE} = -5.2V, V_{CC} = GND, T_A = +25°C

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
t_{PLH}, t_{PHL}	Propagation Delay (CP-Q)		1.1	1.4	ns	See Figures 3 and 4
t_{PLH}, t_{PHL}	Propagation Delay (S_D-$\overline{Q}$, C_D-Q)		1.3	1.7	ns	
t_{TLH}	Transition Time 20% to 80%		0.9	1.3	ns	
t_{THL}	Transition Time 80% to 20%		0.9	1.3	ns	
$f_{TOG(MAX)}$	Toggle Frequency (CP)	550	650		MHz	See Figure 2

Note: This device is guaranteed for $f_{TOG(max)} \geq$ 500 MHz over the 0°C to +75°C temperature range.

Truth Table

Inputs					Q_{t+1}	Operation
S_D	C_D	D	$\overline{CE}$	CP		
H	L	X	X	X	H	Direct Set
L	H	X	X	X	L	Direct Clear
H	H	X	X	X	—	Intermediate
L	L	X	H	↑	Q_t	Disable Clock
L	L	H	L	↑	H	Clocked Set
L	L	L	L	↑	L	Clocked Clear

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
↑ = LOW to HIGH Transition
t, t+1 = Time Before and After Clock Positive Transition

Functional Description

Master and slave clock thresholds are internally offset in opposite directions to avoid race conditions or simultaneous master-slave changes when the clock has slow rise or fall times. While the clock is LOW, the slave is in a HOLD condition and information present on the D input is gated into the master. When the clock goes HIGH, it locks the master into its present state, making it insensitive to the D input, causing the new information to appear on the outputs.

The CP and $\overline{CE}$ inputs are logically identical, but physical constraints associated with the Dual In-Line package make the $\overline{CE}$ input slower at the upper end of the toggle range. To prevent new data from entering the master on the next CP LOW cycle, $\overline{CE}$ should be HIGH while CP is still HIGH.

A HIGH signal on S_D or C_D will override the clocked inputs and force Q or $\overline{Q}$, respectively, to go HIGH. If both C_D and S_D are HIGH, the two output voltages will be somewhere between the HIGH and LOW levels and thus, cannot be usefully defined.

When the input signals for the 11C70 come from other ECL circuits, either 11CXX series or 10K types, these circuits will automatically provide appropriate signal swings, provided, of course, that these circuits are operated within their ratings and that due consideration is given to terminations appropriate to the particular application, as discussed in the Fairchild ECL Users Handbook.

For applications where the the clock signal comes from a circuit type other than ECL (in high frequency prescaling, for example) it is generally necessary to use external components to shift the signal levels and center them about the 11C70 input threshold region. A typical biasing scheme is shown in Figure 1. Resistors R1 and R2 are chosen such that the quiescent voltage at the CP input is -1.3V with respect to the V_{CC} terminal of the 11C70. Also indicated is the coupling from $\overline{Q}$ back to the D input to make a simple toggle. The clock source should be designed to provide a signal swing in the range of 400 mV to 1200 mV, peak-to-peak, over the specified frequency and temperature range. To avoid saturating the input transistor, and thus limiting the frequency capability, the positive peak of the clock should not be more positive than -0.4V with respect to V_{CC}.

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The 11C70 outputs have no internal pull-down resistors. When driving a microstrip line terminated at the far end by a resistor returned to -2V(w.r.t. V_{CC}), the quiescent I_{OH} current in the line performs the pull-down function when the output starts to go LOW. For series termination or for short unterminated lines, a 270Ω resistor to V_{EE} will provide adequate pull-down current. The outputs switch slightly faster when both outputs are equally loaded than if only one output is loaded. Equal and opposite changes in Q and $\overline{Q}$ load currents tend to cancel the effects of the small inductance of the V_{CC} pin.

The test arrangements illustrate the use of split power supplies, with a 2V V_{CC} and -3.2V V_{EE}. This is done as a matter of instrumentation convenience, since it allows the outputs to be connected via 50Ω cables directly to the sampling scope inputs, which have 50Ω internal terminations. By thus avoiding the use of probes, test correlation problems between supplier and user are minimized. In actual applications, only a single power supply is needed, and ground can be assigned to V_{CC}, as in ECL systems or to V_{EE} side as in TTL systems. RF bypass capacitors are recommended in either case.

Figure 1 Input Biasing for AC Coupled Triggering

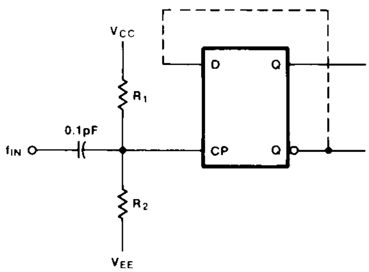
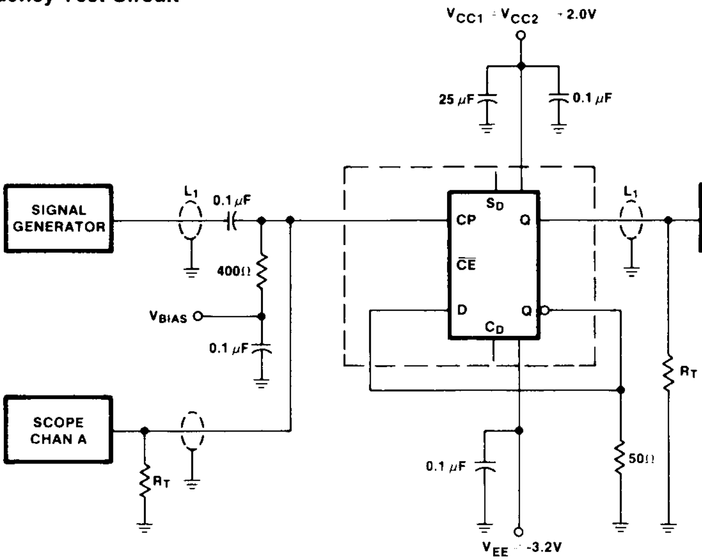


Figure 2 Toggle Frequency Test Circuit



RT 50Ω termination of scope
L1 50Ω impedance lines

Adjust VBIAS for + 0.7V baseline of 800mV peak-to-peak sinewave input

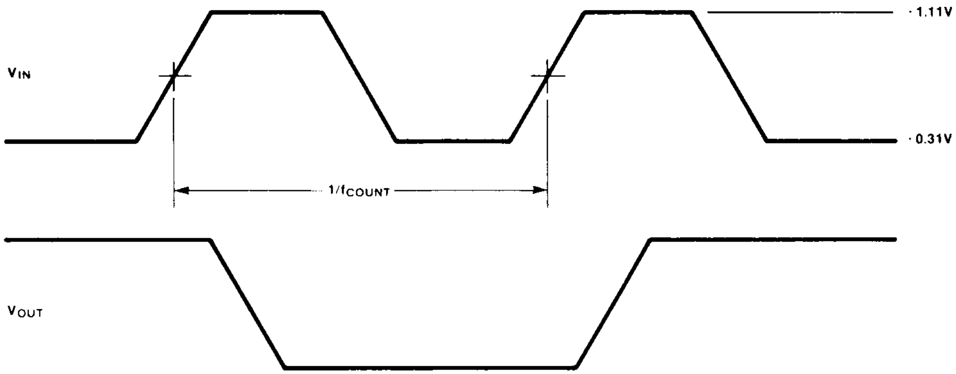
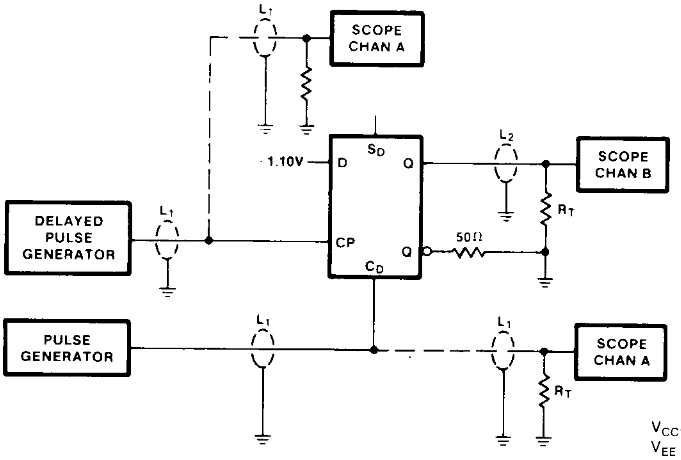


Figure 3 Propagation Delay and C_D Test Circuit



$V_{CC1} = V_{CC2} = +2.0V$
$V_{EE} = -3.2V$
$R_T = 50\Omega$ termination of scope
$L_1 = L_2$ equal 50Ω impedance lines
All input transition times are 2.0 ± 0.2 ns

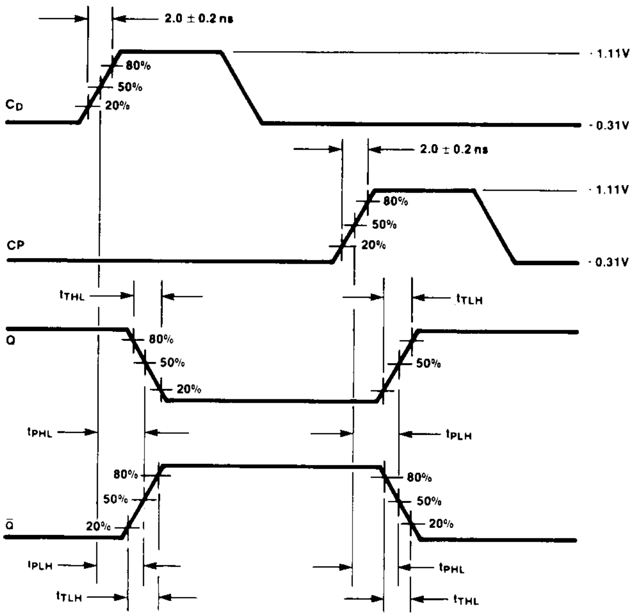
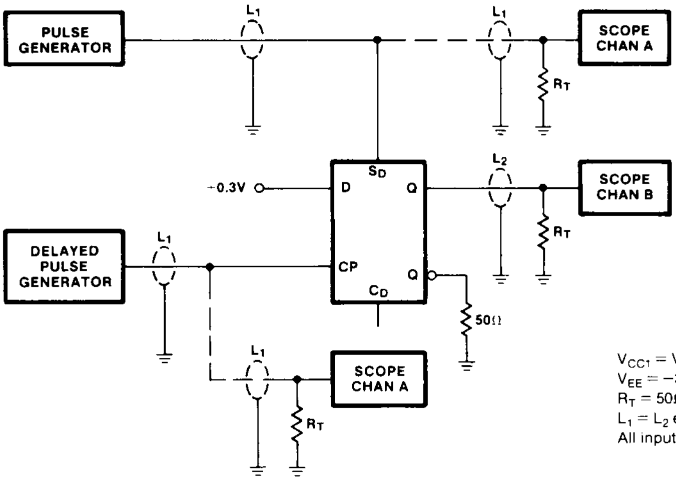


Figure 4 Propagation Delay and S_D Test Circuit



$V_{CC1} = V_{CC2} = +2.0V$
$V_{EE} = -3.2V$
$R_T = 50\Omega$ termination of scope
$L_1 = L_2$ equal 50Ω impedance lines
All input transition times are 2.0 ± 0.2 ns