



MMC 40107

DUAL 2-INPUT NAND BUFFER/DRIVER

GENERAL DESCRIPTION

The MMC 40107 is a monolithic ic. available in 14-lead dual in-line ceramic package and plastic package.

The MMC 40107 is a dual 2-input NAND buffer/driver containing two independent 2-input NAND buffers with open-drain single n-channel transistor outputs.

This device features a wired-OR capability and high output sink current capability (136 mA typ at $V_{DD} = 10\text{ V}$, $V_{DS} = 1\text{ V}$).

FEATURES

- quiescent current specified to 20 V
- maximum input leakage of $1\text{ }\mu\text{A}$ at 18 V (full package temperature range)
- standardized symmetrical output characteristics
- 5 V, 10 V, and 15 V parametric ratings

APPLICATIONS

Driver circuits

ABSOLUTE MAXIMUM RATINGS

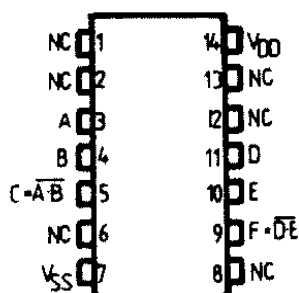
V_{DD}^*	Supply voltage: G and H types	-0.5 to	20	V
	E and F types	-0.5 to	18	V
V_i	Input voltage	-0.5 to	$V_{DD} + 0.5$	V
I_{i1}	DC input current (any one input)		± 10	mA
P_{tot}	Total power dissipation (per package)		200	mW
	Dissipation per output transistor for $T_A =$ full package-temperature range		100	mW
T_A	Operating temperature: G and H types	-55 to	125	$^{\circ}\text{C}$
	E and F types	-40 to	85	$^{\circ}\text{C}$
T_{stg}	Storage temperature	-65 to	150	$^{\circ}\text{C}$

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}^*	Supply voltage: G and H types	3 to	18	V
	E and F types	3 to	15	V
V_i	Input voltage	0 to	V_{DD}	V
T_A	Operating temperature: G and H types	-55 to	125	$^{\circ}\text{C}$
	E and F types	-40 to	85	$^{\circ}\text{C}$

CONNECTION DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended* operating conditions)

PARAMETER			TEST CONDITIONS				VALUES						UNIT	
			V _I (V)	V _O (V)	I _O (μ A)	V _{DD} (V)	T _{LOW}		25°C			T _{HIGH}		
							min.	max.	min.	typ	max.	min.		max.
I _L Quiescent current	G, H types	0/ 5			5		1		0.02	1		30	μ A	
		0/10			10		2		0.02	2		60		
		0/15			15		4		0.02	4		120		
		0/20			20		20		0.04	20		600		
	E, F types	0/ 5			5		4		0.02	4		30		
		0/10 0/15			10 15		8 16		0.02 0.02	8 16		60 120		
V _{IH} ** Input high voltage				0.5/4.5 1/9 1.5/12.5	< 1 < 1 < 1	5 10 15	3.5 7 11		3.5 7 11		3.5 7 11	V		
V _{IL} ** Input low voltage				4.5 9 13.5	< 1 < 1 < 1	5 10 15		1.5 3 4		1.5 3 4		1.5 3 4	V	
I _{OL} Output sink current	G, H types	5	0.4		5	21		16	32		12		mA	
		5	1		5	44		30	68		25			
		10	0.5		10	49		37	74		28			
		10	1		10	89		68	136		51			
		15	0.5		15	66		50	100		38			
	E, F types	5	0.4		5	17		13.6	32		12			
		5	1		5	35.7		25.5	68		22			
		10	0.5		10	39.1		31.4	74		27			
		10	1		10	72.2		57.8	136		51			
		15	0.5		15	53.5		42.5	100		37			
I _{OH} Output drive current			No internal pull-up device											
I _{IH} , I _{IL} Input leakage current	G, H types	0/18	Any input		18		± 0.1		$\pm 10^{-5}$	± 0.1		± 1	μ A	
	E, F types	0/15			15		± 0.3		$\pm 10^{-5}$	± 0.3		± 1		
I _{OH} , I _{OL} ** 3-state output leakage current	G, H types	0/18	18		18		2		10 ⁻⁴	2		20	μ A	
	E, F types	0/15	15		15		2		10 ⁻⁴	2		20		
C _I Input capacitance			Any input						5	7.5			pF	
C _O Output capacitance			Any output						30					

* T_{LOW} = -55°C for G, H devices; -40°C for E, F devices.* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V2 V min. with V_{DD} = 10 V2.5 V min. with V_{DD} = 15 V** Measured with external pull-up resistor, R_L = 10 K Ω to V_{DD}

*** Forced output disabled

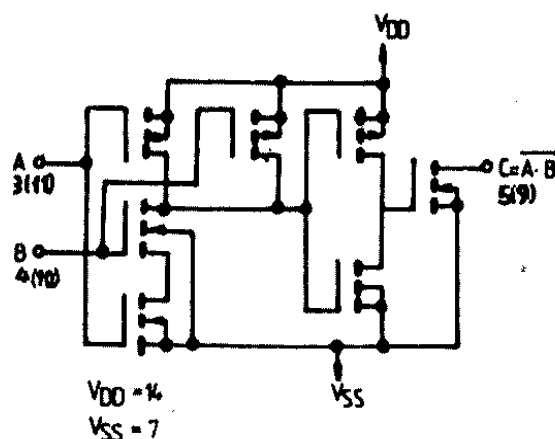
DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, typical temperature coefficient for all V_{DD} values is $0.3\%/^\circ\text{C}$, all input rise and fall time 20 ns)

PARAMETER		TEST CONDITIONS	VALUES			UNIT
		V _{DD} (V)	min.	typ.	max.	
t _{PHL}	Propagation delay time	R _L *=120 Ω	5	100	200	ns
t _{PLH}	High-to-Low		10	45	90	
			15	30	60	
	Low-to-High	R _L *=120 Ω	5	100	200	ns
			10	60	120	
			15	50	100	
t _{THL}	Transition time	R _L *=120 Ω	5	50	100	ns
t _{TLH}	High-to-Low		10	20	40	
			15	10	20	
	Low-to-High	R _L *=120 Ω	5	50	100	ns
			10	35	70	
			15	25	50	

* R_L is external pull-up resistor to V_{DD} .

SCHEMATIC DIAGRAM AND TRUTH TABLE



TRUTH TABLE

A	B	C
0	0	1 [*] Z [*]
1	0	1 [*] Z [*]
0	1	1 [*] Z [*]
1	1	0

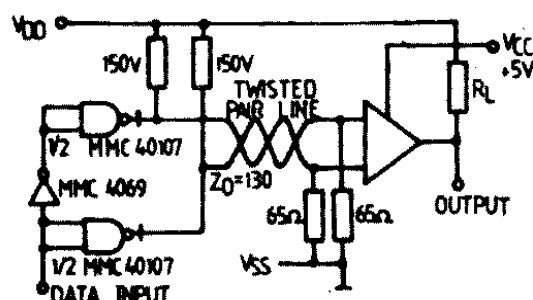
* Requires external pull-up resistor (R_L) to V_{DD}

* Without pull-up resistor (3-state)

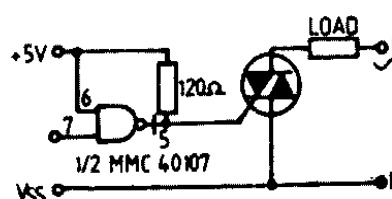
TYPICAL APPLICATIONS

The bar on the output line of this logic diagram indicates that the output is open drain as is shown in the previous schematic diagram and truth table.

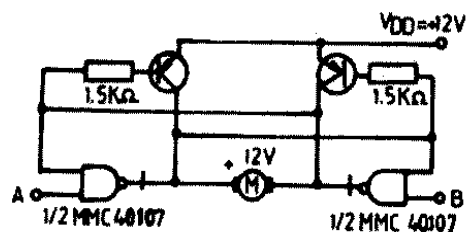
Line-driver circuit *



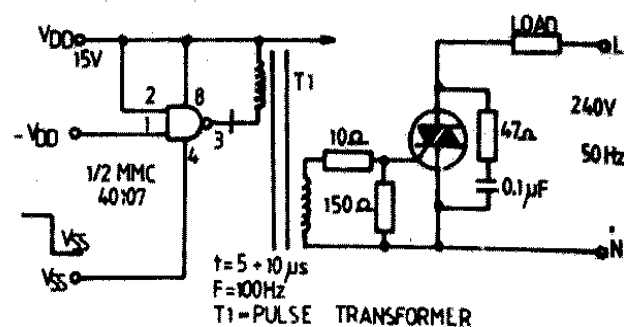
Direct dc drive interface of 40107 with a triac



Motor-controller circuit

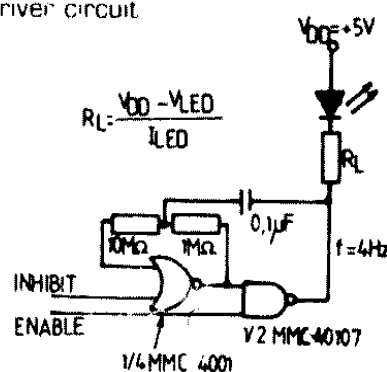


Interface of 40107 with triac whit COS/MOS component and triac isolated

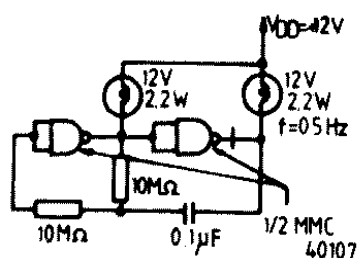


A	B	MOTOR FUNCTION
0	0	OFF
1	0	COUNTER CLOCKWISE
1	1	AS PREVIOUS STATE
0	1	CLOCKWISE
1	1	AS PREVIOUS STATE

LED driver circuit



A 22 watt incandescent lamp-driver circuit



INHIBIT	ENABLE	OUTPUT
0	0	OFF
1	0	OFF
0	1	OFF
1	1	ON

Multiplexed LED circuit

