



MMC 40192 MMC 40193

PRESETTABLE UP/DOWN COUNTERS (DUAL CLOCK WITH RESET) 40192-BCD TYPE 40193-BINARY TYPE

GENERAL DESCRIPTION

The MMC 40192, MMC 40193 are monolithic integrated circuits processed in standard Al-gate technology. The MMC 40192 is a 4-Bit Synchronous Up/Down Decade Counter and the MMC 40193 is a 4-Bit Synchronous Up/Down Binary Counter. Counting up and counting down is performed by two count inputs (CLOCK UP and CLOCK DOWN respectively), one being held high while the other is clocked. The outputs (Q_1 — Q_4) change on the positive-going transition of this clock. These counters feature preset inputs (J_1 — J_4) that are enabled when load (PRESET ENABLE) is a logical „0“ and a clear (RESET) which forces all outputs to „0“ when it is at logical „1“. The counters also have CARRY and BORROW inputs so that they can be cascaded using no external circuitry.

FEATURES

- Individual clock lines for counting up or counting down
- Synchronous high-speed carry and borrow propagation delays for cascading
- Active low parallel load
- Active high asynchronous reset
- Quiescent current specified at 20 V
- 5 V, 10 V, 15 V parametric ratings

ABSOLUTE MAXIMUM RATINGS

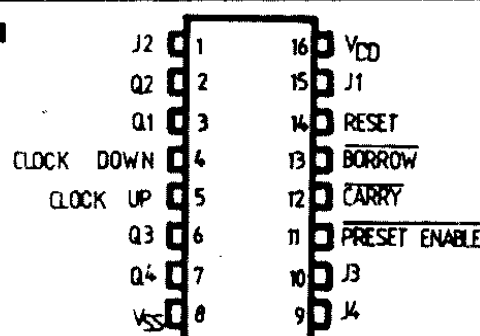
V_{DD}^*	Supply voltage: G and H types	-0.5 to 20	V
	E and F types	-0.5 to 18	V
V_i	Input voltage	-0.5 to $V_{DD}+0.5$	V
I_i	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_A = full package-temperature range	100	mW
T_A	Operating temperature :		
	G and H types	-55 to 125	°C
	E and F types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

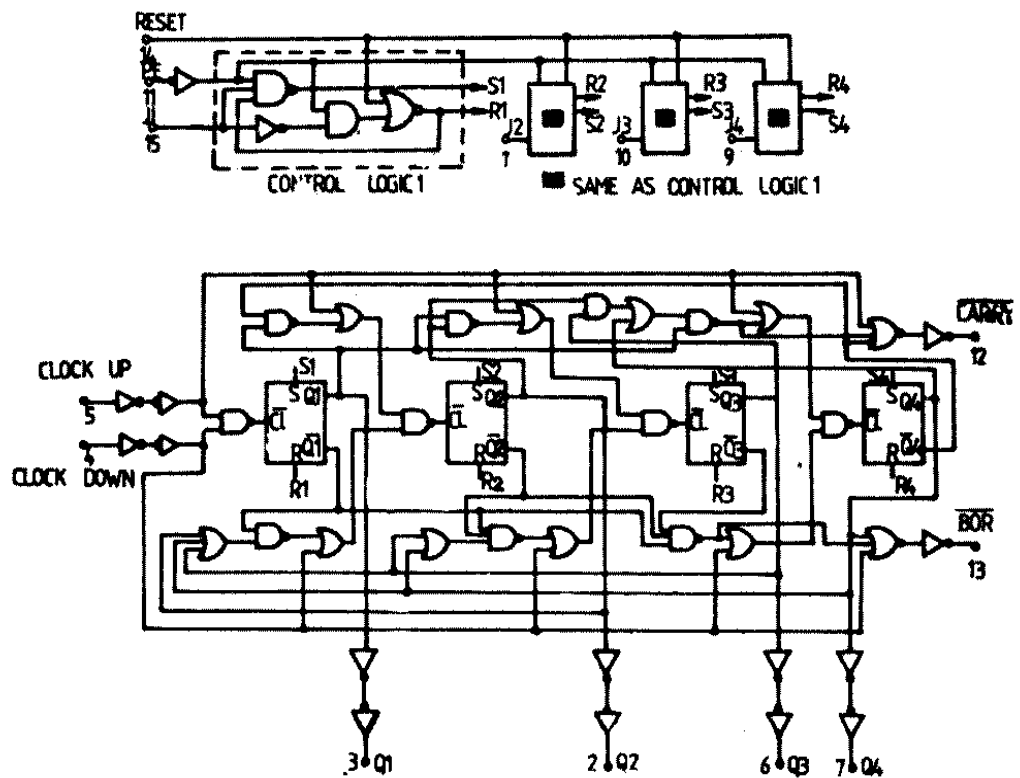
V_{DD}^*	Supply voltage: G and H types	3 to 18	V
	E and F types	3 to 15	V
V_i	Input voltage	0 to V_{DD}	V
T_A	Operating temperature :		
	G and H types	-55 to 125	°C
	E and F types	-40 to 85	°C

CONNECTION DIAGRAM

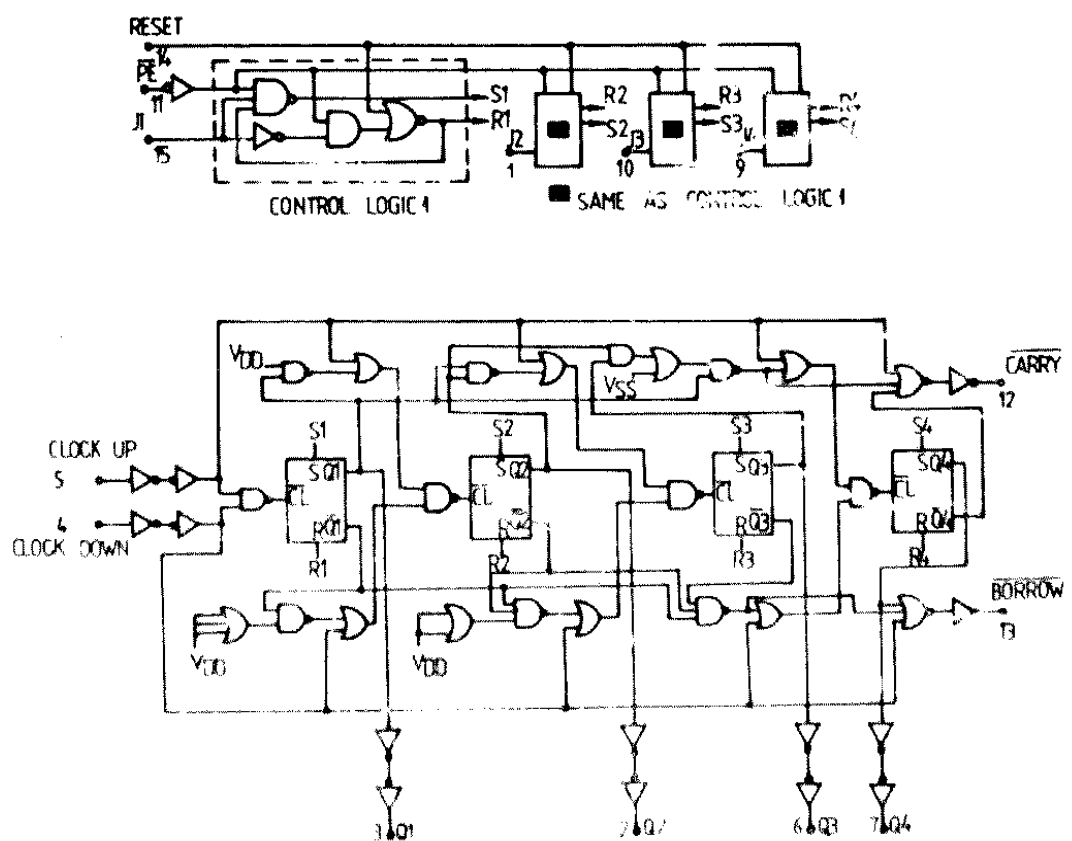


LOGIC DIAGRAM

MMC 40192

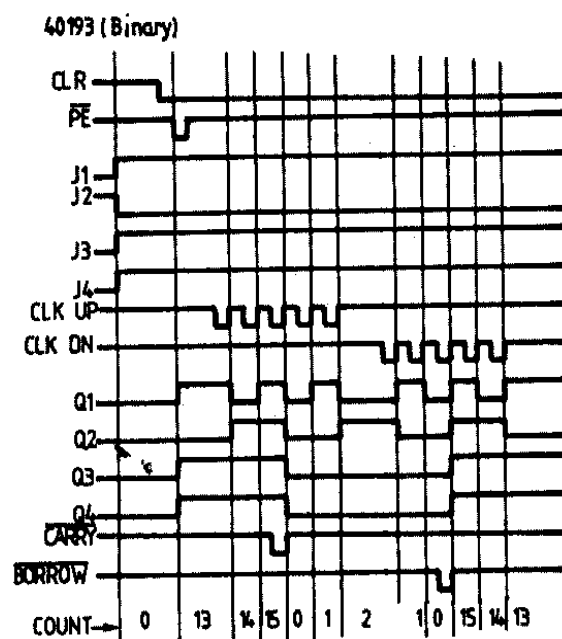
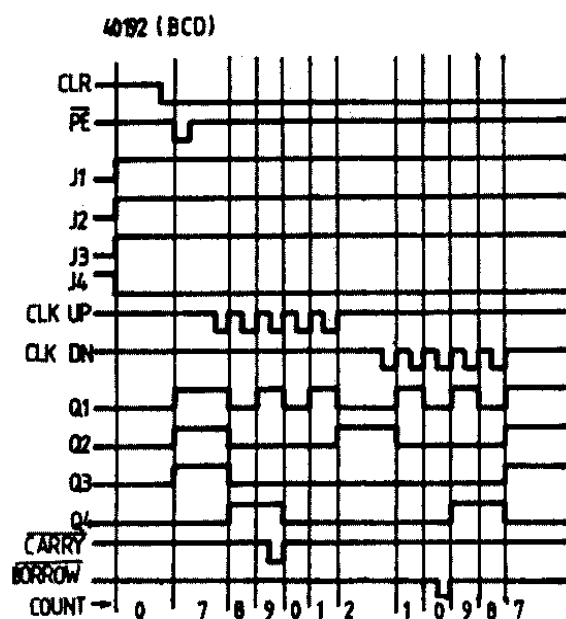


MMC 40193

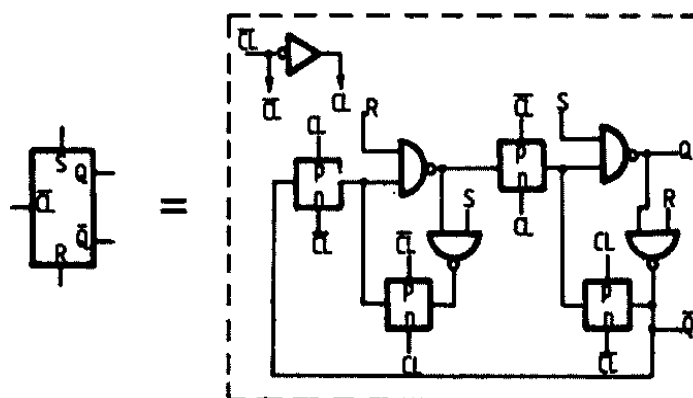


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TIMING DIAGRAM



Internal logic of flip-flop



TRUTH TABLE

CLOCK UP	CLOCK DOWN	PRESET ENABLE	RESET	ACTION
 1 1 X X	 1 1 X X	1 1 1 1 0 X	0 0 0 0 0 1	COUNT UP NO COUNT COUNT DOWN NO COUNT PRESET RESET

1 = HIGH LEVEL

0 = LOW LEVEL

X = DON'T CARE

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V _I (V)	V _O (V)	I _O (μ A)	V _{DD} (V)	T _{LOW}		25°C			T _{HIGH}		
							min.	max.	min.	typ	max.	min	max.	
I _L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μ A
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V _{OH}	Output high voltage		0/ 5 0/10 0/15		< 1 < 1 < 1	5 10 15	4.95 9.95 14.95		4.95 9.95 14.95			4.95 9.95 14.95		V
V _{OL}	Output low voltage		5 / 0 10/ 0 15/ 0		< 1 < 1 < 1	5 10 15		0.05 0.05 0.05			0.05 0.05 0.05		0.05 0.05 0.05	V
V _{IH}	Input high voltage			0.5/4.5 1/ 9 1.5/13.5	< 1 < 1 < 1	5 10 15	3.5 7 11		3.5 7 11			3.5 7 11		V
V _{IL}	Input low voltage			4.5/0.5 9/ 1 13.5/1.5	< 1 < 1 < 1	5 10 15		1.5 3 4			1.5 3 4		1.5 3 4	V
I _{OH}	Output drive current	G, H types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		E, F types	0/ 5	2.5		5	-1.53		-1.36	-3.2		-1.1		
			0/ 5	4.6		5	-0.52		-0.44	-1		-0.36		
			0/10	9.5		10	-1.3		-1.1	-2.6		-0.9		
			0/15	13.5		15	-3.6		-3.0	-6.8		-2.4		
I _{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I _{IK} , I _{IL}	Input leakage current	G, H types	0/18	Any input		13		± 0.1		$\pm 10^{-5}$	± 0.1		± 1	μ A
		E, F types	0/15			15		± 0.3		$\pm 10^{-5}$	± 0.3		± 1	
C _I	Input capacitance			Any input						5	7.5			pF

* T_{LOW} = -55°C for G, H devices; -40°C for E, F devices.* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V2 V min. with V_{DD} = 10 V2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$, typical temperature coefficient for all V_{DD} values is $0.3\%/^\circ\text{C}$, all input rise and fall times = 20 ns)

PARAMETER		TEST CONDITIONS		VALUES			UNIT
			$V_{DD}(\text{V})$	min.	typ.	max.	
t_{PHL}	Propagation delay time		5		250	500	ns
t_{PLH}	Clock Up or Clock Down to Q		10		120	240	
	Reset to Q		15		90	180	
	$\overline{\text{PE}}$ to Q		5		200	400	ns
			10		100	200	
			15		70	140	
	Clock Up to $\overline{\text{Carry}}$		5		160	320	ns
	Clock Down to $\overline{\text{Borrow}}$		10		80	160	
			15		60	120	
	$\overline{\text{Reset}}$ or $\overline{\text{PE}}$ to $\overline{\text{Borrow}}$ or $\overline{\text{Carry}}$		5		300	600	ns
			10		150	300	
			15		110	220	
t_{THL}	Transition time		5		100	200	ns
t_{TLH}			10		50	100	
			15		40	80	
t_{rem}^*	Removal time		5	80	40		ns
	Reset or $\overline{\text{PE}}$		10	40	20		
			15	30	15		
t_W	Clock input pulse width		5	480	240		ns
	Reset		10	300	150		
			15	260	130		
	$\overline{\text{PE}}$		5		120	240	ns
			10		85	170	
			15		70	140	
	Clock		5		90	180	ns
			10		45	90	
			15		30	60	
t_r, t_f	Clock input rise or fall time		5			15	μs
			10			15	
			15			5	
t_{CL}	Maximum clock input frequency		5	2	4		MHz
			10	4	8		
			15	5.5	11		

* The time required for Reset or Preset Enable control to be removed before clocking (see timing diagram).

Timing diagram defining t_{rem}

