

**MMC4046**

MICROPOWER PHASE -LOCKED LOOP

GENERAL DESCRIPTION

The MMC 4046 micropower phase-locked loop (PLL) consists of a low power, linear, voltage-controlled oscillator (VCO), a source follower, a zener diode, and two stage comparators. The two phase comparators have a common signal input and a common comparator input. The signal input can be directly coupled for a large voltage signal, or capacitively coupled to the self-biasing amplifier at the signal input for a small voltage signal.

FEATURES

- Wide supply voltage range -3V to 18V
- Low dynamic power consumption -70 μ W (typ) at $f_o=10$ kHz, $V_{DD}=5$ V
- VCO frequency -1.3 MHz (typ) at $V_{DD}=10$ V

APPLICATIONS

- FM demodulator and modulator
- Frequency synthesis and multiplication
- Frequency discrimination
- Data synchronization and conditioning
- Voltage-to-frequency conversion
- Tone decoding
- Motor speed control

ABSOLUTE MAXIMUM RATINGS

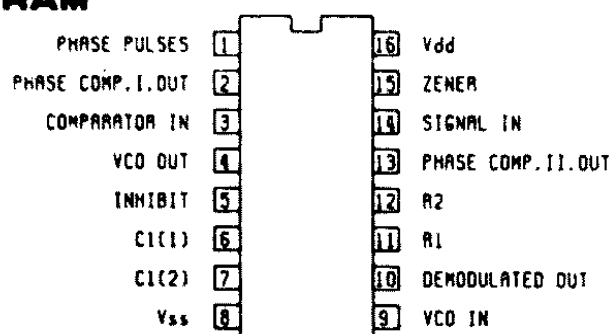
V_{DD}^*	Supply voltage: G and H types	-0.5 to	20	V
	E and F types	-0.5 to	18	V
V_i	Input voltage	-0.5 to	$V_{DD}+0.5$	V
I_i	DC input current (any one input)		± 10	mA
P_{tot}	Total power dissipation (per package)		200	mW
	Dissipation per output transistor			
	for T_A = full package-temperature range		100	mW
T_A	Operating			
	temperature: G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C
T_{stg}	Storage temperature	-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}^*	Supply voltage: G and H types	3 to	18	V
	E and F types	3 to	15	V
V_i	Input voltage	0 to	V_{DD}	V
T_A	Operating			
	temperature: G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C

CONNECTION DIAGRAM



[illegible]

The VCO requires one external capacitor C1 and one or two external resistors (R₁ or R₁ and R₂). Resistor R₁ and capacitor C₁ determine the frequency range of the VCO and resistor R₂ enables the VCO to have a frequency offset if required. The high input impedance (10¹² Ω) of the VCO simplifies the design of low pass filters by permitting the designer a wide choice of resistor-to-capacitor ratios in order not to load the low pass filter. A source-follower output of the VCO input voltage is provided at terminal 10 (DEMODULATED OUTPUT). If this terminal is used, a load resistor (R_S) of 10K or more should be connected from this terminal to V_{SS}. If unused this terminal should be left open. The VCO can be connected either directly or through frequency dividers to the comparator input of the phase comparators. A full CMOS logic swing is available at the output of the VCO and allows direct coupling to CMOS frequency dividers such as the MMC 4024, MMC 4018, MMC 4020, MMC 4022, MMC4029, MMC4059. One or more MMC 4018 (Presettable Divide-by-N-Counter) or MMC 4029 (presettable Up/Down Counter), together with the MMC 4046, (phase-Locked Loop) can be used to build a micropower low-frequency synthesizer. A logic 0 on the INHIBIT input "enables" the VCO and the source follower, while a logic 1 "turns off" both to minimize standby power consumption.

PHASE COMPARATORS

The phase-comparator signal input (terminal 14) can be direct-coupled provided the signal swing is within CMOS logic levels /logic "0" < 30% ($V_{DD}-V_{SS}$), logic "1" > 70% ($V_{DD}-V_{SS}$)/. For smaller swings the signal must be capacitively coupled to the self-biasing amplifier at the signal input. Phase comparator I is an exclusive-OR network; it operates analogously to an over-driver balanced mixer. To maximize the lock range, the signal-and-comparator-input frequencies must have a 50% duty cycle. With no signal or noise on the signal input, this phase comparator has an average output voltage equal to $V_{DD}/2$. The low-pass filter connected to the output of phase comparator I supplies the averaged voltage to the VCO input, and causes the VCO to oscillate at the center frequency (f_0). The frequency range of input signals on which the PLL will lock if it was initially out of lock is defined as the frequency capture range ($2f_c$). The frequency range of input signals on which the loop will stay locked if it was initially in lock is defined as the frequency lock range ($2f_L$). The capture range is < the lock range. With phase comparator I the range of frequencies over which the PLL can acquire lock (capture range) is dependent on the low-pass-filter characteristics, and can be made as large as the lock range. Phase-comparator I enables a PLL system to remain in lock in spite of high amounts of noise in the input signal. One characteristic of this type of phase comparator is that it may lock into input frequencies that are close to harmonics of the VCO center-frequency. A second characteristic is that the phase angle between the signal and the comparator input varies between 0° and 180° , and is 90° at the center frequency. Fig. (a) shows the typical, triangular, phase-to-output response characteristic of phase-comparator I. Typical waveforms for a CMOS phase-locked-loop employing phase comparator I in locked condition f_n is shown in Fig. (b).

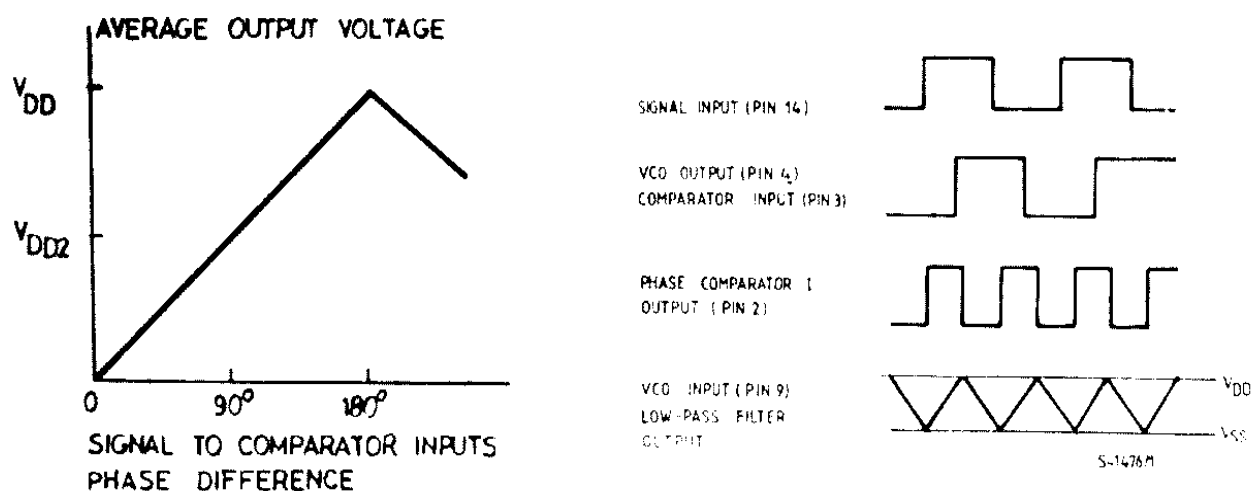
Phase-comparator II is an edge-controlled digital memory network. It consists of four flip-flop stages, control gating, and a three-stage output comprising p-and n-type drivers having a common output node. When the p-MOS or n-MOS drivers are ON they pull the output up to V_{DD} or down to V_{SS} , respectively. This type of phase comparator acts only on the positive edges of the signal and comparator inputs. The duty cycles of the signal and comparator inputs are not important since positive transitions control the PLL system utilizing this type of comparator. If the signal-input frequency is higher than the comparator-input frequency, the p-type output driver is maintained ON most of the time, and both n-and p-drivers OFF (3 state) the remainder of the time. If the signal-input frequency is lower than the comparator-input frequency, the n-type output driver is maintained ON most of the time, and both the n-and p-drivers OFF (3 state) the remainder of the time. If the signal and comparator-input frequencies are the same, but the signal input lags the comparator input in phase, the n-type output driver is maintained ON for a time corresponding to the phase difference. If the signal and comparator-input frequencies are the same, but the comparator input lags the signal in phase, the p-type output driver is maintained ON for a time corresponding to the phase difference. Subsequently, the capacitor voltage of the low-pass filter connected to this phase comparator is adjusted until the signal and comparator inputs are equal in both phase and frequency. At this stable point both p-and n-type output drivers remain OFF and thus the phase comparator output becomes an open circuit and holds the voltage on the capacitor of the low-pass filter constant. Moreover the signal at the "phase pulses" output is a high level which can be used for indicating a locked condition. Thus, for phase comparator II, no phase difference exists between signal and comparator input over the full VCO frequency range. More-over, the power dissipation due to the low-pass filter is reduced when this type of phase comparator is used because both the p-and n-type output drivers are OFF for most of the signal input cycle.

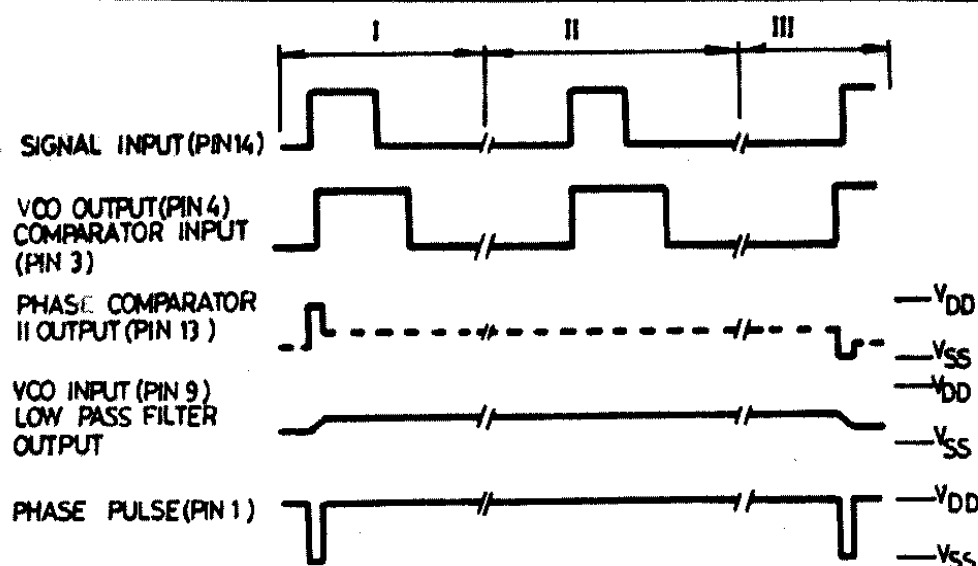
It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range, independent of the low-pass filter. With no signal present at the signal input, the VCO is adjusted to its lowest frequency for phase comparator II. Fig. (c) shows typical waveforms for a CMOS PLL employing phase comparator II in a locked condition.

Fig. (a) — Phase comparator I characteristics low-pass filter output

Fig. (b) — Typical waveforms for CMOS Phase Locked-Loop employing phase comparator I in locked condition of f_0 .

Fig. (c) — Typical waveforms for CMOS Phase-Locked-Loop employing phase comparator II in locked condition





NOTE: DASHED LINE IS AN OPEN-CIRCUIT CONDITION

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER		TEST CONDITIONS					VALUES						UNIT		
		V _I (V)	V _O (V)	I _O (μA)	V _{DD} (V)	T _{LOW}		25°C		T _{HIGH}					
						min.	max.	min.	typ	max.	min.	max.			
VCO SECTION															
V _{OH}	Output high voltage	0/ 5 0/10 0/15		< 1 < 1 < 1	5 10 15	4.95 9.95 14.95		4.95 9.95 14.95			4.95 9.95 14.95		V		
V _{OL}	Output low voltage	5 /0 10/0 15/0		< 1 < 1 < 1	5 10 15		0.05 0.05 0.05			0.05 0.05 0.05		0.05 0.05 0.05	V		
I _{OH}	Output drive current	G, H types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA	
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36			
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9			
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4			
		E, F types	0/ 5	2.5		5	-1.53		-1.36	-3.2		-1.1			
			0/ 5	4.6		5	-0.52		-0.44	-1		-0.36			
I _{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA	
			0/10	0.5		10	1.6		1.3	2.6		0.9			
			0/15	1.5		15	4.2		3.4	6.8		2.4			
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36			
			0/10	0.5		10	1.3		1.1	2.6		0.9			
			0/15	1.5		15	3.6		3.0	6.8		2.4			
I _{in} , I _h	Input leakage current	G, H types	0/18	Any input	18		±0.1		±10 ⁻⁵	±0.1		±1	μA		
		E, F types	0/15		15		±0.3		±10 ⁻⁵	±0.3		±1			

PARAMETER	TEST CONDITIONS				VALUES							UNIT
	V _I (V)	V _O (V)	I _{OL} (μA)	V _{DD} (V)	T _{LOW}		25°C			T _{HIGH}		
					min.	max.	min.	typ.	max.	min.	max.	

PHASE COMPARATOR SECTION

I _{DD} Total device current	G, H types	0/ 5 0/10 0/15 0/20			5 10 15 20		5 10 15 100			5 10 20 100		150 300 600 3000	μ A
	Pin 14=V _{SS} or V _{DD} Pin 5=V _{DD}	E, F types 0/ 5 0/10 0/15			5 10 15		20 40 80			30 60 100		300 600 1000	
V _{IH} —Input high voltage			0.5/4.5 1/9 1.5/13.5	< 1 < 1 < 1	5 10 15	3.5 7 11		3.5 7 11			3.5 7 11		V
V _{IL} —Input low voltage			4.5/0.5 9/1 13.5/1.5	< 1 < 1 < 1	5 10 15		1.5 3 4			1.5 3 4		1.5 3 4	V
I _{OH} —Output drive current	G, H types	0/ 5 0/ 5 0/10 0/15	2.5 4.6 9.5 13.5		5 5 10 15	-2 -0.64 -1.6 -4.2		-1.6 -0.51 -1.3 -3.4	-3.2 -1 -2.6 -6.8		-1.15 -0.36 -0.9 -2.4		μ A
	E, F types	0/ 5 0/ 5 0/10 0/15	2.5 4.6 9.5 13.5		5 5 10 15	-1.53 -0.52 -1.3 3.6		-1.36 -0.44 -1.1 -3.0	-3.2 -1 -2.6 6.8		-1.1 -0.36 -0.9 2.4		μ A
I _{OL} —Output sink current	G, H types	0/ 5 0/10 0/15	0.4 0.5 1.5		5 10 15	0.64 1.6 4.2		0.51 1.3 3.4	1 2.6 6.8		0.36 0.9 2.4		μ A
	E, F types	0/ 5 0/10 0/15	0.4 0.5 1.5		5 10 15	0.52 1.3 3.6		0.44 1.1 3.0	1 2.6 6.8		0.36 0.9 2.4		μ A
I _{IH} , I _{IL} —Input leakage current	G, H types	0/18	Any input		18		± 0.1		$\pm 10^{-5}$	± 0.1		± 1	μ A
	E, F types	0/15			15		± 0.3		$\pm 10^{-5}$	± 0.3		± 1	μ A
I _{OH} 3—state output	G, H types	0/18	0/18		18		± 0.4		$\pm 10^{-5}$	± 0.4		± 12	μ A
	E, F types	0/15	0/15		15		± 1.0		$\pm 10^{-5}$	± 1.0		± 7.5	μ A
C _I —Input capacitance			Any input						5	7.5			pF

* T_{LOW} = -55°C for G, H devices; -40°C for E, F devices.

* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V

2 V min. with V_{DD} = 10 V

2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A=25^\circ\text{C}$; $C_L=50\text{pF}$; $R_L=200\text{K}$; typical temperature coefficient for all V_{DD} values is $0.3\%/^\circ\text{C}$, all input rise and fall time = 20 ns).

PARAMETER	TEST CONDITIONS V_{DD} (V)			VALUES			UNIT	
				Min.	Typ.	Max.		
VCO SECTION								
P_D Operating power dissipation	$f_0=10\text{kHz}$ $R_2=\infty$ $C_1=50\text{pF}$	$R_1=1\text{M}\Omega$ 10 15	5	15 8.0 30.0	3.0 16.0 60.0	mW		
f_{max} Maximum frequency	$R_1=10\text{K}$ $R_2=\infty$ $V_{\text{COIN}}=V_{DD}$	$C_1=50\text{pF}$ 10 15	5	0.2 0.4 0.6	0.4 0.8 1.2	MHz		
	$R_1=5\text{K}$ $R_2=\infty$ $V_{\text{COIN}}=V_{DD}$	$C_1=50\text{pF}$ 10 15	5	0.3 0.6 1.0	0.6 1.2 2.0			
	Center frequency (f_0) and frequency range $f_{\text{max}}-f_{\text{min}}$			Programmable with external components R_1 , R_2 and C_1				
	Nonlinearity	$V_{\text{COIN}}=2.5\text{V}\pm 0.3$	$R_1=10\text{K}$	5	6		%	
$V_{\text{COIN}}=5\text{V}\pm 1$		$R_1=100\text{K}$	10	2				
$V_{\text{COIN}}=5\text{V}\pm 2.5$		$R_1=400\text{K}$	10	10				
$V_{\text{COIN}}=7.5\text{V}\pm 1.5$		$R_1=100\text{K}$	15	2				
$V_{\text{COIN}}=7.5\text{V}\pm 5$		$R_1=1\text{M}$	15	18				
V_{CO} Output duty cycle			5,10,15	50		%		
t_{THL} VCO output transition t_{TLH} time			5 10 15	100 50 40	200 100 80	ns		
Source follower output (demodulated output) offset voltage $V_{\text{COIN}}-V_{\text{DEM}}$	$R_S>10\text{k}$		5,10,15	3.0		V		
Source follower output (demodulated output) Nonlinearity	$V_{\text{COIN}}=2.5\text{V}\pm 0.3$	$R_S=100\text{K}$	5	1		%		
	$V_{\text{COIN}}=5\text{V}\pm 2.5$	$R_S=300\text{K}$	10	2				
	$V_{\text{COIN}}=7.5\text{V}\pm 5$	$R_S=500\text{K}$	15	3				
V_Z Zener diode voltage	$I_Z=50\mu\text{A}$				5.7 6.2 6.7	V		
R_Z Zener dynamic resistance	$I_Z=2\text{mA}$				100	Ω		

PHASE COMPARATOR SECTION

R14 Pin 14 (signal in) input resistance	5	0.5		
	10	0.1		MΩ
	15	0.05		
A.C. coupled signal input voltage sensitivity* (peak-to-peak)	5	1.2		V
	10	2.4		
	15	4.8		
t _{PHL} Propagation delay time High to low level Pins 14 to 13	5	225	450	ns
	10	100	200	
	15	65	130	
t _{PLH} Propagation delay time Low to high, level	5		350	ns
	10		150	
	15		100	
t _{PHZ} Propagation delay time 3-state High level to High impedance Pins 14 to 13	5		225	ns
	10		100	
	15		65	
t _{PLZ} Low level to high impedance	5		285	ns
	10		130	
	15		95	
t _r , t _f Input rise or fall time Comparator Pin 3	5		50	μs
	10		1	
	15		0.3	
Signal Pin 14	5		500	μs
	10		20	
	15		2.5	
t _{THL} Transition time t _{TLH}	5		100	ns
	10		50	
	15		40	

* For sine wave the frequency must be greater than 10 kHz for Phase Comparator 11

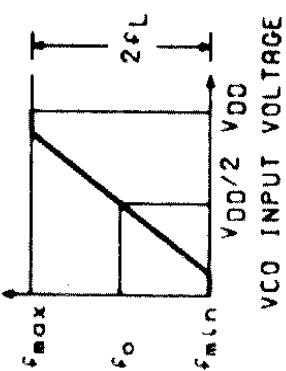
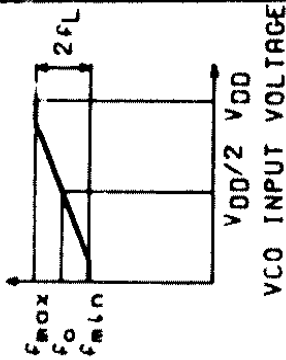
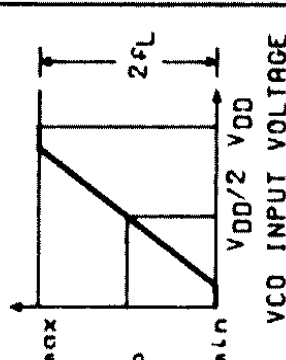
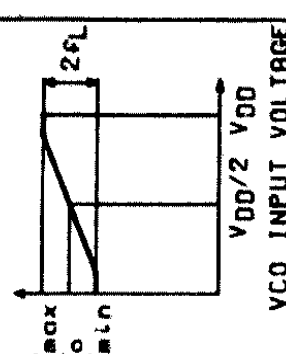
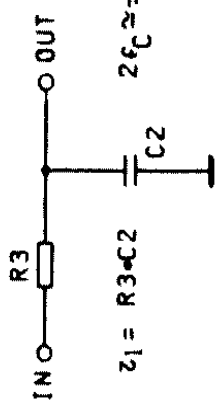
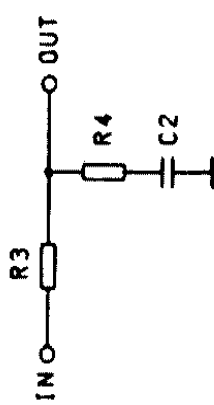
DESIGN INFORMATION

This information is a guide for approximating the values of external components for the 4046 in a Phase-Locked-Loop system. The selected external components must be within the following ranges.

$$5\text{ k} < R_1, R_2, R_S < 1\text{ M}$$

$$C_1 > 100\text{ pF at } V_{DD} > 5\text{ V}$$

$$C_1 > 50\text{ pF at } V_{DD} > 10\text{ V}$$

CHARACTERISTICS	USING PHASE COMPARATOR I		USING PHASE COMPARATOR II	
	VCO WITHOUT OFFSET R2 = ∞	VCO WITH OFFSET	VCO WITHOUT OFFSET R2 = ∞	VCO WITH OFFSET
VCO Frequency				
For No Signal Input	VCO in PLL systems will adjust to centre frequency, f0		VCO in PLL system will adjust to lowest operating frequency, fmin	
Frequency Lock Range, 2fL	2fL = full VCO frequency range 2fL = fmax - fmin			
Frequency Capture Range, 2fC	 $Z_1 = R3 \parallel C2$ $2f_C \approx \frac{1}{\pi} \sqrt{\frac{2\pi f_L}{Z_1}}$		$f_C = f_L$	
				
Loop Filter Component Selection				
Phase Angle between Signal and Comparator Centre Frequency	90° at centre frequency (f0), approximating 0° and 180° at ends of lock range (2fL)		Always 0° in lock	
Locks on Harmonics of Centre Frequency	Yes		No	
Signal Input Noise Rejection	High		Low	