



MMC 4035

4-STAGE PARALLEL IN/PARALLEL OUT SHIFT REGISTER

GENERAL DESCRIPTION

The MMC 4035 (G and H types) and MMC 4035 (E and F types) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package. The MMC 4035 integrated circuit is a four-stage clocked signal serial register with provision for synchronous PARALLEL inputs to each stage and SERIAL inputs to the first stage via JK logic. Register stages 2, 3, and 4 are coupled in a serial D flip-flop configuration when the register is in the serial mode (PARALLEL/SERIAL control low). Parallel entry into each register stage is permitted when the PARALLEL/SERIAL control is high. In the parallel or serial mode information is transferred on positive clock transition. When the TRUE/COMPLEMENT control is high, the true contents of the register are available at the output terminals. When the TRUE/COMPLEMENT control is low, the outputs are the complements of the data in the register. The TRUE/COMPLEMENT control functions asynchronously with respect to the CLOCK signal. JK input logic is provided on the first stage SERIAL input to minimize logic requirements particularly in counting and sequence-generation applications. With JK inputs connected together, the first stage becomes a D flip-flop. An asynchronous common RESET is also provided.

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FEATURES

- 4-stage clocked shift operation
- Synchronous parallel entry on all 4 stages
- JK inputs on first stage
- Asynchronous TRUE/COMPLEMENT control on all outputs
- Static flip-flop operation, master-slave configuration
- Buffered inputs and outputs
- High speed 12 MHz (typ.) at $V_{DD} = 10$ V.

ABSOLUTE MAXIMUM RATINGS

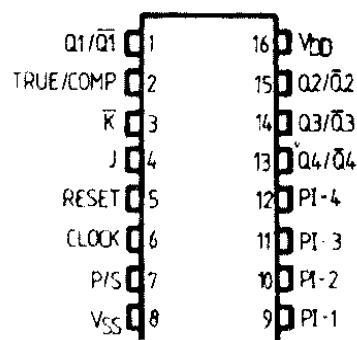
V_{DD}^*	Supply voltage: G and H types	-0.5 to 20	V
	E and F types	-0.5 to 18	V
V_i	Input voltage	-0.5 to $V_{DD}+0.5$	V
I_i	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_A = full package-temperature range	100	mW
T_A	Operating temperature: G and H types	-55 to 125	°C
	E and F types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

* All voltage values are referred to V_{SS} pin voltage

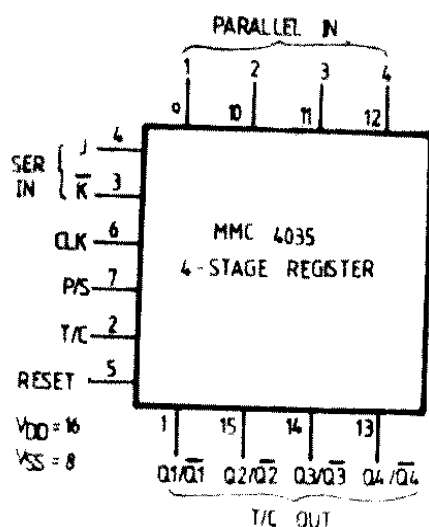
RECOMMENDED OPERATING CONDITIONS

V_{DD}^*	Supply voltage: G and H types	3 to 18	V
	E and F types	3 to 15	V
V_i	Input voltage	0 to V_{DD}	V
T_A	Operating temperature: G and H types	-55 to 125	°C
	E and F types	-40 to 85	°C

CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM

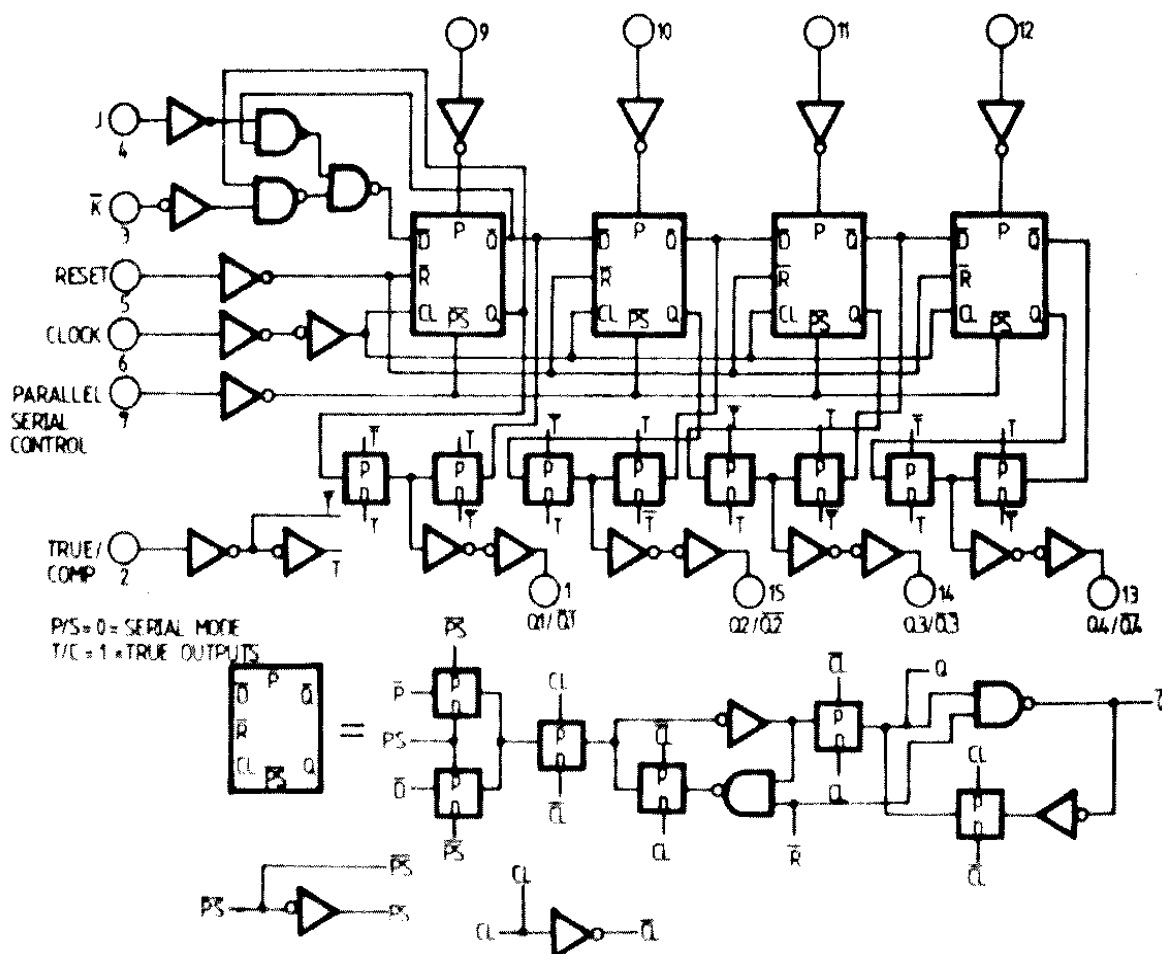


TRUTH TABLE

FIRST STAGE

CLOCK (ϕ)	t_{n-1} (INPUTS)				t_n (OUTPUTS)
	J	K	R	Q_{n-1}	Q_n
	0	X	0	0	0
	1	X	0	0	1
	X	0	0	1	0
	1	0	0	Q_{n-1}	$\bar{Q}_{n-1}$ TOGGLE MODE
	X	1	0	1	1
	X	X	0	Q_{n-1}	Q_{n-1}
X	X	X	1	X	0

LOGIC DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V _I (V)	V _O (V)	I _O (μ A)	V _{DD} (V)	T _{Low}		25°C			T _{High}		
							min.	max.	min.	typ.	max.	min.	max.	
I _L Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μ A	
		0/10			10		10		0.04	10		300		
		0/15			15		20		0.04	20		600		
		0/20			20		100		0.08	100		3000		
	E, F types	0/ 5			5		20		0.04	20		150		
		0/10			10		40		0.04	40		300		
		0/15			15		80		0.04	80		600		
V _{OH} Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V	
		0/10		< 1	10	9.95		9.95			9.95			
		0/15		< 1	15	14.95		14.95			14.95			
V _{OL} Output low voltage		5 / 0		< 1	5		0.05			0.05		0.05	V	
		10/ 0		< 1	10		0.05			0.05		0.05		
		15/ 0		< 1	15		0.05			0.05		0.05		
V _{IH} Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V	
			1/9	< 1	10	7		7			7			
			1.5/13.5	< 1	15	11		11			11			
V _{IL} Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V	
			9/1	< 1	10		3			3		3		
			13.5/1.5	< 1	15		4			4		4		
I _{OH} Output drive current	G, H types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA	
		0/ 5	4.6		5	-0.64		-0.51	-1		-0.36			
		0/10	9.5		10	-1.6		-1.3	-2.6		-0.9			
		0/15	13.5		15	-4.2		-3.4	-6.8		-2.4			
	E, F types	0/ 5	2.5		5	-1.53		-1.36	-3.2		-1.1			
		0/ 5	4.6		5	-0.52		-0.44	-1		-0.36			
		0/10	9.5		10	-1.3		-1.1	-2.6		-0.9			
		0/15	13.5		15	3.6		3.0	6.8		2.4			
I _{OL} Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA	
		0/10	0.5		10	1.6		1.3	2.6		0.9			
		0/15	1.5		15	4.2		3.4	6.8		2.4			
	E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36			
		0/10	0.5		10	1.3		1.1	2.6		0.9			
		0/15	1.5		15	3.6		3.0	6.8		2.4			
I _{IH} , I _{IL} Input leakage current	G, H types	0/18	Any input		18		± 0.1		$\pm 10^{-5}$	± 0.1		± 1	μ A	
	E, F types	0/15			15		± 0.3		$\pm 10^{-5}$	± 0.3		± 1		
C _i Input capacitance			Any input						5	7.5			pF	

* T_{LOW} = -55°C for G, H devices; -40°C for E, F devices.* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V2 V min. with V_{DD} = 10 V2.5 V min. with V_{DD} = 15 V

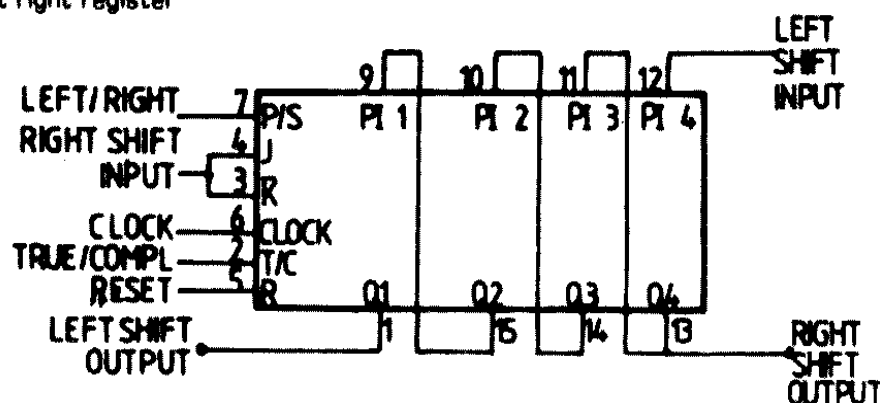
DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ kohm}$, typical temperature coefficient for all $V_{DD} = 0.3\%/^\circ\text{C}$ values, all input rise and fall time = 20 ns)

PARAMETER		TEST CONDITIONS V _{OD} (V)	VALUES			Unit
			min.	typ.	max.	
Clocked operation						
t _{PLH} t _{PHL}	Propagation delay time	5 10 15		250 100 75	500 200 150	ns
t _{THL} t _{TLH}	Transition time	5 10 15		100 50 40	200 100 80	ns
f _{CL}	Maximum clock input frequency	5 10 15	2 6 8	4 12 16		MHz
t _W	Clock pulse width	5 10 15		100 45 30	200 90 60	ns
t _r , t _f	Clock input rise or fall time	5 10 15		15 15 15		μs
t _{setup}	Data setup time J/K lines	5 10 15		110 40 30	220 80 60	ns
t _{setup}	Data setup time Parallel-In-Lines	5 10 15		70 25 20	140 50 40	ns
Reset operation						
t _{PLH} t _{PHL}	Propagation delay time	5 10 15		230 100 80	460 200 160	ns
t _W	Reset pulse width	5 10 15		125 55 40	250 110 40	ns

TYPICAL APPLICATIONS

Shift left/shift right register



The logic diagram illustrates the internal structure of a 4-bit parallel adder. It features four input lines labeled Q1, Q2, Q3, and Q4. The circuit uses a combination of NAND, NOR, and NOT gates to generate five output signals: P/S, CARRY FORWARD, PI-2, PI-3, and PI-4. The logic for each output is as follows:

- P/S:** Generated by a NOR gate with inputs from Q2 and Q3.
- CARRY FORWARD:** Generated by a NOR gate with inputs from Q1 and Q2.
- PI-2:** Generated by a NOT gate with input from Q2.
- PI-3:** Generated by a NOR gate with inputs from Q1 and Q2, followed by a NOT gate.
- PI-4:** Generated by a NOT gate with input from Q1.

The diagram shows an MMC 4035 4-stage register with inputs P/S, T/C, J, K, R and parallel inputs PI-1 to PI-4. The outputs are Q1, Q2, Q3, and Q4. The circuit uses four 4002 inverters to generate a 'CONTROL' signal. A 4030 NAND gate is also present at the bottom of the circuit.

State sequences

Using a control line (E) two different state sequences can be generated. For example, suppose the following two sequences are desired on command (control line).

Control = E = 0

	Q ₁	Q ₂	Q ₃	Q ₄		Q ₁	Q ₂	Q ₃	Q ₄
	A	B	C	D		A	B	C	D
0	0	0	0	0	15	1	1	1	1
1	1	0	0	0	14	0	0	1	1
2	0	1	0	0	13	1	0	1	1
5	1	0	1	0	10	0	1	0	1
10	0	1	0	1	5	1	0	1	0
4	0	0	1	0	11	1	1	0	1
9	1	0	0	1	6	0	1	1	0
3	1	1	0	0	12	0	0	1	1
6	0	1	1	0	9	1	0	0	1
13	1	0	1	1	2	0	1	0	0
11	1	1	0	1	4	0	0	1	0
7	1	1	1	0	8	0	0	0	1
14	0	1	1	1	1	1	0	0	0
12	0	0	1	1	3	1	1	0	0
8	0	0	0	1	7	1	1	1	0