



MMC 4067 MMC4097

ANALOG MULTIPLEXERS/DEMULTIPLEXERS: MMC 4067: SINGLE 16-CHANNEL MMC 4097: DIFFERENTIAL 8-CHANNEL

GENERAL DESCRIPTION

The MMC 4067, MMC 4097 are monolithic integrated circuits, available in 24-lead dual-in-line plastic package.

The MMC 4067, MMC 4097 analog multiplexers/demultiplexers are digitally controlled analog switches having low ON impedance, low OFF leakage current, and internal address decoding. In addition, the ON resistance is relatively constant over the full input-signal range.

The MMC 4067 is a 16-channel multiplexer with four binary control inputs A, B, C, D, and an inhibit input, arranged so that any combination of the inputs selects one switch.

The MMC 4097 is a differential 8-channel multiplexer having three binary control inputs A, B, C, and an inhibit input. The inputs permit selection of one of eight pairs of switches. A logic "1" present at the inhibit input turns all channels off.

FEATURES

- Low on resistance: 125Ω (typ.) over 15 V_{p-p} signal-input range for $V_{DD}V_{SS} = 15\text{ V}$
- High off resistance: channel leakage of $\pm 10\text{ pA}$ (typ.) for $V_{DD}V_{SS} = 15\text{ V}$
- Matched switch characteristics: $\Delta R_{on} = 5\Omega$ (typ.) for $V_{DD}V_{SS} = 15\text{ V}$
- Very low quiescent power dissipation under all digital-control input and supply conditions: $0.2\text{ }\mu\text{W}$ (typ.) for $V_{DD}V_{SS} = 10\text{ V}$
- Binary address decoding on chip

ABSOLUTE MAXIMUM RATINGS

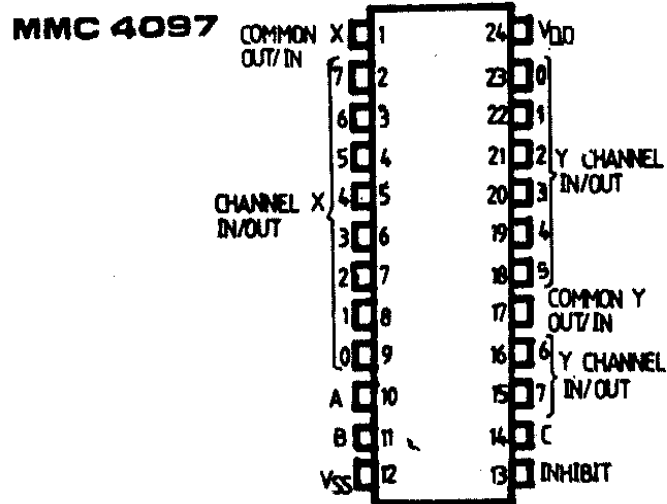
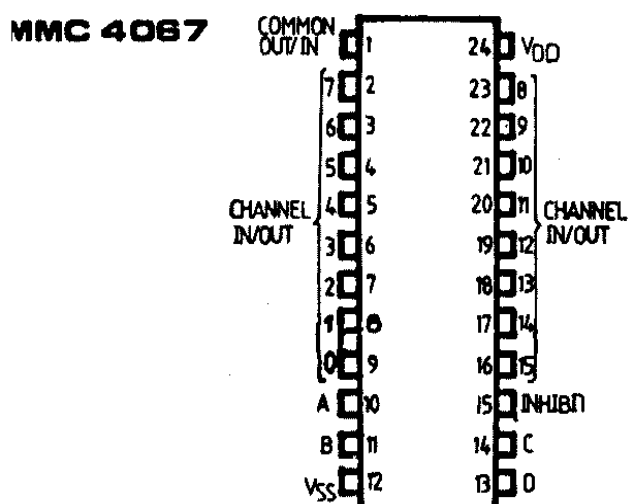
V_{DD}^*	Supply voltage: G and H types	-0.5 to	20	V
	E and F types	-0.5 to	18	V
V_i	Input voltage	-0.5 to	$V_{DD}+0.5$	V
I_i	DC input current (any one input)		± 10	mA
P_{tot}	Total power dissipation (per package)		200	mW
	Dissipation per output transistor for $T_A =$ full package-temperature range		100	mW
T_A	Operating temperature: G and H types	-55 to	125	$^{\circ}\text{C}$
	E and F types	-40 to	85	$^{\circ}\text{C}$
T_{stg}	Storage temperature	-65 to	150	$^{\circ}\text{C}$

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}^*	Supply voltage: G and H types	3 to	18	V
	E and F types	3 to	15	V
V_i	Input voltage	0 to	V_{DD}	V
T_A	Operating temperature: G and H types	-55 to	125	$^{\circ}\text{C}$
	E and F types	-40 to	85	$^{\circ}\text{C}$

CONNECTION DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS						VALUES					UNIT
			V _{IS} (V)	V _{EE} (V)	V _{SS} (V)	V _{DD} (V)	T _{LOW} (●)		25°C			T _{HIGH} (●)		
							min.	max.	min.	typ	max.	min.	max.	
I _L	Quiescent device current	G and H types				5		5		0.04	5		150	μA
						10		10		0.04	10		300	
						15		20		0.04	20		600	
						20		100		0.08	100		3000	
	E and F types				5		20		0.04	20		150		
					10		40		0.04	40		300		
					15		80		0.04	80		600		

Switch

ON Resistance	G and H types	0 ≤ V _I ≤ V _{DD}	0	0	5		800		470	1050		1300	Ω
					10		310		180	400		580	
					15		200		125	240		320	
	E and F types	0 ≤ V _I ≤ V _{DD}	0	0	5		850		470	1050		1200	
					10		330		180	400		520	Ω
					15		210		125	240		300	
ΔON Resistance (Between any 2 channels)			0	0	5				10				Ω
					10				10				
					15				5				
OFF(●)Any leakage current	Any channel OFF	G and H types		0	0	18		100	+/-0.1	100		1000	nA
	All channels OFF (common OUT/IN)	G and H types		0	0	18		100	+/-0.1	100		1000	nA
	Any channel OFF	E and F types		0	0	15		300	+/-0.1	300		1000	nA
	All channels OFF (common OUT/IN)	E and F types		0	0	15		300	+/-0.1	300		1000	nA
C	Input								5				
Capacitance	Output 4067								55				pF
	Output 4097								35				
	Feedthrough			-5	5				0.2				

Control (Address or Inhibit)

V _{IL} Input low voltage	V _{DD} thru 1 kΩ	V _{EE} V _{IS} R _I 1K to V _{SS} I _{IS} 2μA (on all OFF channels)	5		15		15		15		15	V
			10		3		3		3		3	
			15		4		4		4		4	
V _{IH} Input high voltage			5	3.5		35				3.5		
			10	7		7				7		
			15	11		11				11		
I _{IN} I _L Input leakage current	G and H types	V _I = 0/18	18		±0.1		±10 ⁻³	±0.1		±1		μA
	E and F types	V _I = 0/15	15		±0.3		±10 ⁻³	±0.3		±1		μA

PARAMETER	TEST CONDITIONS				VALUES						UNIT	
	V _I (V)	V _O (V)	I _O (μA)	V _{DD} (V)	T _{LOW} *		25°C			T _{HIGH} *		
					min.	max.	min.	typ	max.	min.		max.
CI Input capacitance	Any address or inhibit input							5	7.5			pF

(●) Determined by minimum feasible leakage measurement for automatic testing

* $T_{LOW} = -55^\circ\text{C}$ for G and H types; -40°C for E and F types

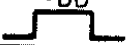
$T_{HIGH} = +125^\circ\text{C}$ for G and H types; $+85^\circ\text{C}$ for E and F types

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_{amb} = 25^\circ\text{C}$, $C_L = 50$ pF, all input square wave rise and fall times = 20 ns)

PARAMETER	TEST CONDITIONS							VALUES		UNIT	
	V_C (V)	R_L (k Ω)	f_i (kHz)	V_i (V)	V_{SS} (V)	V_{DD} (V)		TYP.	MAX.		
Switch											
t_{pd} Propagation delay time (Signal input to output)	$= V_{DD}$	200			0	5 10 15		30 15 11	60 30 20	ns	
Frequency response channel „ON“ (Sine wave input) at 20 Log(V_O/V_i) = -3dB	$= V_{DD}$	1		5(●)	0	10	V_O at common 4067 OUT/IN	14 20		MHz	
							V_O at any channel	60		MHz	
Feedthrough (all channels OFF) at 20 Log(V_O/V_i) = -40dB	$= V_{SS}$	1		5(●)	0	10	V_O at common 4067 OUT/IN	20 12		MHz	
							V_O at any channel	8			
Frequency signal crosstalk at 20 Log($V_{o(B)}/V_{i(A)}$) = -40 dB	$V_{C(A)} = V_{DD}$ $V_{C(B)} = V_{SS}$	1		5(●)	0	10	Between any (A and B) channels	1		MHz	
							Between sections (A and B) 4097 only	Measured on common	10		
								Measured on any channel	18		
Sine wave distortion $f_{is} = 1$ kHz sine wave	5	10	1	2(●)	0	5		0.3		%	
	10	10	1	3(●)	0	10		0.2			
	15	10	1	5(●)	0	15		0.12			

Control (Address or inhibit)

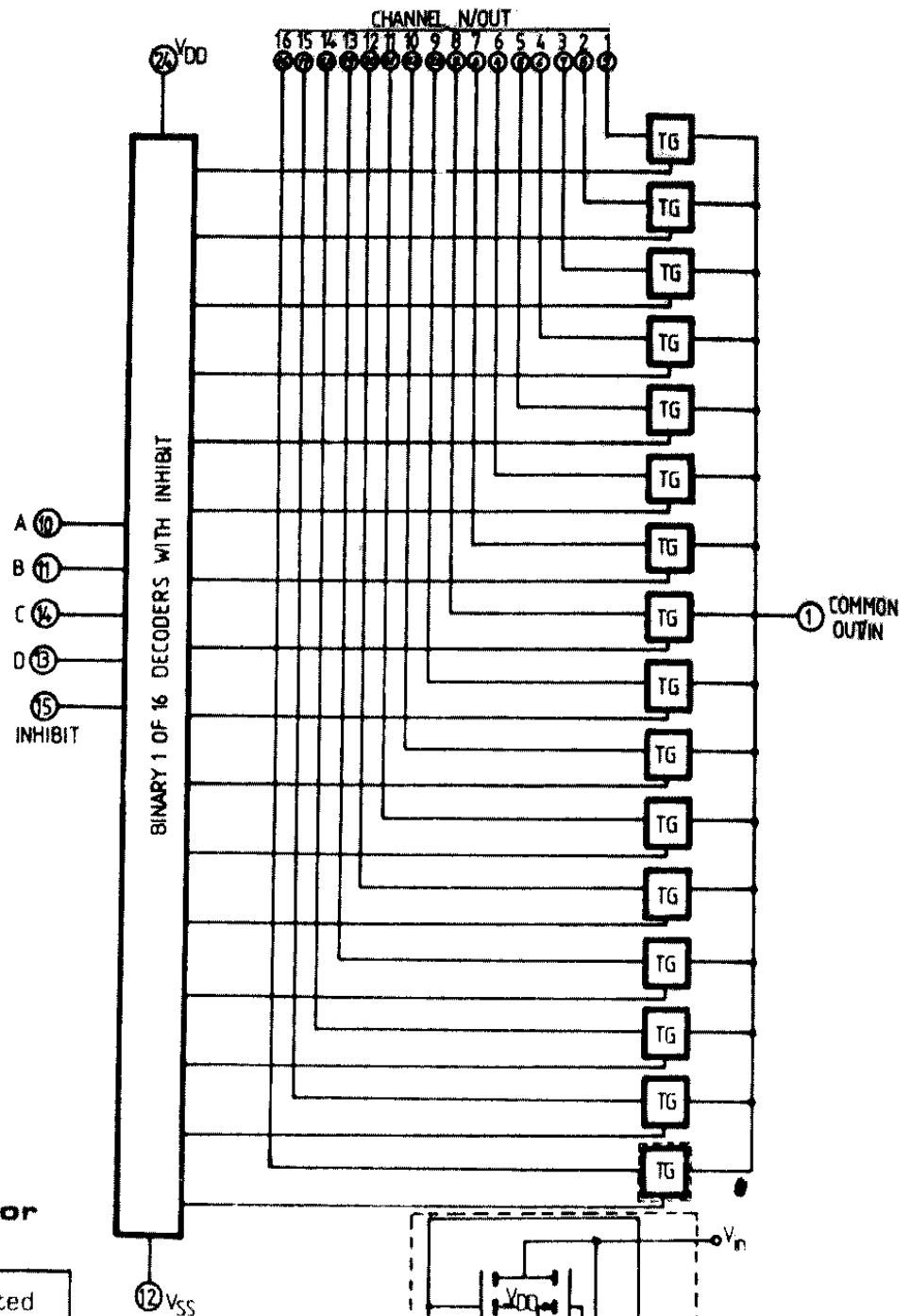
Propagation delay time: address or inhibit to signal OUT (channel turning ON)	 V_{DD}	10			0 0 0	5 10 15		325 135 95	650 270 190	ns
Propagation delay time: address or inhibit to signal OUT (channel turning OFF)	 V_{DD}	0.3			0 0 0	5 10 15		220 90 65	440 180 130	ns
Address or inhibit to signal crosstalk	 V_{DD}	10*			0	10		75		mV peak

* Both ends of channel

(●) peak to peak voltage symmetrical about $(V_{DD} - V_{SS})/2$

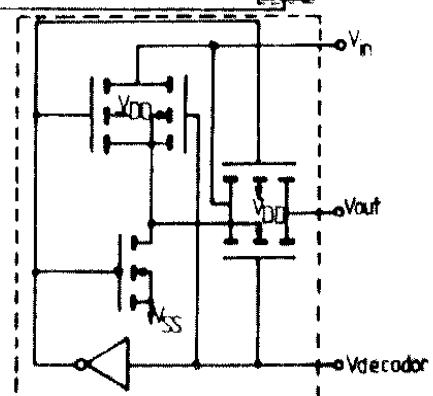
LOGIC DIAGRAM

MMC 4067

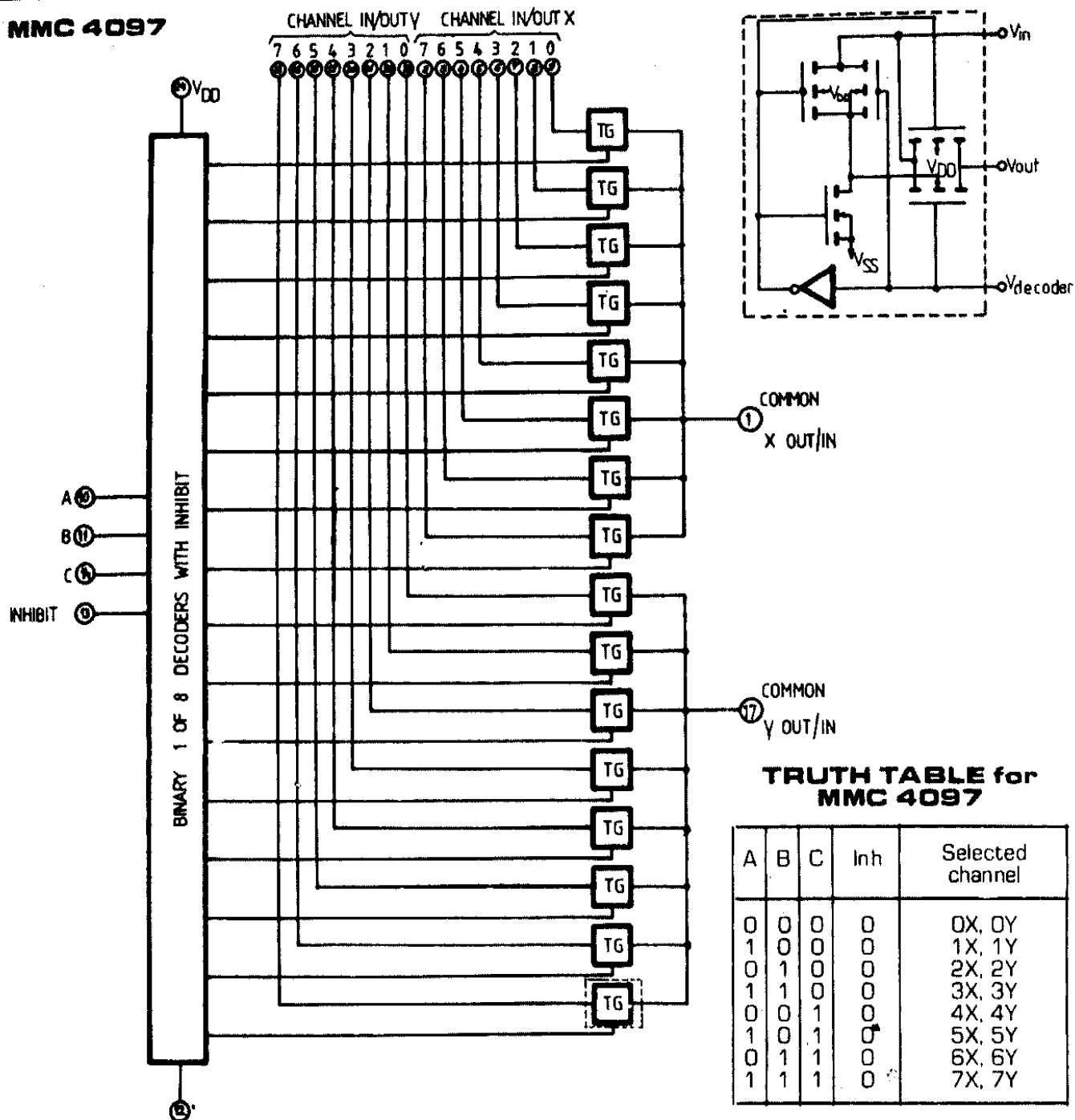


TRUTH TABLE for
MMC 4067

A	B	C	D	Inh	Selected channel
X	X	X	X	1	None
0	1	0	0	0	0
0	1	0	0	0	1
0	1	0	0	0	2
0	1	0	0	0	3
0	1	0	1	0	4
0	1	0	1	0	5
0	1	1	0	0	6
0	1	1	0	0	7
0	0	0	1	0	8
0	1	0	1	0	9
0	1	0	1	0	10
0	1	1	1	0	11
0	1	1	1	0	12
0	1	1	1	0	13
0	1	1	1	0	14
0	1	1	1	0	15



MMC 4097



APPLICATIONS INFORMATION

In applications where separate power sources are used to drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load). This provision avoids permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from the MMC 4067 or MMC 4097.

When switching from one address to another, some of the ON periods of the channels of the multiplexers will overlap momentarily, which may be objectionable in certain applications. Also when a channel is turned on or off by an address input, there is a momentary conductive path from the channel to V_{SS} , which will dump some charge from any capacitor connected to the input or output of the channel. The inhibit input turning on a channel will similarly dump some charge to V_{SS} . The amount of charge dumped is mostly a function of the signal level above V_{SS} . Typically, at $V_{DD}/V_{SS} = 10V$, a 100 pF capacitor connected to the input or output of the channel will lose 3-4% of its voltage at the moment the channel turns on or off. This loss of voltage is essentially independent of the address or inhibit signal transition time, if the transition time is less than 1-2 μs . When the inhibit signal turns a channel off, there is no charge dumping to V_{SS} . Rather, there is a slight rise in the channel voltage level (65 mV typ.) due to capacitive coupling from inhibit input to channel input or output. Address inputs also couple some voltage steps onto the channel signal levels.

In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8 volt.