



MMC 4060

14-STAGE RIPPLE-CARRY BINARY COUNTER/ DIVIDER AND OSCILLATOR

GENERAL DESCRIPTION

The MMC 4060 is a monolithic i.c. processed in standard Al-gate CMOS technology. This device consists of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC or crystal oscillator circuits. All counter stages are master-slave flip-flops. The state of the counter is advanced one step in binary order on the negative transition of ϕ_I (and ϕ_0). A high level on the RESET line resets the counter to the all 0's state and disables the oscillator. Schmitt trigger action on the clock line permits unlimited clock rise and fall times. All inputs and outputs are fully buffered.

FEATURES

- Medium-speed operation
- Fully static operation
- Buffered inputs and outputs
- Common reset

ABSOLUTE MAXIMUM RATINGS

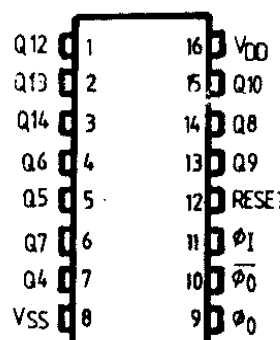
V_{DD}^*	Supply voltage: G and H types	-0.5 to	20	V
	E and F types	-0.5 to	18	V
V_I	Input voltage	-0.5 to	$V_{DD}+0.5$	V
I_I	DC input current (any one input)		± 10	mA
P_{tot}	Total power dissipation (per package)		200	mW
	Dissipation per output transistor for T_A = full package-temperature range		100	mW
T_A	Operating temperature :			
	G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C
T_{stg}	Storage temperature	-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}^*	Supply voltage: G and H types	3 to	18	V
	E and F types	3 to	15	V
V_I	Input voltage	0 to	V_{DD}	V
T_A	Operating temperature :			
	G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C

CONNECTION DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES						UNIT	
			V _I (V)	V _O (V)	I _{HI} (μ A)	V _{OH} (V)	T _{LOW}		25°C			T _{HIGH}		
							min.	max.	min.	typ	max.	min.		max.
I _I	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μ A
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
		0/15			15		80		0.04	80		600		
V _{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V _{OL}	Output low voltage		5 / 0		< 1	5		0.05			0.05		0.05	V
			10/ 0		< 1	10		0.05			0.05		0.05	
			15/ 0		< 1	15		0.05			0.05		0.05	
V _{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				15/13.5	< 1	15	11		11			11		
V _{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I _{OA}	Output drive current	G, H types	0/ 5	25		5	-2		1.6	32		-1.15		mA
			0/ 5	46		5	-0.64		-0.51	-1		-0.36		
			0/10	95		10	-1.6		-1.3	-2.6		-0.9		
			0/15	135		15	-4.2		-3.4	-6.8		-2.4		
		E, F types	0/ 5	25		5	-1.53		1.36	32		-1.1		
			0/ 5	46		5	-0.52		-0.44	-1		-0.36		
			0/10	95		10	-1.3		1.1	2.6		-0.9		
			0/15	135		15	-3.6		-3.0	-6.8		-2.4		
I _{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36	mA	
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
	E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36			
		0/10	0.5		10	1.3		1.1	2.6		0.9			
		0/15	1.5		15	3.6		3.0	6.8		2.4			
I _{IK} , I _{IL}	Input leakage current	G, H types	0/18	Any input	18		± 0.1		$\pm 10^{-5}$	± 0.1		± 1	μ A	
		E, F types	0/15		15		± 0.3		$\pm 10^{-5}$	± 0.3		± 1		
C _i	Input capacitance			Any input					5	75			pF	

* T_{LOW} -55°C for G, H devices; -40°C for E, F devices* T_{HIGH} +125°C for G, H devices; +85°C for E, F devices

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V2 V min. with V_{DD} = 10 V2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ kohm}$, typical temperature coefficient for all $V_{DD} = 0.3\%/^\circ\text{C}$ values, all input rise and fall time = 20 ns)

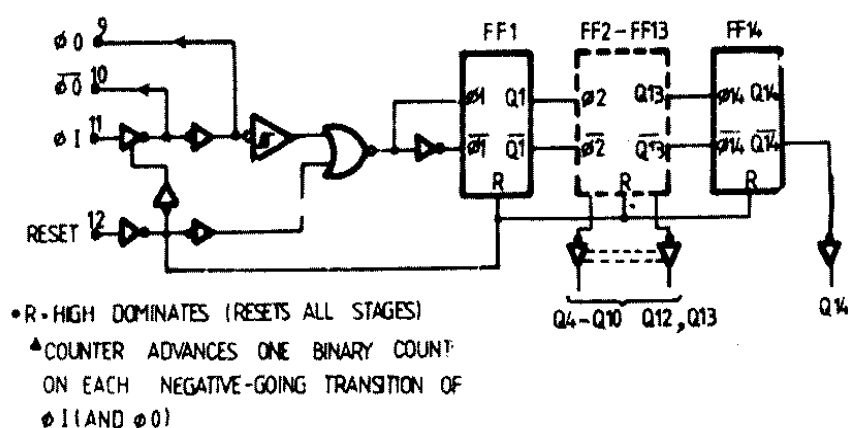
PARAMETER		TEST CONDITIONS		VALUES			UNIT
			V _{DD} (V)	Min.	Typ.	Max.	
Input-pulse operation							
t _{PLH} Propagation delay time t _{PHL} (Q to Q4 Out)		5		370	740	ns	
		10		150	300		
		15		100	200		
t _{PLH} Propagation delay time t _{PHL} (Qn to Q _{n+1})		5		100	200	ns	
		10		50	100		
		15		40	80		
t _{TLH} Transition time t _{THL}		5		100	200	ns	
		10		50	100		
		15		40	80		
t _W Input pulse width	f = 100 kHz	5		50	100	ns	
		10		20	40		
		15		15	30		
t _r t _f Input rise and fall time		5	Unlimited			μs	
		10					
		15					
f _{max} Maximum clock input frequency		5	3.5	7		MHz	
		10	8	16			
		15	12	24			
Reset operation							
t _{PLH} Propagation delay time		5		180	360	ns	
		10		80	160		
		15		50	100		
t _W Reset pulse width		5		60	120	ns	
		10		30	60		
		15		20	40		
RC operation							
Variation of frequency (Unit-to-Unit)	C _x = 200 pF	5	18	21.5	25	kHz	
	R _S = 560 kΩ	10	20	23	26		
	R _x = 50 kΩ	15	21.1	24	27		
Variation of frequency with voltage (Same Unit)	C _x = 200 pF	5V to 10 V	—	—	2	kHz	
	R _S = 560 kΩ	10 V to 15 V	—	—	1		
	R _x = 50 kΩ						
R _x max	C _x = 10 μF	5	—	—	20	MΩ	
	= 50 μF	10	—	—	20		
	= 10 μF	15	—	—	10		

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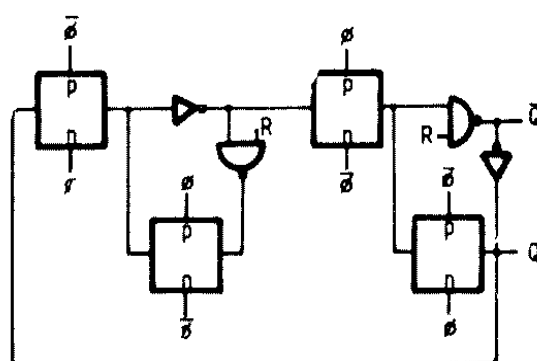
PARAMETER	TEST CONDITIONS	VALUES			UNIT	
		$V_{DD}(V)$	Min.	Typ.		Max.
D_x max	$R_x = 500\text{ k}\Omega$	5	—	—	1000	μF
	$= 300\text{ k}\Omega$	10	—	—	50	
	$= 300\text{ k}\Omega$	15	—	—	50	
Maximum Oscillator Frequency*	$R_x = 5\text{ k}\Omega$	10	530	650	810	kHz
	$C_x = 15\text{ pF}$	15	690	800	940	

* RC oscillator applications are not recommended at supply voltages below 7 V for $R_x = 50 \text{ k}\Omega$

LOGIC DIAGRAM



Detail of typical flip-flop stage



APPLICATIONS

