OKI Semiconductor

This version: Mar. 1998

MSM51V16160D/DSL

1,048,576-Word × 16-Bit DYNAMIC RAM : FAST PAGE MODE TYPE

DESCRIPTION

The MSM51V16160D/DSL is a 1,048,576-word × 16-bit dynamic RAM fabricated in Oki's silicon-gate CMOS technology. The MSM51V16160D/DSL achieves high integration, high-speed operation, and low-power consumption because Oki manufactures the device in a quadruple-layer polysilicon/double-layer metal CMOS process. The MSM51V16160D/DSL is available in a 42-pin plastic SOJ or 50/44-pin plastic TSOP. The MSM51V16160DSL (the self-refresh version) is specially designed for lower-power applications.
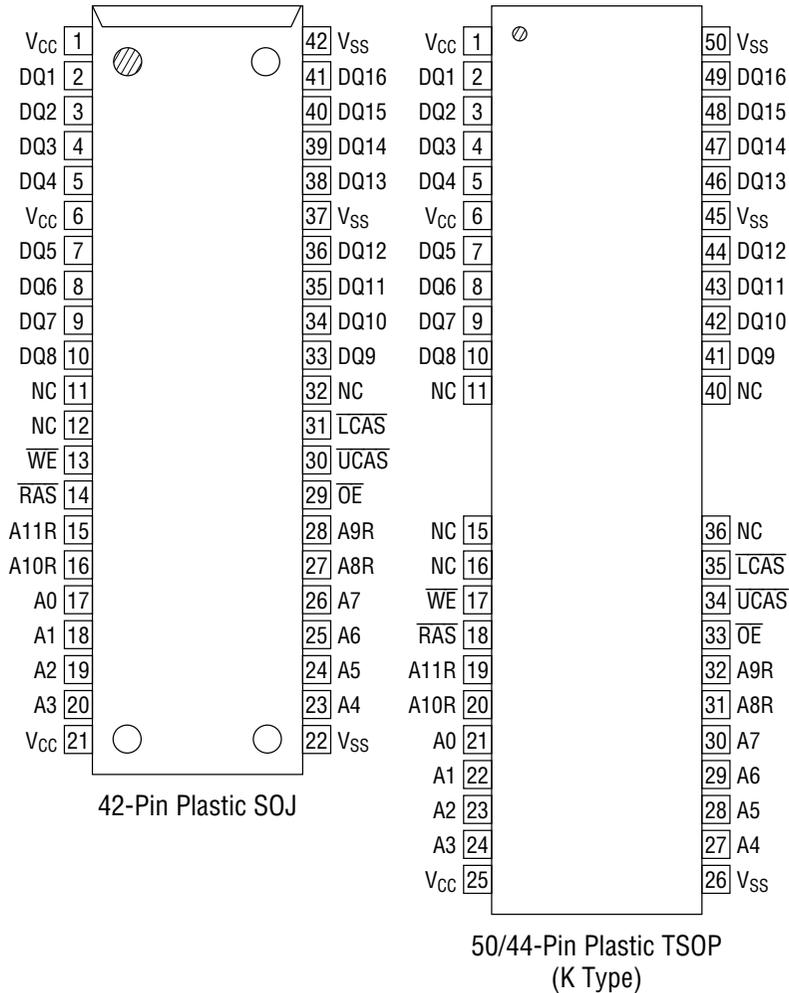
FEATURES

- 1,048,576-word × 16-bit configuration
- Single 3.3 V power supply, ±0.3 V tolerance
- Input   : LVTTL compatible, low input capacitance
- Output : LVTTL compatible, 3-state
- Refresh : 4096 cycles/64 ms, 4096 cycles/128 ms (SL version)
- Fast page mode, read modify write capability
- $\overline{CAS}$ before $\overline{RAS}$ refresh, hidden refresh, $\overline{RAS}$-only refresh capability
- $\overline{CAS}$ before $\overline{RAS}$ self-refresh capability (SL version)
- Package options:
  42-pin 400 mil plastic SOJ   (SOJ42-P-400-1.27)   (Product : MSM51V16160D/DSL-xxJS)
  50/44-pin 400 mil plastic TSOP   (TSOPII50/44-P-400-0.80-K) (Product : MSM51V16160D/DSL-xxTS-K)
  xx indicates speed rank.

PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}	t_{OEA}		Operating (Max.)	Standby (Max.)
MSM51V16160D/DSL-50	50 ns	25 ns	13 ns	13 ns	90 ns	270 mW	1.8 mW/ 0.72 mW (SL version)
MSM51V16160D/DSL-60	60 ns	30 ns	15 ns	15 ns	110 ns	234 mW	
MSM51V16160D/DSL-70	70 ns	35 ns	20 ns	20 ns	130 ns	216 mW	

PIN CONFIGURATION (TOP VIEW)

42-Pin Plastic SOJ

V_{CC}	1	42	V_{SS}
DQ1	2	41	DQ16
DQ2	3	40	DQ15
DQ3	4	39	DQ14
DQ4	5	38	DQ13
V_{CC}	6	37	V_{SS}
DQ5	7	36	DQ12
DQ6	8	35	DQ11
DQ7	9	34	DQ10
DQ8	10	33	DQ9
NC	11	32	NC
NC	12	31	$\overline{LCAS}$
$\overline{WE}$	13	30	$\overline{UCAS}$
$\overline{RAS}$	14	29	$\overline{OE}$
A11R	15	28	A9R
A10R	16	27	A8R
A0	17	26	A7
A1	18	25	A6
A2	19	24	A5
A3	20	23	A4
V_{CC}	21	22	V_{SS}

42-Pin Plastic SOJ

50/44-Pin Plastic TSOP (K Type)

V_{CC}	1	50	V_{SS}
DQ1	2	49	DQ16
DQ2	3	48	DQ15
DQ3	4	47	DQ14
DQ4	5	46	DQ13
V_{CC}	6	45	V_{SS}
DQ5	7	44	DQ12
DQ6	8	43	DQ11
DQ7	9	42	DQ10
DQ8	10	41	DQ9
NC	11	40	NC
NC	15	36	NC
NC	16	35	$\overline{LCAS}$
$\overline{WE}$	17	34	$\overline{UCAS}$
$\overline{RAS}$	18	33	$\overline{OE}$
A11R	19	32	A9R
A10R	20	31	A8R
A0	21	30	A7
A1	22	29	A6
A2	23	28	A5
A3	24	27	A4
V_{CC}	25	26	V_{SS}

50/44-Pin Plastic TSOP
(K Type)

Pin Name	Function
A0 - A7, A8R - A11R	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{LCAS}$	Lower Byte Column Address Strobe
$\overline{UCAS}$	Upper Byte Column Address Strobe
DQ1 - DQ16	Data Input/Data Output
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply (3.3 V)
V_{SS}	Ground (0 V)
NC	No Connection

Note :   The same power supply voltage must be provided to every V_{CC} pin, and the same GND voltage level must be provided to every V_{SS} pin.

BLOCK DIAGRAM
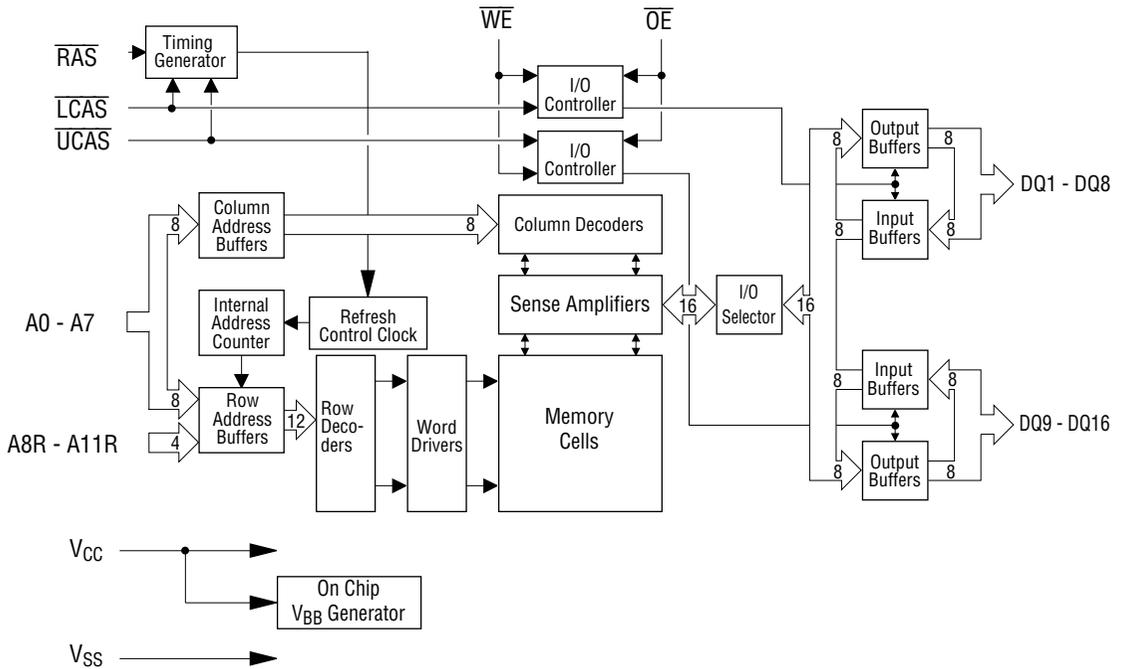
FUNCTION TABLE

Input Pin					DQ Pin		Function Mode
$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	DQ1 - DQ8	DQ9 - DQ16	
H	*	*	*	*	High-Z	High-Z	Standby
L	H	H	*	*	High-Z	High-Z	Refresh
L	L	H	H	L	D_{OUT}	High-Z	Lower Byte Read
L	H	L	H	L	High-Z	D_{OUT}	Upper Byte Read
L	L	L	H	L	D_{OUT}	D_{OUT}	Word Read
L	L	H	L	H	D_{IN}	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	D_{IN}	Upper Byte Write
L	L	L	L	H	D_{IN}	D_{IN}	Word Write
L	L	L	H	H	High-Z	High-Z	—

*: "H" or "L"

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−0.5 to 4.6	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_D*	1	W
Operating Temperature	T_{opr}	0 to 70	°C
Storage Temperature	T_{stg}	−55 to 150	°C

*: Ta = 25°C

Recommended Operating Conditions

(Ta = 0°C to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	3.0	3.3	3.6	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	−0.3	—	0.8	V

Capacitance

(V_{CC} = 3.3 V ±0.3 V, Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A7, A8R - A11R)	C_{IN1}	—	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{WE}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ1 - DQ16)	$C_{I/O}$	—	7	pF

DC Characteristics

(V$_{CC}$ = 3.3 V ±0.3 V, Ta = 0°C to 70°C)

Parameter	Symbol	Condition	MSM51V16160 D/DSL-50		MSM51V16160 D/DSL-60		MSM51V16160 D/DSL-70		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	V$_{OH}$	I$_{OH}$ = −2.0 mA	2.4	V$_{CC}$	2.4	V$_{CC}$	2.4	V$_{CC}$	V	
Output Low Voltage	V$_{OL}$	I$_{OL}$ = 2.0 mA	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	I$_{LI}$	0 V ≤ V$_I$ ≤ V$_{CC}$ + 0.3 V; All other pins not under test = 0 V	−10	10	−10	10	−10	10	µA	
Output Leakage Current	I$_{LO}$	DQ disable 0 V ≤ V$_O$ ≤ V$_{CC}$	−10	10	−10	10	−10	10	µA	
Average Power Supply Current (Operating)	I$_{CC1}$	$\overline{RAS}$, $\overline{CAS}$ cycling, t$_{RC}$ = Min.	—	75	—	65	—	60	mA	1, 2
Power Supply Current (Standby)	I$_{CC2}$	$\overline{RAS}$, $\overline{CAS}$ = V$_{IH}$	—	2	—	2	—	2	mA	1
		$\overline{RAS}$, $\overline{CAS}$	—	0.5	—	0.5	—	0.5	mA	
		≥ V$_{CC}$ −0.2 V	—	200	—	200	—	200	µA	1, 5
Average Power Supply Current ($\overline{RAS}$-only Refresh)	I$_{CC3}$	$\overline{RAS}$ cycling, $\overline{CAS}$ = V$_{IH}$, t$_{RC}$ = Min.	—	75	—	65	—	60	mA	1, 2
Power Supply Current (Standby)	I$_{CC5}$	$\overline{RAS}$ = V$_{IH}$, $\overline{CAS}$ = V$_{IL}$, DQ = enable	—	5	—	5	—	5	mA	1
Average Power Supply Current ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	I$_{CC6}$	$\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$	—	75	—	65	—	60	mA	1, 2
Average Power Supply Current (Fast Page Mode)	I$_{CC7}$	$\overline{RAS}$ = V$_{IL}$, $\overline{CAS}$ cycling, t$_{PC}$ = Min.	—	70	—	65	—	60	mA	1, 3
Average Power Supply Current (Battery Backup)	I$_{CC10}$	t$_{RC}$ = 31.3 µs, $\overline{CAS}$ before $\overline{RAS}$, t$_{RAS}$ ≤ 1 µs	—	400	—	400	—	400	µA	1, 4, 5
Average Power Supply Current ($\overline{CAS}$ before $\overline{RAS}$ Self-Refresh)	I$_{CCS}$	$\overline{RAS}$ ≤ 0.2 V, $\overline{CAS}$ ≤ 0.2 V	—	300	—	300	—	300	µA	1, 5

Notes : 1. I$_{CC}$ Max. is specified as I$_{CC}$ for output open condition.
2. The address can be changed once or less while $\overline{RAS}$ = V$_{IL}$.
3. The address can be changed once or less while $\overline{CAS}$ = V$_{IH}$.
4. V$_{CC}$ − 0.2 V ≤ V$_{IH}$ ≤ V$_{CC}$ + 0.3 V, −0.3 V ≤ V$_{IL}$ ≤ 0.2 V.
5. SL version.

AC Characteristics (1/2)

(V_{CC} = 3.3 V ±0.3 V, Ta = 0°C to 70°C) Note 1, 2, 3

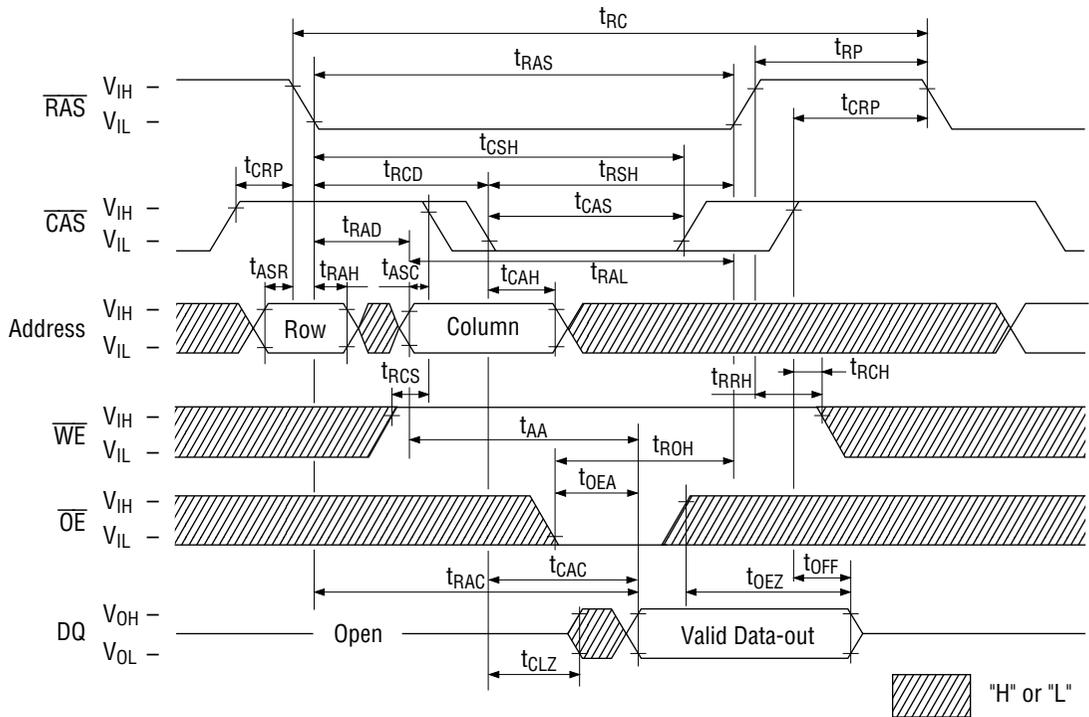| Parameter	Symbol	MSM51V16160 D/DSL-50		MSM51V16160 D/DSL-60		MSM51V16160 D/DSL-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	90	—	110	—	130	—	ns	
Read Modify Write Cycle Time	t_{RWC}	131	—	155	—	185	—	ns	
Fast Page Mode Cycle Time	t_{PC}	35	—	40	—	45	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t_{PRWC}	76	—	85	—	100	—	ns	
Access Time from $\overline{RAS}$	t_{RAC}	—	50	—	60	—	70	ns	4, 5, 6
Access Time from $\overline{CAS}$	t_{CAC}	—	13	—	15	—	20	ns	4, 5
Access Time from Column Address	t_{AA}	—	25	—	30	—	35	ns	4, 6
Access Time from $\overline{CAS}$ Precharge	t_{CPA}	—	30	—	35	—	40	ns	4, 12
Access Time from $\overline{OE}$	t_{OEA}	—	13	—	15	—	20	ns	4
Output Low Impedance Time from $\overline{CAS}$	t_{CLZ}	0	—	0	—	0	—	ns	4
$\overline{CAS}$ to Data Output Buffer Turn-off Delay Time	t_{OFF}	0	13	0	15	0	20	ns	7
$\overline{OE}$ to Data Output Buffer Turn-off Delay Time	t_{OEZ}	0	13	0	15	0	20	ns	7
Transition Time	t_T	3	50	3	50	3	50	ns	3
Refresh Period	t_{REF}	—	64	—	64	—	64	ms	
Refresh Period (SL version)	t_{REF}	—	128	—	128	—	128	ms	15
$\overline{RAS}$ Precharge Time	t_{RP}	30	—	40	—	50	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	50	10,000	60	10,000	70	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	50	100,000	60	100,000	70	100,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	13	—	15	—	20	—	ns	
$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	t_{ROH}	13	—	15	—	20	—	ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	7	—	10	—	10	—	ns	14
$\overline{CAS}$ Pulse Width	t_{CAS}	13	10,000	15	10,000	20	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	50	—	60	—	70	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	—	5	—	5	—	ns	12
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	30	—	35	—	40	—	ns	12
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	17	37	20	45	20	50	ns	5
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	12	25	15	30	15	35	ns	6
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	7	—	10	—	10	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	11
Column Address Hold Time	t_{CAH}	7	—	10	—	15	—	ns	11
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	25	—	30	—	35	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	11
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	ns	8, 11
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	ns	8

AC Characteristics (2/2)

(V$_{CC}$ = 3.3 V ±0.3 V, Ta = 0°C to 70°C) Note 1, 2, 3

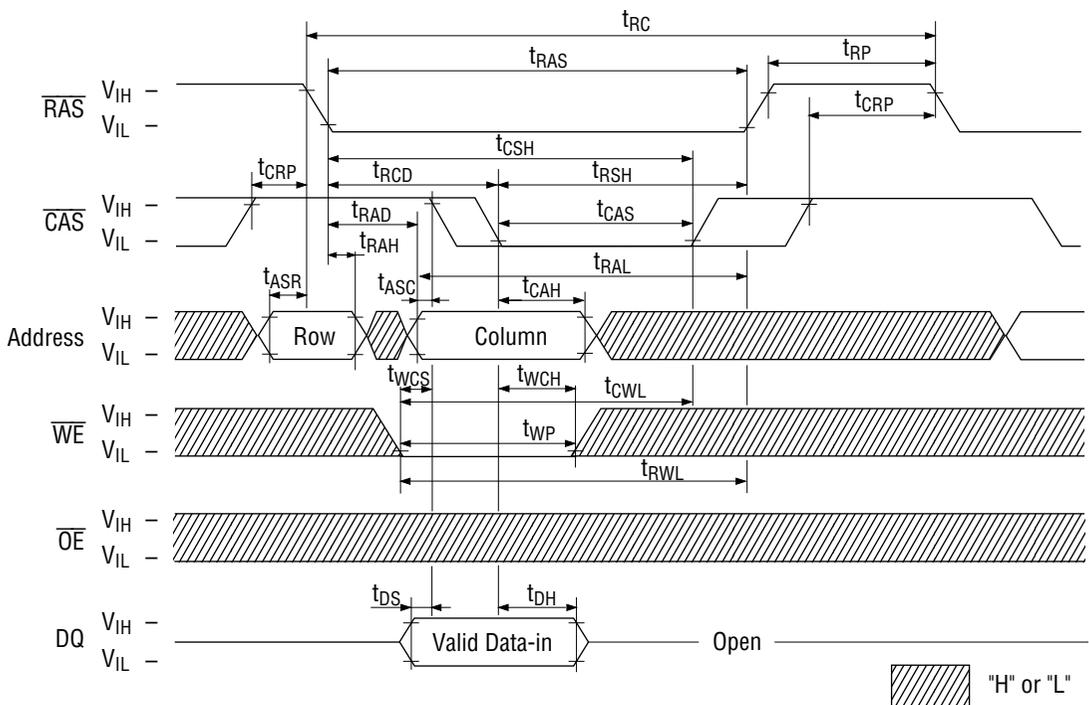| Parameter	Symbol	MSM51V16160 D/DSL-50		MSM51V16160 D/DSL-60		MSM51V16160 D/DSL-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Command Set-up Time	t$_{WCS}$	0	—	0	—	0	—	ns	9, 11
Write Command Hold Time	t$_{WCH}$	7	—	10	—	15	—	ns	11
Write Command Pulse Width	t$_{WP}$	7	—	10	—	10	—	ns	
$\overline{OE}$ Command Hold Time	t$_{OEH}$	13	—	15	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t$_{RWL}$	13	—	15	—	20	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t$_{CWL}$	13	—	15	—	20	—	ns	13
Data-in Set-up Time	t$_{DS}$	0	—	0	—	0	—	ns	10, 11
Data-in Hold Time	t$_{DH}$	7	—	10	—	15	—	ns	10, 11
$\overline{OE}$ to Data-in Delay Time	t$_{OED}$	13	—	15	—	20	—	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t$_{CWD}$	36	—	40	—	50	—	ns	9
Column Address to $\overline{WE}$ Delay Time	t$_{AWD}$	48	—	55	—	65	—	ns	9
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t$_{RWD}$	73	—	85	—	100	—	ns	9
$\overline{CAS}$ Precharge $\overline{WE}$ Delay Time	t$_{CPWD}$	53	—	60	—	70	—	ns	9
$\overline{CAS}$ Active Delay Time from $\overline{RAS}$ Precharge	t$_{RPC}$	5	—	5	—	5	—	ns	11
$\overline{RAS}$ to $\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$)	t$_{CSR}$	10	—	10	—	10	—	ns	11
$\overline{RAS}$ to $\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$)	t$_{CHR}$	10	—	10	—	10	—	ns	12
$\overline{RAS}$ Pulse Width ($\overline{CAS}$ before $\overline{RAS}$ Self-Refresh)	t$_{RASS}$	100	—	100	—	100	—	μs	15
$\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Self-Refresh)	t$_{RPS}$	90	—	110	—	130	—	ns	15
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Self-Refresh)	t$_{CHS}$	−50	—	−50	—	−50	—	ns	15

Notes: 1. A start-up delay of 200 µs is required after power-up, followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh or $\overline{CAS}$ before $\overline{RAS}$ refresh) before proper device operation is achieved.

2. The AC characteristics assume t_T = 5 ns.

3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring input timing signals. Transition times (t_T) are measured between V_{IH} and V_{IL}.

4. This parameter is measured with a load circuit equivalent to 1 TTL load and 100 pF. The output timing reference levels are V_{OH} = 2.0 V and V_{OL} = 0.8 V.

5. Operation within the t_{RCD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then the access time is controlled by t_{CAC}.

6. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, then the access time is controlled by t_{AA}.

7. t_{OFF} (Max.) and t_{OEZ} (Max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.

8. t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. t_{WCS}, t_{CWD}, t_{RWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (Min.), then the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (Min.) , $t_{RWD} \geq t_{RWD}$ (Min.), $t_{AWD} \geq t_{AWD}$ (Min.) and $t_{CPWD} \geq t_{CPWD}$ (Min.), then the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, then the condition of the data out (at access time) is indeterminate.

10. These parameters are referenced to the $\overline{UCAS}$ and $\overline{LCAS}$, leading edges in an early write cycle, and to the $\overline{WE}$ leading edge in an $\overline{OE}$ control write cycle, or a read modify write cycle.

11. These parameters are determined by the falling edge of either $\overline{UCAS}$ or $\overline{LCAS}$, whichever is earlier.

12. These parameters are determined by the rising edge of either $\overline{UCAS}$ or $\overline{LCAS}$, whichever is later.

13. t_{CWL} should be satisfied by both $\overline{UCAS}$ and $\overline{LCAS}$.

14. t_{CP} is determined by the time both $\overline{UCAS}$ and $\overline{LCAS}$ and high.
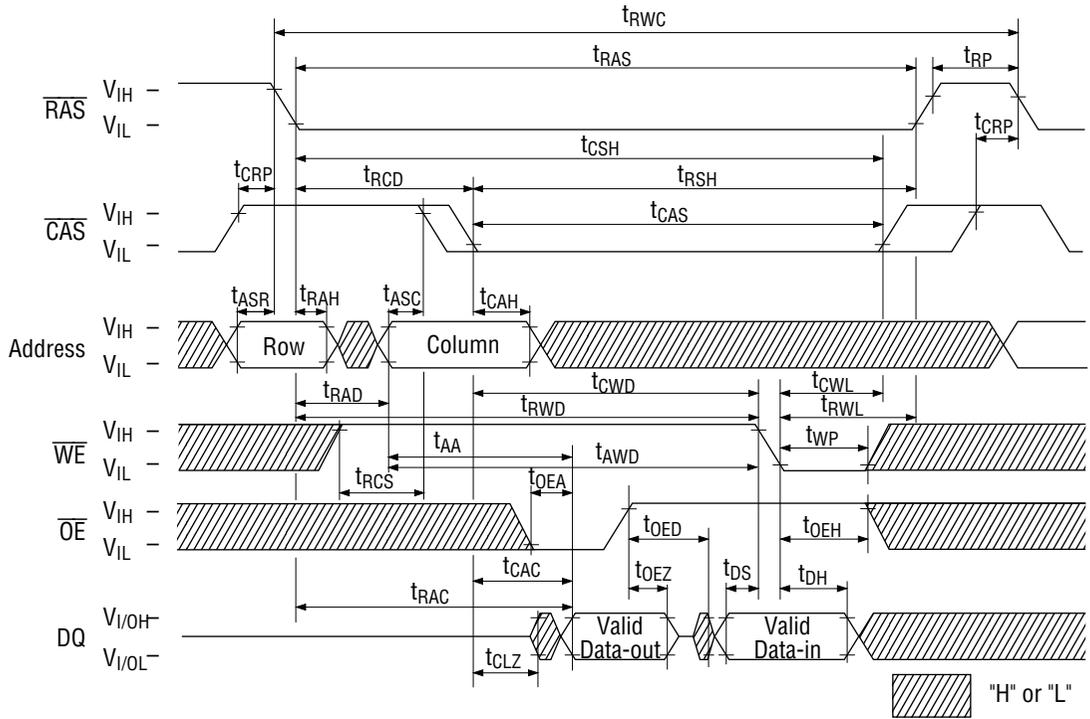
15. Only SL version.

TIMING WAVEFORM

Read Cycle

Write Cycle (Early Write)

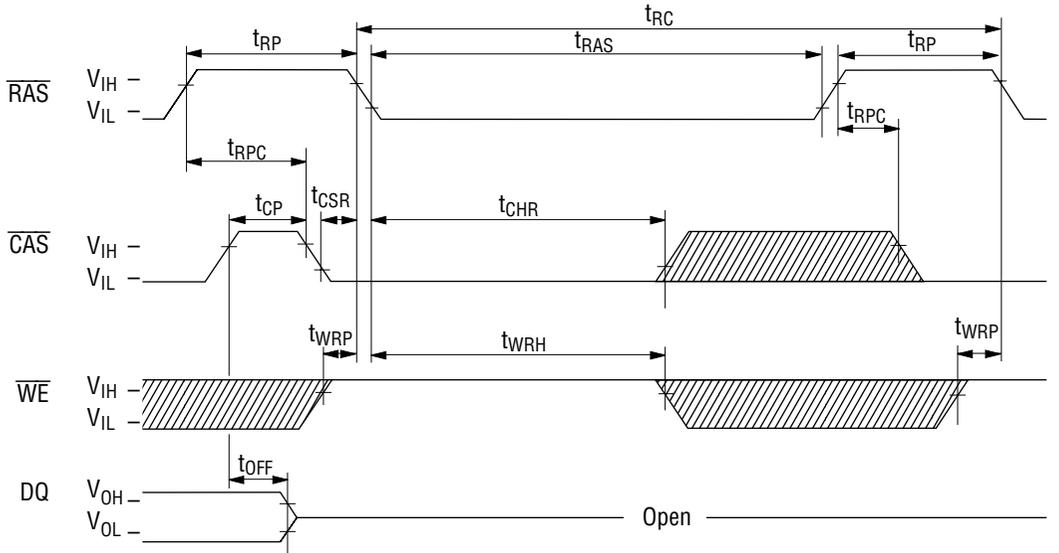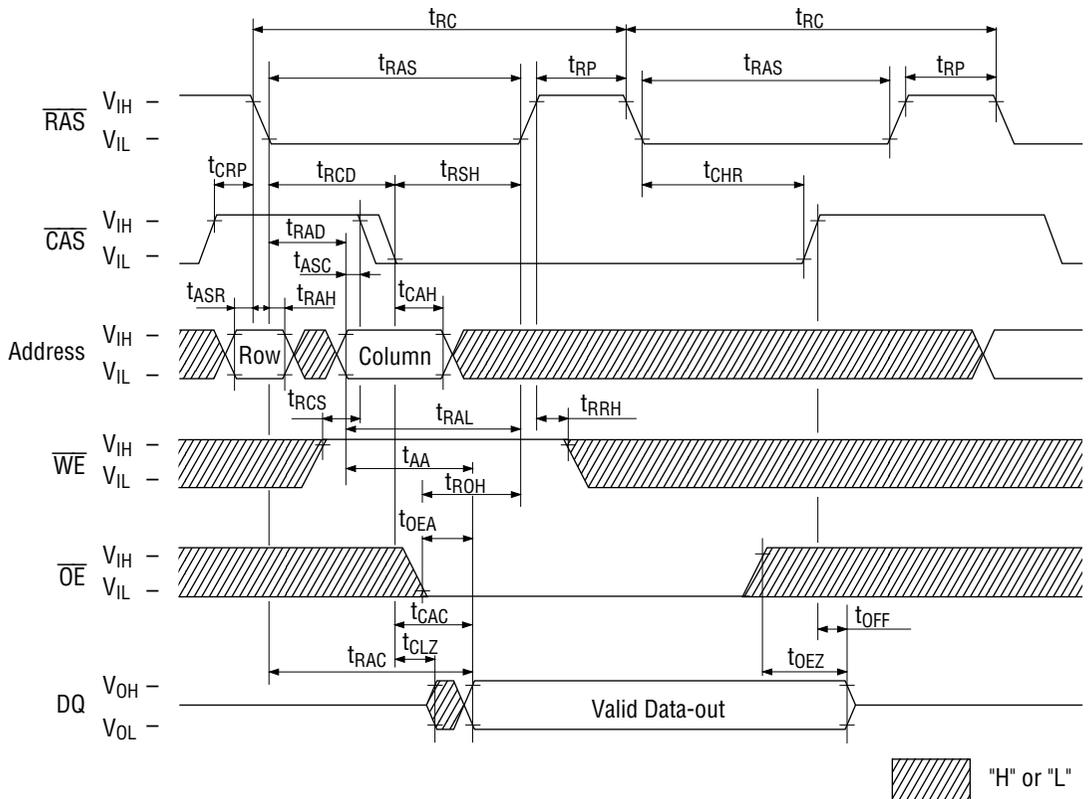**Read Modify Write Cycle**

Fast Page Mode Read Cycle

Fast Page Mode Write Cycle (Early Write)

Note: $\overline{OE}$ = "H" or "L"   "H" or "L"

Fast Page Mode Read Modify Write Cycle

RAS-Only Refresh Cycle

Note: $\overline{WE}$, $\overline{OE}$ = "H" or "L"   "H" or "L"

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle

Note: $\overline{OE}$, Address = "H" or "L"   [hatched] "H" or "L"

Hidden Refresh Read Cycle

[hatched] "H" or "L"

Hidden Refresh Write Cycle
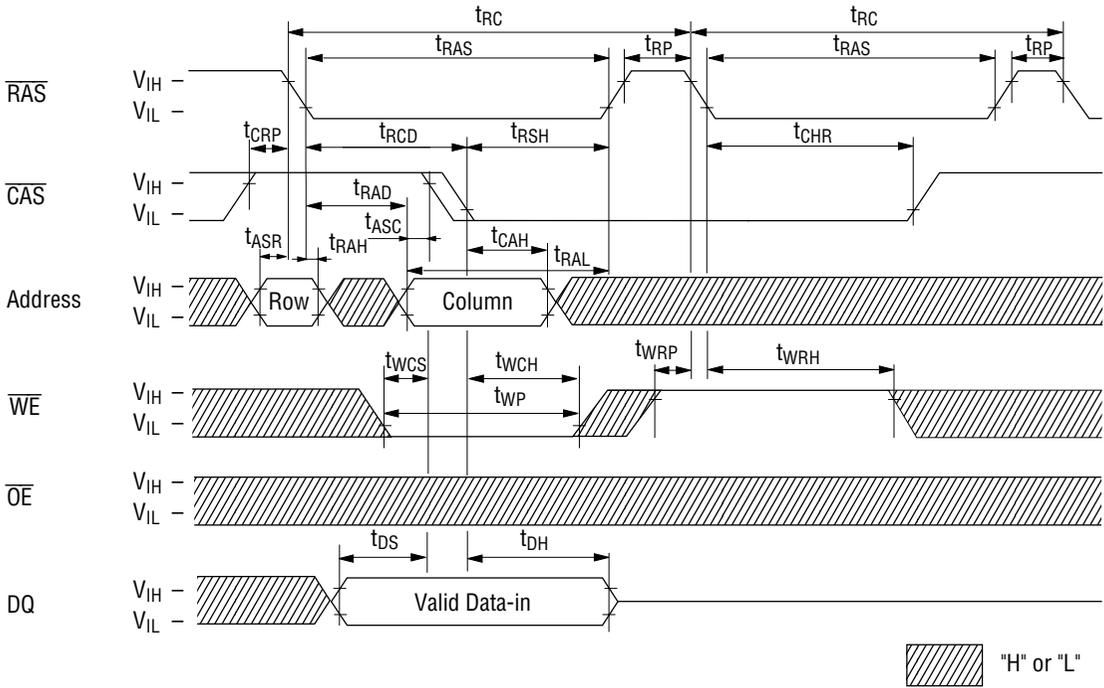
CAS before RAS Self-Refresh Cycle
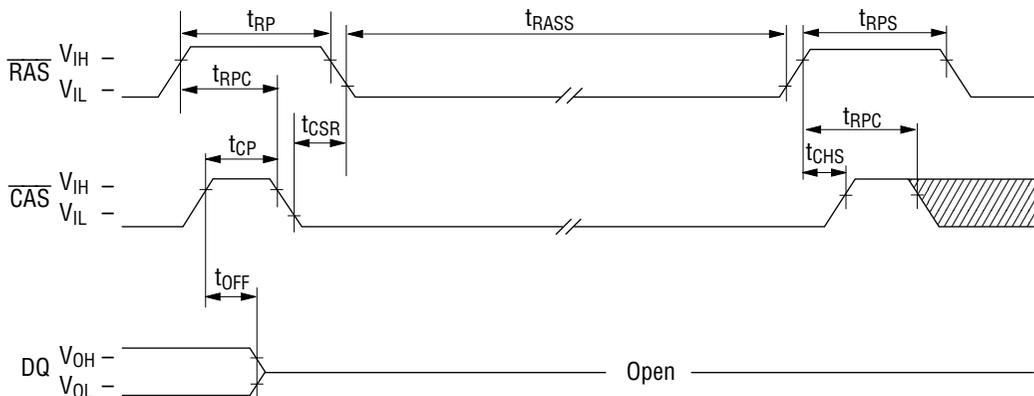
Note: WE, OE, Address = "H" or "L"   ▨ "H" or "L"
Only SL version

PACKAGE DIMENSIONS

(Unit : mm)
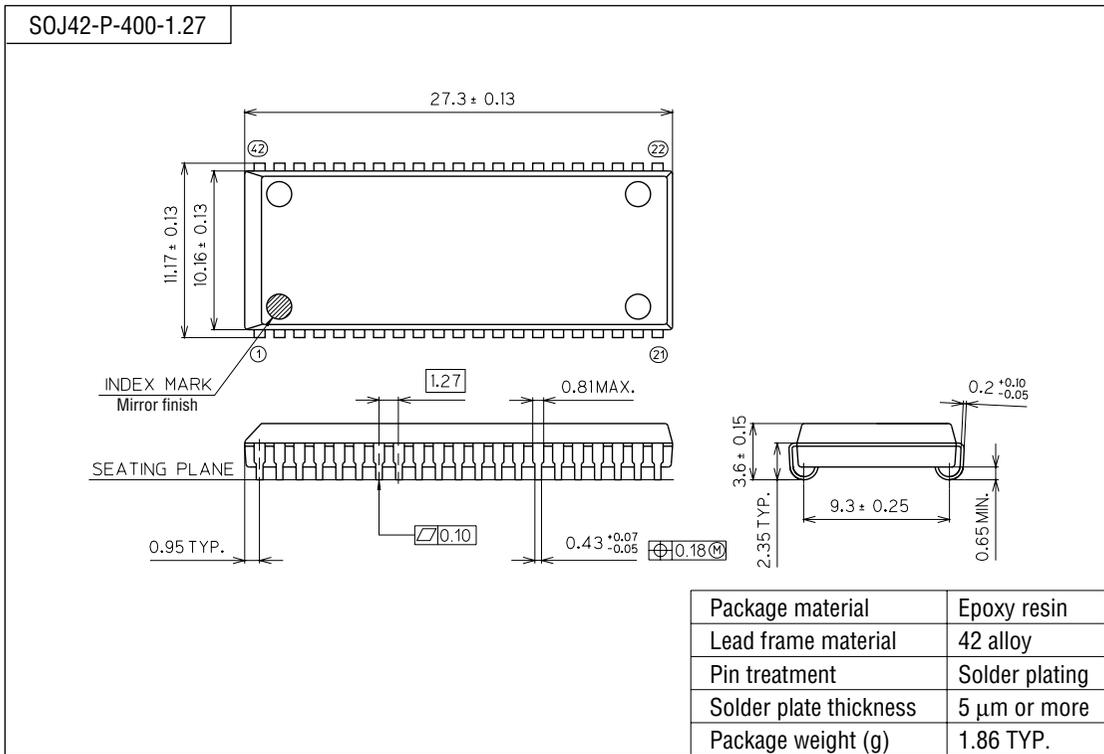
SOJ42-P-400-1.27

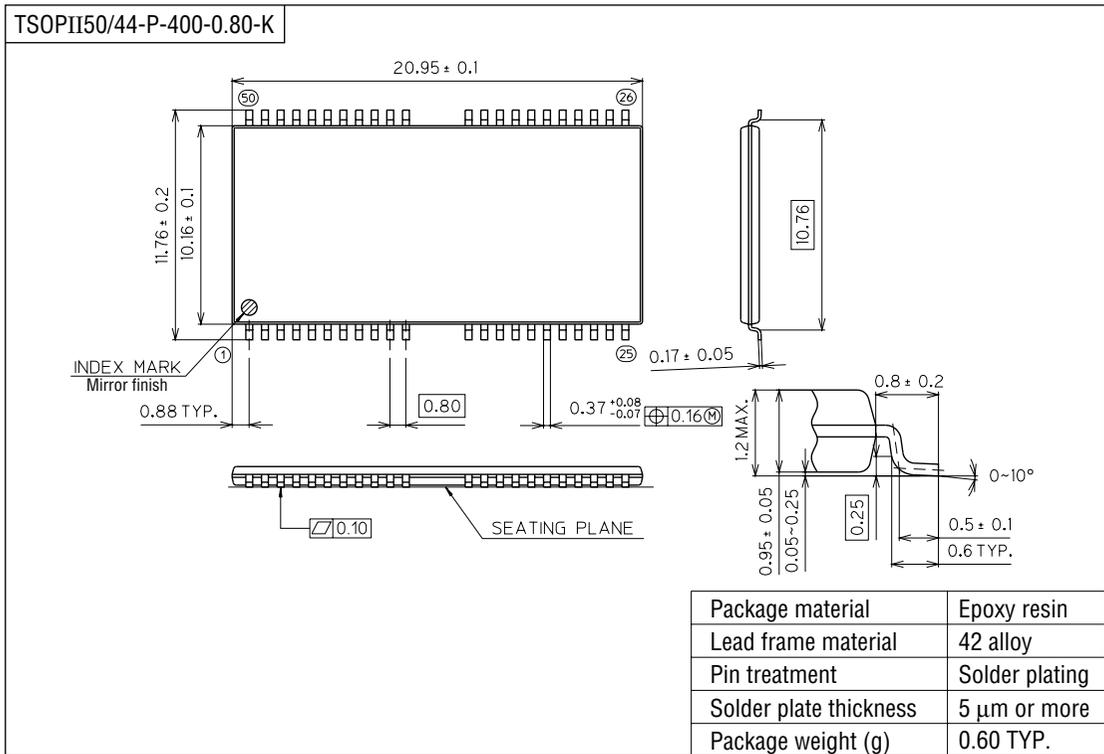| Package material | Epoxy resin |
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	1.86 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

TSOPII50/44-P-400-0.80-K

Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.60 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).