

OKI Semiconductor

MSM514265B/BSL

262,144-Word × 16-Bit DYNAMIC RAM : HYPER PAGE MODE TYPE

DESCRIPTION

The MSM514265B/BSL is a new generation Dynamic RAM organized as 262,144-word × 16-bit configuration.

The technology used to fabricate the MSM514265B/BSL is OKI's CMOS silicon gate process technology.

The device operates at a single 5V power supply. Its I/O pins are TTL compatible.

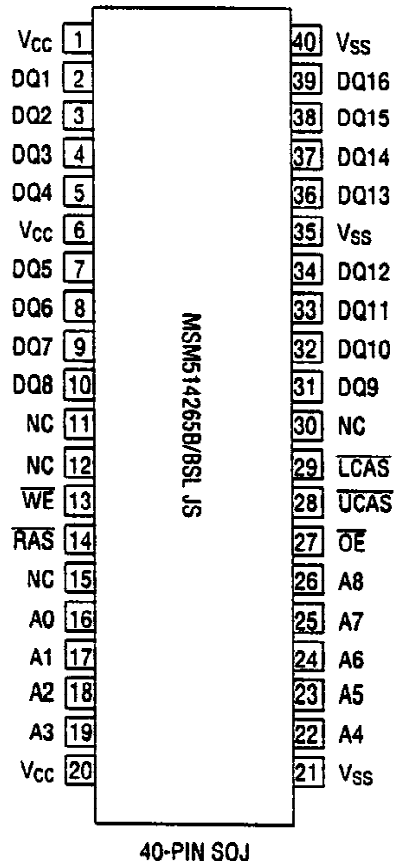
FEATURES

- Silicon gate, quadruple polysilicon CMOS, 1 transistor memory cell
- 262,144-word × 16-bit organization
- Single 5V power supply, ±10% tolerance
- Input: TTL compatible
- Output: TTL compatible, tristate
- Refresh: 512 cycles/8ms, 512 cycles/128ms (SL version)
- Hyper page mode, read modify write capability
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, Hidden refresh, $\overline{\text{RAS}}$ only refresh capability
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self-refresh capability (SL version)
- Package :
40-Pin 400mil Plastic SOJ (SOJ40-P-400)

PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}	t_{OEA}		Operating (Max.)	Standby (Max.)
MSM514265B/BSL-50	50ns	22ns	12ns	12ns	84ns	1210mW	5.5mW/ 1.1mW (SL version)
MSM514265B/BSL-60	60ns	30ns	15ns	15ns	104ns	1100mW	
MSM514265B/BSL-70	70ns	35ns	20ns	20ns	124ns	990mW	

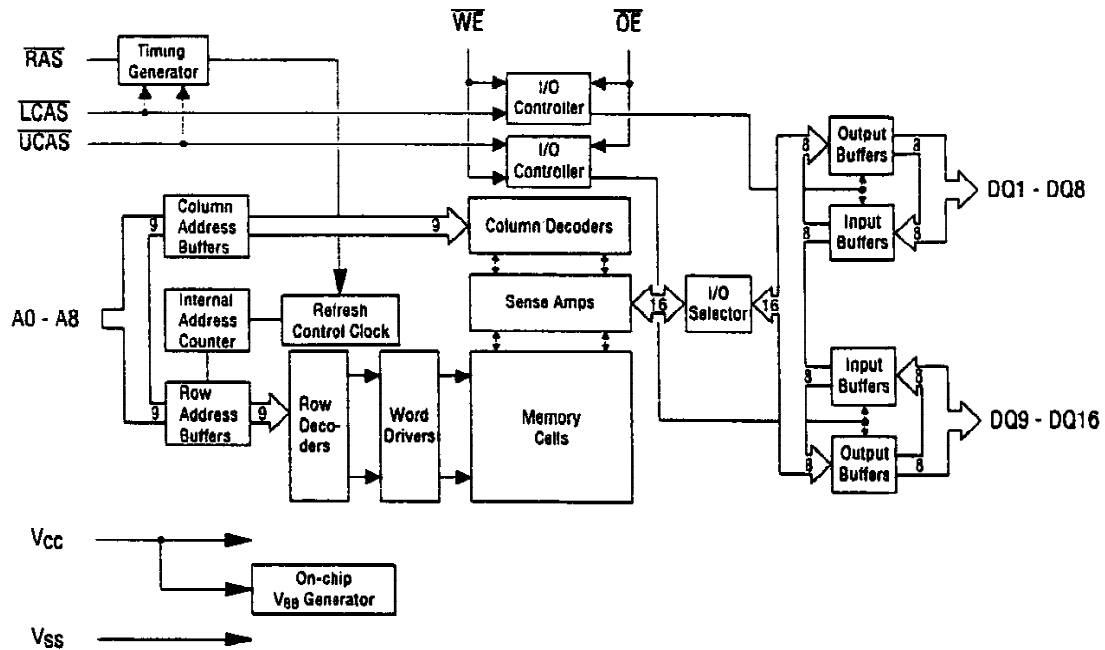
PIN CONFIGURATION (TOP VIEW)



Pin Name	Function
A0 - A8	Address Input
RAS	Row Address Strobe
LCAS	Lower Byte Column Address Strobe
UCAS	Upper Byte Column Address Strobe
DQ1 - DQ16	Data - Input / Data - Output
OE	Output Enable
WE	Write Enable
Vcc	Power Supply (5V)
Vss	Ground (0V)
NC	No Connection

Note: Same power supply voltage must be provided to every V_{CC} pin, and same GND voltage level must be provided to every V_{SS} pin.

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL TABLE

Input Pin					DQ Pin		Functional Mode
RAS	LCAS	UCAS	WE	OE	DQ1 - DQ8	DQ9 - DQ16	
H	*	*	*	*	High-Z	High-Z	Standby
L	H	H	*	*	High-Z	High-Z	Refresh
L	L	H	H	L	DOUT	High-Z	Lower Byte Read
L	H	L	H	L	High-Z	DOUT	Upper Byte Read
L	L	L	H	L	DOUT	DOUT	Word Read
L	L	H	L	H	DIN	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	DIN	Upper Byte Write
L	L	L	L	H	DIN	DIN	Word Write
L	L	L	H	H	High-Z	High-Z	—

ELECTRICAL CHARACTERISTICS**Absolute Maximum Ratings**

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V _{SS}	V _I	-1.0 to 7.0	V
Short Circuit Output Current	I _{OS}	50	mA
Power Dissipation	P _D *	1	W
Operating Temperature	T _{opr}	0 to 70	°C
Storage Temperature	T _{stg}	-55 to 150	°C

*: T_a = 25°C**Recommended Operating Conditions**(T_a = 0 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V _{CC}	4.5	5.0	5.5	V
	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	—	6.5	V
Input Low Voltage	V _{IL}	-1.0	—	0.8	V

Capacitance(V_{CC} = 5V ± 10%, T_a = 25°C, f = 1MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A8)	C _{IN1}	—	7	pF
Input Capacitance (RAS, LCAS, UCAS, WE, OE)	C _{IN2}	—	7	pF
Output Capacitance (DQ1 - DQ16)	C _{I/O}	—	10	pF

DC Characteristics

($V_{CC} = 5V \pm 10\%$, $T_a = 0$ to $70^\circ C$)

Parameter	Symbol	Condition	MSM514265B /BSL-50		MSM514265B /BSL-60		MSM514265B /BSL-70		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	V_{OH}	$I_{OH} = -2.0mA$	2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V	
Output Low Voltage	V_{OL}	$I_{OL} = 2.0mA$	0	0.8	0	0.8	0	0.8	V	
Input Leakage Current	I_{LI}	$0V \leq V_i \leq 6.5V$; All other pins not under test = $0V$	-10	10	-10	10	-10	10	μA	
Output Leakage Current	I_{LO}	DQ _i Disable $0V \leq V_o \leq 5.5V$	-10	10	-10	10	-10	10	μA	
Average Power Supply Current (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling $t_{RC} = \text{Min.}$	—	220	—	200	—	180	mA	1, 2
Power Supply Current (Standby)	I_{CC2}	$\overline{RAS}$, $\overline{CAS} = V_{IH}$	—	2	—	2	—	2	mA	1
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2V$	—	1	—	1	—	1	μA	1, 5
			—	200	—	200	—	200	μA	
Average Power Supply Current (RAS Only Refresh)	I_{CC3}	$\overline{RAS} = \text{cycling}$ $\overline{CAS} = V_{IH}$ $t_{RC} = \text{Min.}$	—	220	—	200	—	180	mA	1, 2
Power Supply Current (Standby)	I_{CC5}	$\overline{RAS} = V_{IH}$ $\overline{CAS} = V_{IL}$ Dout = Enable	—	5	—	5	—	5	mA	1
Average Power Supply Current (CAS Before RAS Refresh)	I_{CC6}	$\overline{RAS} = \text{cycling}$ $\overline{CAS}$ before $\overline{RAS}$	—	220	—	200	—	180	mA	1, 2
Average Power Supply Current (Fast Page Mode)	I_{CC7}	$\overline{RAS} = V_{IL}$ $\overline{CAS}$ cycling $t_{PC} = \text{Min.}$	—	220	—	200	—	180	mA	1, 3
Average Power Supply Current (Battery Backup)	I_{CC10}	$t_{RC} = 125\mu s$ $\overline{CAS}$ before $\overline{RAS}$ $t_{RAS} \leq 1\mu s$	—	300	—	300	—	300	μA	1, 2, 4, 5
Average Power Supply Current (CAS Before RAS Self-refresh)	I_{CC8}	$\overline{RAS} \leq 0.2V$ $\overline{CAS} \leq 0.2V$	—	200	—	200	—	200	μA	1, 5

- Notes:
1. Specified values are obtained with the output open.
 2. Address can be changed once or less while $\overline{RAS} = V_{IL}$.
 3. Address can be changed once or less while $\overline{CAS} = V_{IH}$.
 4. $V_{CC} - 0.2V \leq V_{IH} \leq 6.5V$, $-1.0V \leq V_{IL} \leq 0.2V$.
 5. SL version.

AC Characteristics (1/2)

(V_{CC} = 5V ± 10%, T_a = 0 to 70°C) Note 1, 2, 3

Parameter	Symbol	MSM 514265B/BSL-50		MSM 514265B/BSL-60		MSM 514265B/BSL-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t _{RC}	84	—	104	—	124	—	ns	
Read Modify Write Cycle Time	t _{RMW}	109	—	134	—	159	—	ns	
Hyper Page Mode Cycle Time	t _{HPC}	20	—	25	—	25	—	ns	
Hyper Page Mode Read Modify Write Cycle Time	t _{PRMW}	54	—	67	—	77	—	ns	
Access Time from $\overline{\text{RAS}}$	t _{RAC}	—	50	—	60	—	70	ns	4, 5, 6
Access Time from $\overline{\text{CAS}}$	t _{CAC}	—	12	—	15	—	20	ns	4, 5
Access Time from Column Address	t _{AA}	—	22	—	30	—	35	ns	4, 6
Access Time from $\overline{\text{OE}}$	t _{OEa}	—	12	—	15	—	20	ns	4
Access Time from $\overline{\text{CAS}}$ Precharge	t _{CPA}	—	27	—	35	—	40	ns	4, 13
Output Low Impedance Time from $\overline{\text{CAS}}$	t _{CLZ}	0	—	0	—	0	—	ns	4
$\overline{\text{OE}}$ to Data Output Buffer Turn-off Delay Time	t _{OEZ}	0	12	0	15	0	20	ns	7
Transition Time	t _T	1	50	1	50	1	50	ns	3
Refresh Period	t _{REF}	—	8	—	8	—	8	ms	
Refresh Period (SL version)	t _{REF}	—	128	—	128	—	128	ms	16
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	30	—	40	—	50	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RAS}	50	10,000	60	10,000	70	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Hyper Page Mode)	t _{RASP}	50	100,000	60	100,000	70	100,000	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	7	—	10	—	15	—	ns	
$\overline{\text{RAS}}$ Hold Time Reference to $\overline{\text{OE}}$	t _{ROH}	7	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ Precharge Time	t _{CP}	7	—	10	—	10	—	ns	15
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	7	10,000	10	10,000	10	10,000	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	35	—	40	—	45	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	5	—	5	—	10	—	ns	13
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	11	38	14	45	14	50	ns	5
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	9	28	12	30	12	35	ns	6
$\overline{\text{RAS}}$ to Second $\overline{\text{CAS}}$ Delay Time	t _{RSCD}	50	—	60	—	70	—	ns	
Row Address Set-up Time	t _{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t _{RAH}	7	—	10	—	10	—	ns	
Column Address Set-up Time	t _{ASC}	0	—	0	—	0	—	ns	12
Column Address Hold Time	t _{CAH}	5	—	7	—	10	—	ns	12
Column Address Hold Time from $\overline{\text{RAS}}$	t _{AR}	38	—	45	—	50	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t _{RAL}	22	—	30	—	35	—	ns	
Read Command Set-up Time	t _{RCS}	0	—	0	—	0	—	ns	12
Read Command Hold Time	t _{RCH}	0	—	0	—	0	—	ns	9, 12
Read Command Hold Time Reference to $\overline{\text{RAS}}$	t _{RRH}	0	—	0	—	0	—	ns	9

AC Characteristics (2/2)

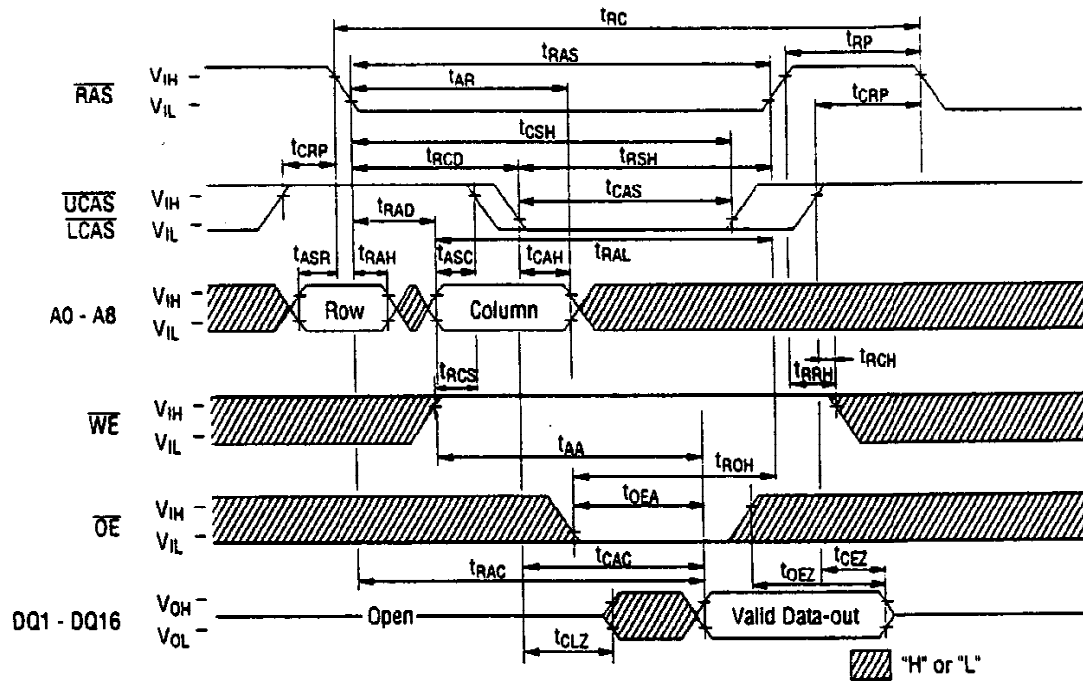
(V_{CC} = 5V ± 10%, T_a = 0 to 70°C) Note 1, 2, 3

Parameter	Symbol	MSM 514265B/BSL-50		MSM 514265B/BSL-60		MSM 514265B/BSL-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Command Set-up Time	t _{WCS}	0	—	0	—	0	—	ns	10, 12
Write Command Hold Time	t _{WCH}	5	—	7	—	7	—	ns	12
Write Command Pulse Width	t _{WP}	5	—	7	—	7	—	ns	
Write Command Hold Time from RAS	t _{WCR}	38	—	45	—	50	—	ns	
OE Command Hold Time	t _{OEH}	12	—	15	—	20	—	ns	
Write Command to CAS Lead Time	t _{CWL}	7	—	9	—	9	—	ns	14
Write Command to RAS Lead Time	t _{RWL}	7	—	9	—	9	—	ns	
Data-in Set-up Time	t _{DS}	0	—	0	—	0	—	ns	11, 12
Data-in Hold Time	t _{DH}	5	—	7	—	7	—	ns	11, 12
Data-in Hold Time from RAS	t _{DHR}	38	—	45	—	50	—	ns	
OE to Data-in Delay Time	t _{OED}	12	—	15	—	20	—	ns	
CAS to WE Delay Time	t _{CWD}	28	—	34	—	44	—	ns	10
Column Address to WE Delay Time	t _{AWD}	38	—	49	—	59	—	ns	10
RAS to WE Delay Time	t _{RWD}	66	—	79	—	94	—	ns	10
CAS Precharge WE Delay Time	t _{CPWD}	43	—	54	—	64	—	ns	10
CAS Active Delay Time from RAS Precharge	t _{RPC}	5	—	5	—	5	—	ns	12
RAS to CAS Set-up Time (CAS Before RAS)	t _{CSR}	5	—	5	—	5	—	ns	12
RAS to CAS Hold Time (CAS Before RAS)	t _{CHR}	7	—	10	—	10	—	ns	13
CAS Precharge Time (Refresh Counter Test)	t _{CPT}	20	—	20	—	20	—	ns	13
CAS Precharge Time	t _{CPN}	10	—	10	—	10	—	ns	15
RAS Pulse Width (CAS Before RAS Self-refresh)	t _{RASS}	100	—	100	—	100	—	μs	16
RAS Precharge Time (CAS Before RAS Self-refresh)	t _{RPS}	84	—	104	—	124	—	ns	16
CAS Hold Time (CAS Before RAS Self-refresh)	t _{CHS}	-50	—	-50	—	-50	—	ns	16
Data Output Hold After CAS Low	t _{DOH}	5	—	5	—	5	—	ns	
CAS to Data Output Buffer Turn-off Delay Time	t _{CEZ}	0	12	0	15	0	20	ns	7, 8
RAS to Data Output Buffer Turn-off Delay Time	t _{REZ}	0	12	0	15	0	20	ns	7, 8
WE to Data Output Buffer Turn-off Delay Time	t _{WEZ}	0	12	0	15	0	20	ns	7
OE Hold Time from CAS (DOUR Disable)	t _{CHO}	5	—	5	—	10	—	ns	
OE Precharge Time	t _{OEP}	7	—	10	—	10	—	ns	
OE Command Hold Time	t _{OCH}	7	—	10	—	10	—	ns	
WE Pulse Width (DOUR Disable)	t _{WPE}	5	—	7	—	7	—	ns	

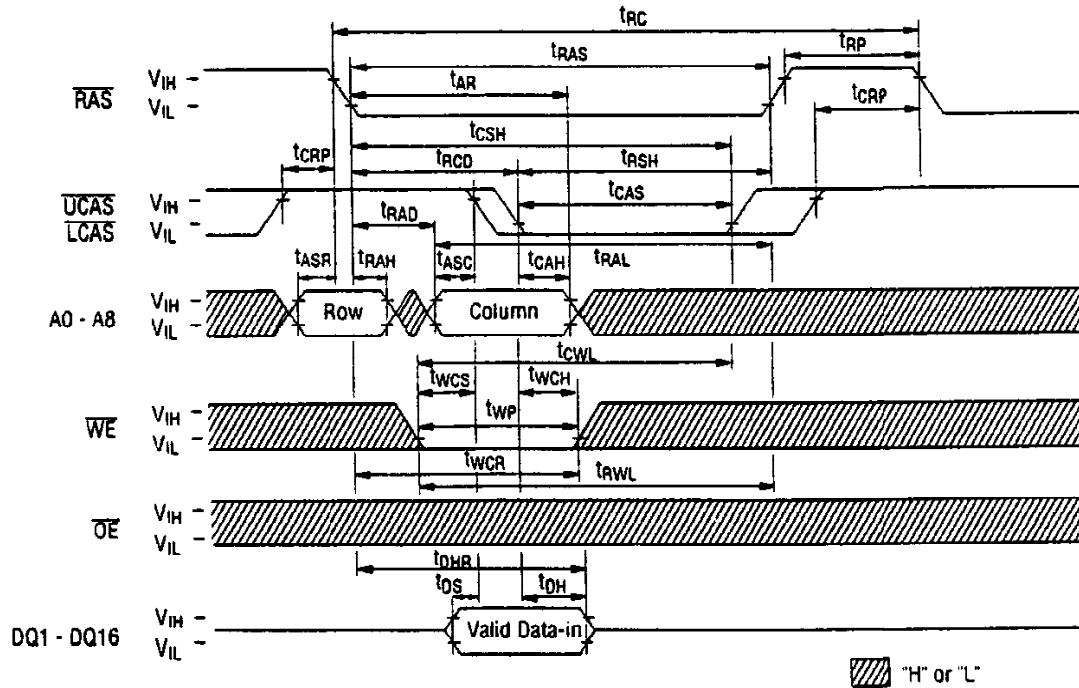
- Notes:
1. An initial pause of 200 μ s is required after power-up followed by any 8 $\overline{\text{RAS}}$ cycles (Example: $\overline{\text{RAS}}$ only refresh) before proper device operation is achieved.
 2. The AC characteristics assume $t_T = 2\text{ns}$.
 3. $V_{IH}(\text{Min.})$ and $V_{IL}(\text{Max.})$ are reference levels of input signals for timing measurement. Transition times(t_T) are measured between V_{IH} and V_{IL} .
 4. Measured with a load circuit equivalent to 1 TTL loads and 50pF.
 5. Operation within the $t_{\text{RCD}}(\text{Max.})$ limit insures that $t_{\text{RAC}}(\text{Max.})$ can be met. $t_{\text{RCD}}(\text{Max.})$ is specified as a reference point only: if t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{Max.})$ limit, then access time is controlled exclusively by t_{CAC} .
 6. Operation within the $t_{\text{RAD}}(\text{Max.})$ limit insures that $t_{\text{RAC}}(\text{Max.})$ can be met. $t_{\text{RAD}}(\text{Max.})$ is specified as a reference point only: if t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{Max.})$ limit, then access time is controlled exclusively by t_{AA} .
 7. $t_{\text{CEZ}}(\text{Max.})$, $t_{\text{REZ}}(\text{Max.})$, $t_{\text{WEZ}}(\text{Max.})$ and $t_{\text{OEZ}}(\text{Max.})$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
 8. Both t_{CEZ} and t_{REZ} must be satisfied for the open circuit condition.
 9. Either t_{RRH} and t_{RCH} must be satisfied for a read cycle.
 10. t_{WCS} , t_{CWD} , t_{RWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{Min.})$, the cycle is an early write cycle and data out will remain open circuit (high impedance) throughout the entire cycle; if $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{Min.})$, $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{Min.})$, $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{Min.})$ and $t_{\text{CPWD}} \geq t_{\text{CPWD}}(\text{Min.})$, the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
 11. These parameters are referenced to $\overline{\text{UCAS}}$, $\overline{\text{LCAS}}$ leading edge in an early write cycle and to $\overline{\text{WE}}$ leading edge in a $\overline{\text{OE}}$ control write cycle or a read modify write cycle.
 12. t_{ASC} , t_{CAH} , t_{RCS} , t_{RCH} , t_{WCS} , t_{DS} , t_{DH} , t_{CSR} and t_{RPC} are determined by the earlier falling edge of $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$.
 13. t_{CRP} , t_{CHR} and t_{CPA} are determined by the later rising edge of $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$.
 14. t_{CWL} should be satisfied by both $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$.
 15. t_{CPN} , t_{CP} and t_{CPT} are determined by the time that both $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ are high.
 16. SL version.

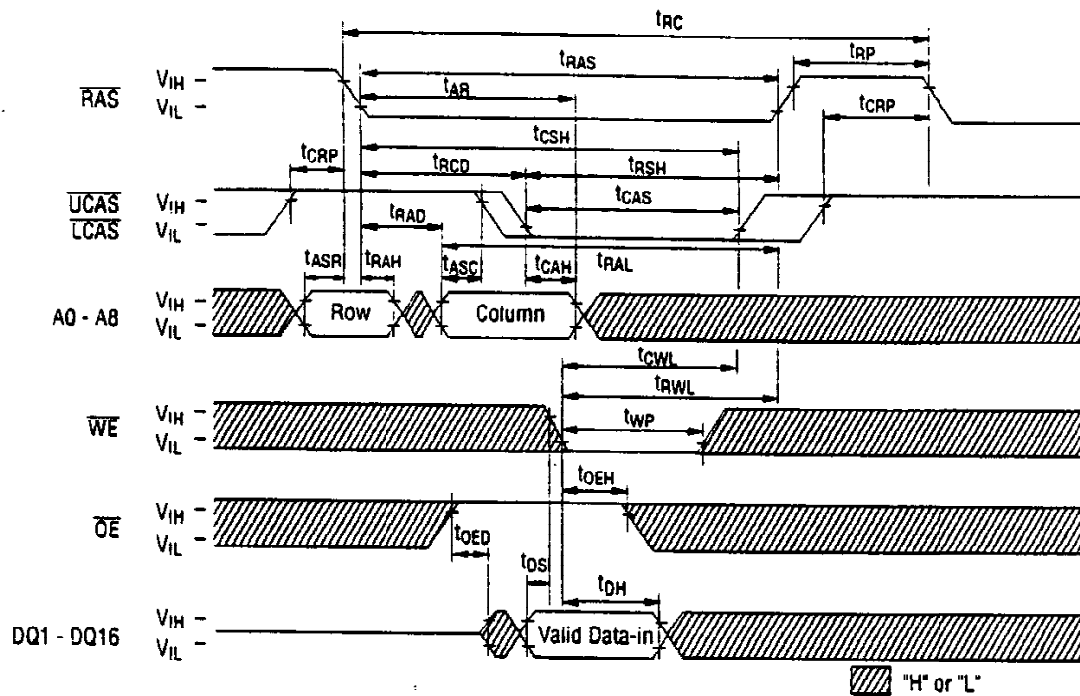
TIMING WAVEFORM

Read Cycle

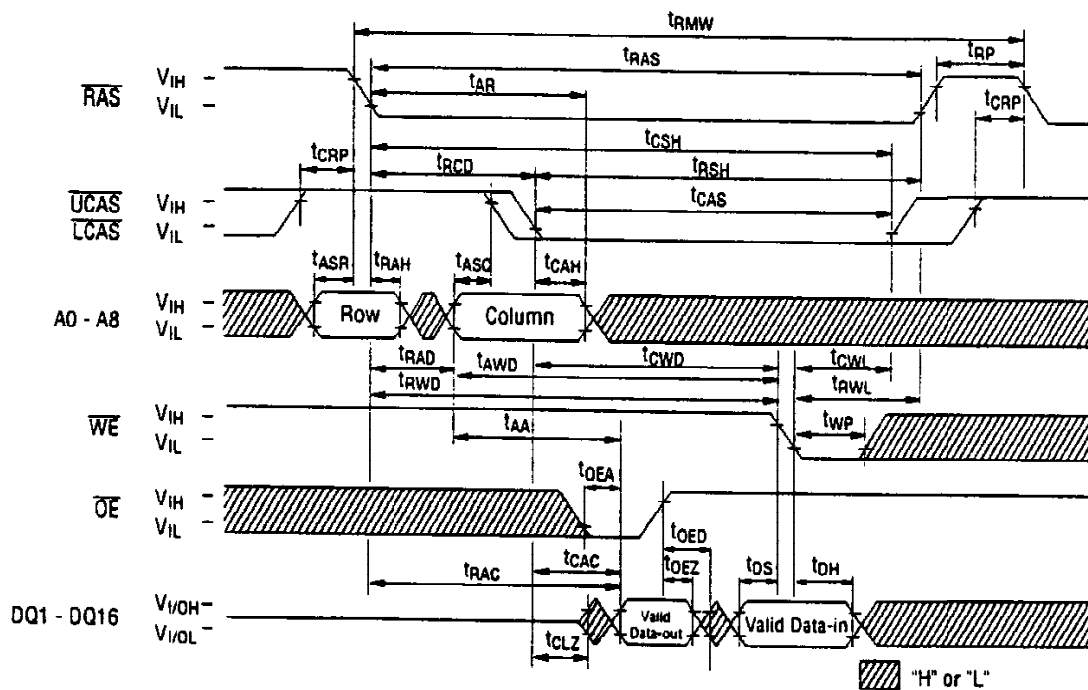


Write Cycle (Early Write)

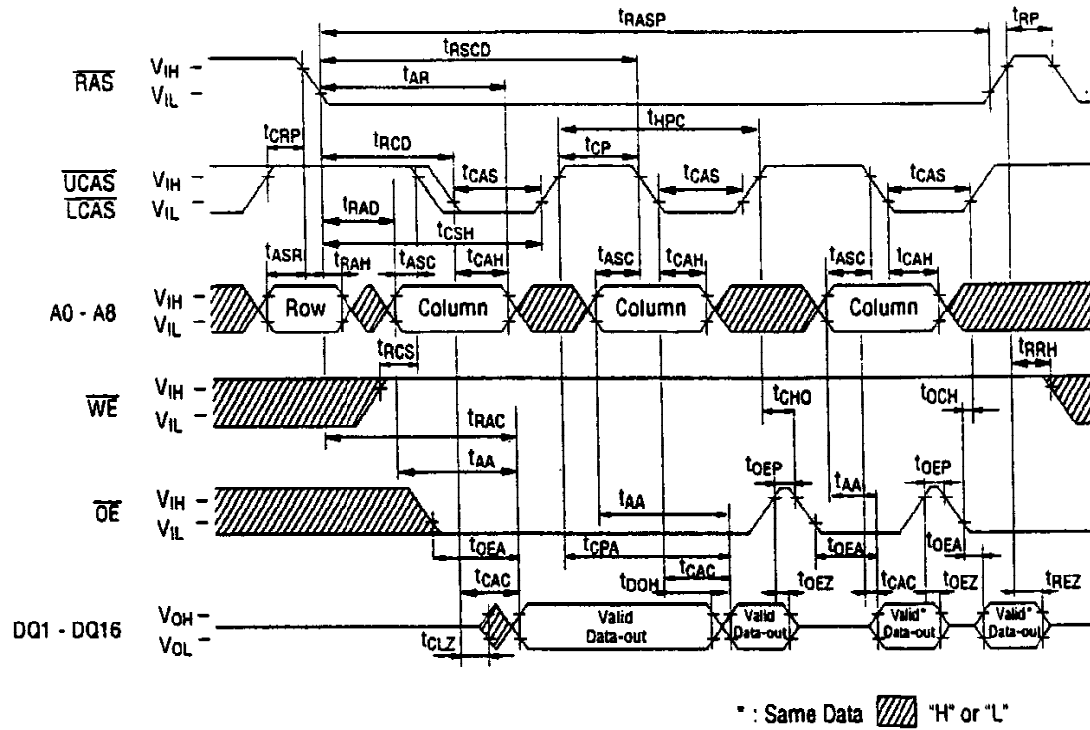


Write Cycle ($\overline{OE}$ Control Write)

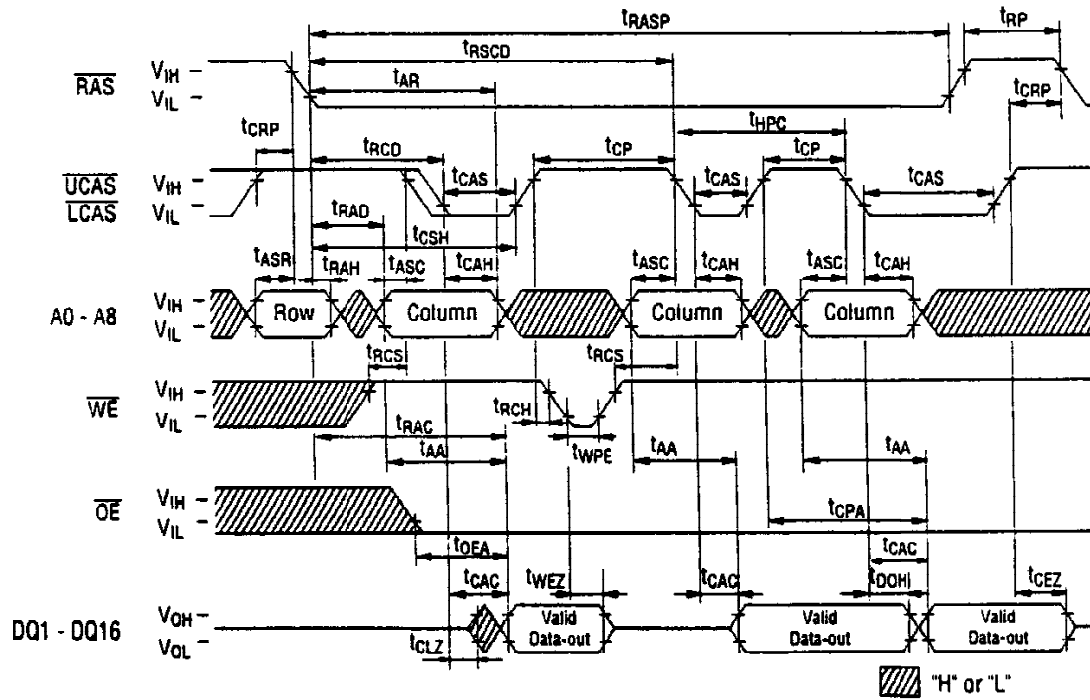
Read Modify Write Cycle



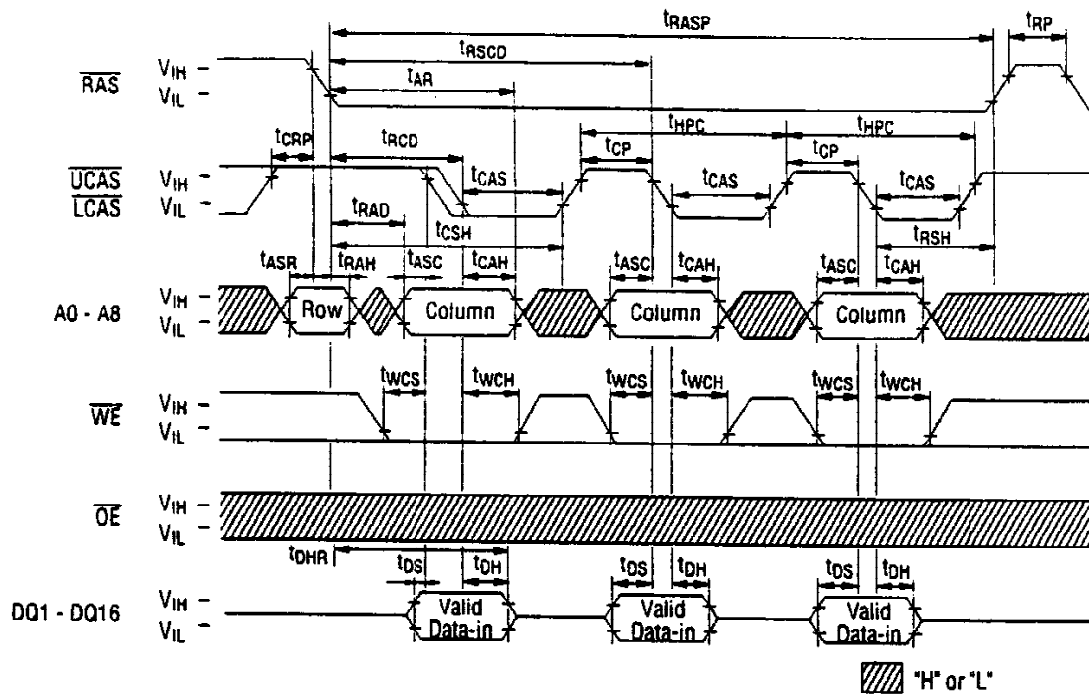
Hyper Page Mode Read Cycle (Part-1)



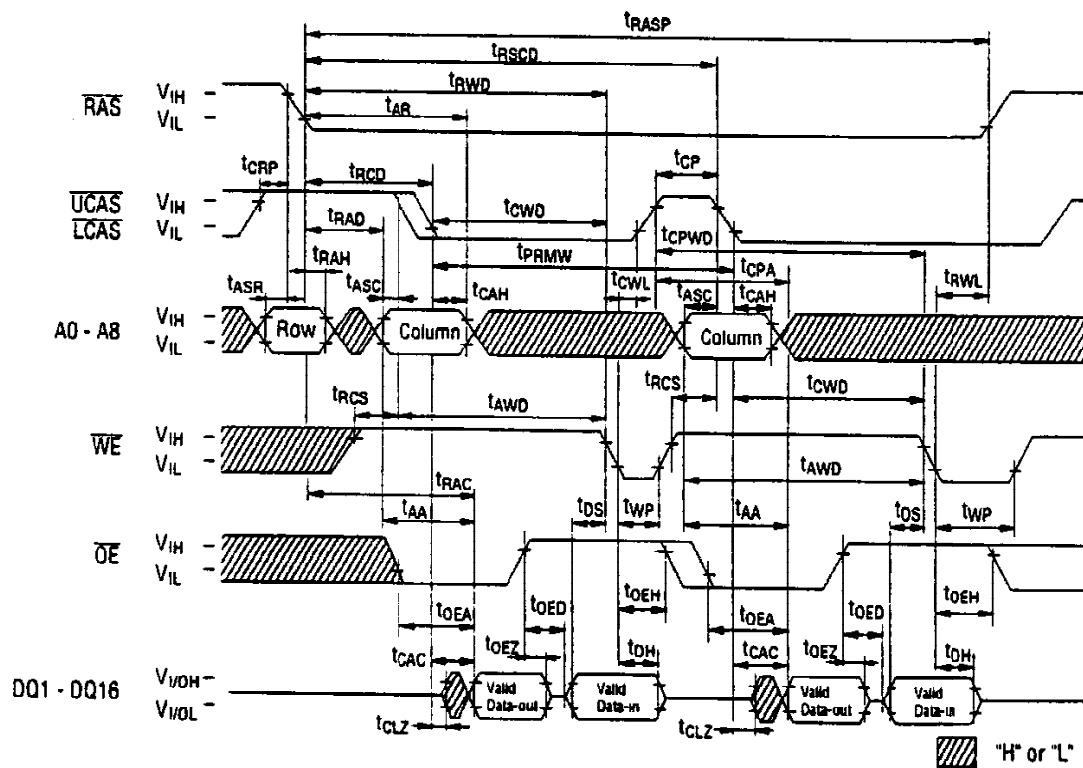
Hyper Page Mode Read Cycle (Part-2)



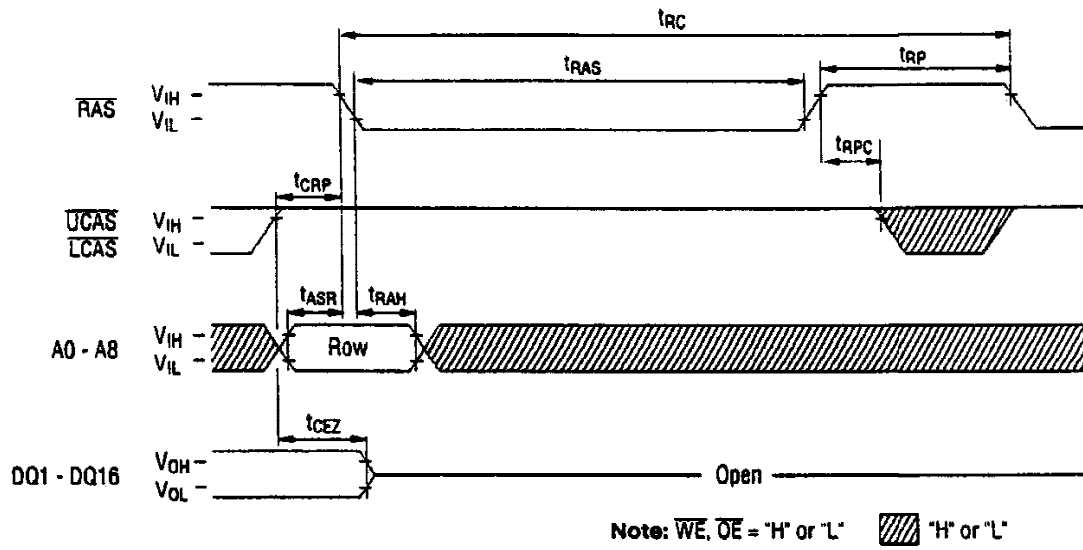
Hyper Page Mode Write Cycle (Early Write)



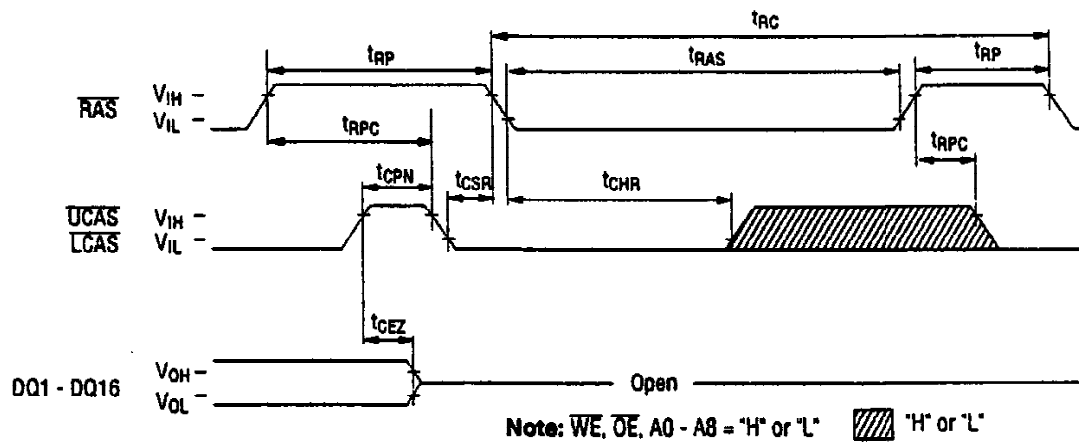
Hyper Page Mode Read Modify Write Cycle



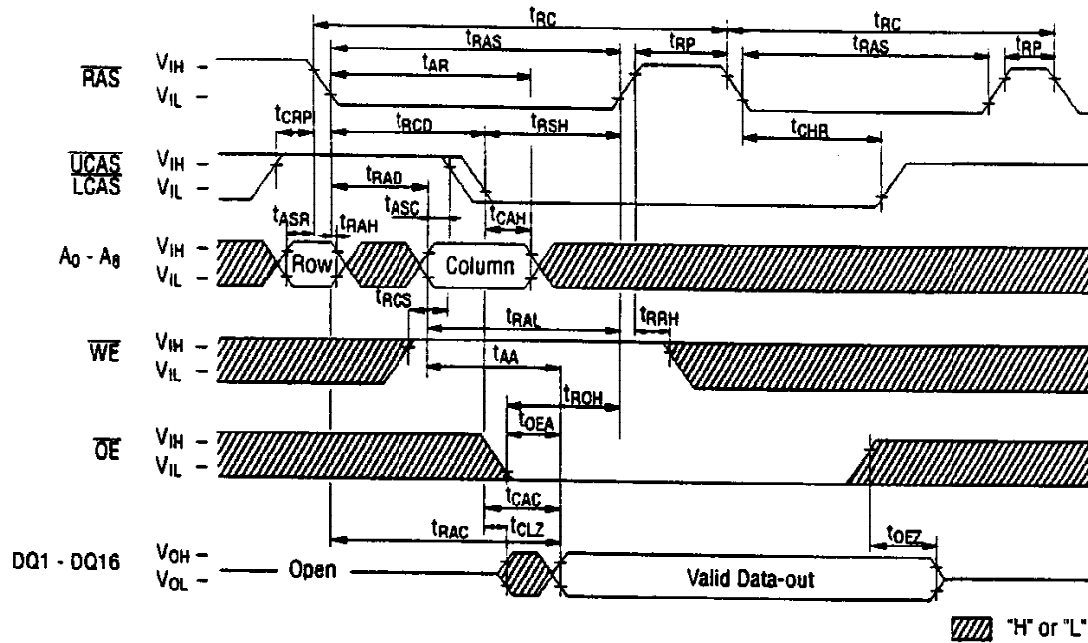
RAS-only Refresh Cycle



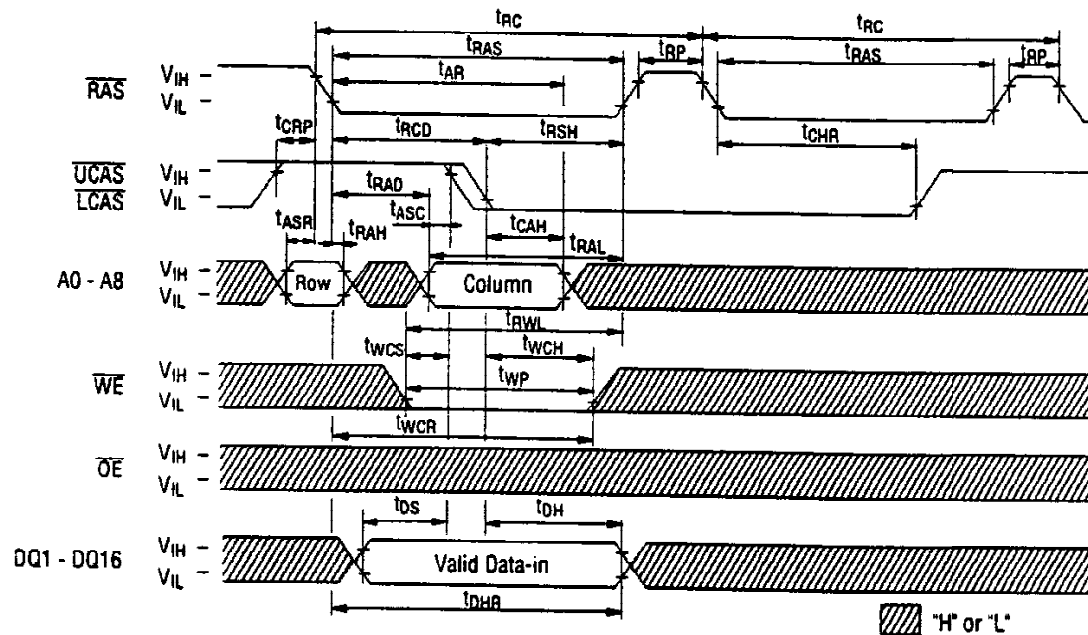
CAS Before RAS Auto Refresh Cycle



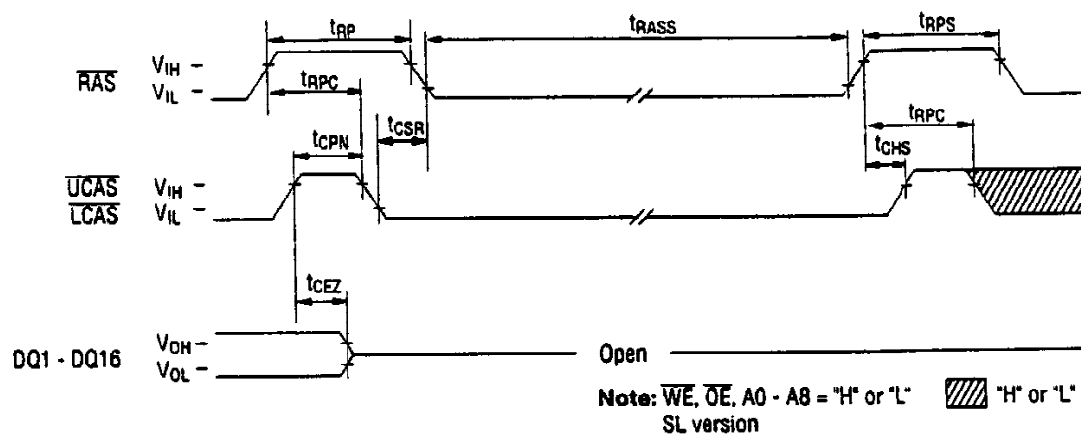
Hidden Refresh Read Cycle



Hidden Refresh Write Cycle



CAS Before RAS Self-refresh Cycle



CAS Before RAS Refresh Counter Test Cycle

