

MSM51V17805B/BSL

2,097,152-Word × 8-Bit DYNAMIC RAM : FAST PAGE MODE TYPE WITH EDO

DESCRIPTION

The MSM51V17805B/BSL is a 2,097,152-word × 8-bit dynamic RAM fabricated in Oki's silicon-gate CMOS technology. The MSM51V17805B/BSL achieves high integration, high-speed operation, and low-power consumption because Oki manufactures the device in a quadruple-layer polysilicon/double-layer metal CMOS process. The MSM51V17805B/BSL is available in a 28-pin plastic SOJ or 28-pin plastic TSOP. The MSM51V17805BSL (the self-refresh version) is specially designed for lower-power applications.

FEATURES

- 2,097,152-word × 8-bit configuration
- Single 3.3 V power supply, ±0.3 V tolerance
- Input : LVTTTL compatible, low input capacitance
- Output : LVTTTL compatible, 3-state
- Refresh : 2048 cycles/32 ms, 2048 cycles/128 ms (SL version)
- Fast page mode with EDO, read modify write capability
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, hidden refresh, $\overline{\text{RAS}}$ -only refresh capability
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self-refresh capability (SL version)
- Multi-bit test mode capability
- Package options:

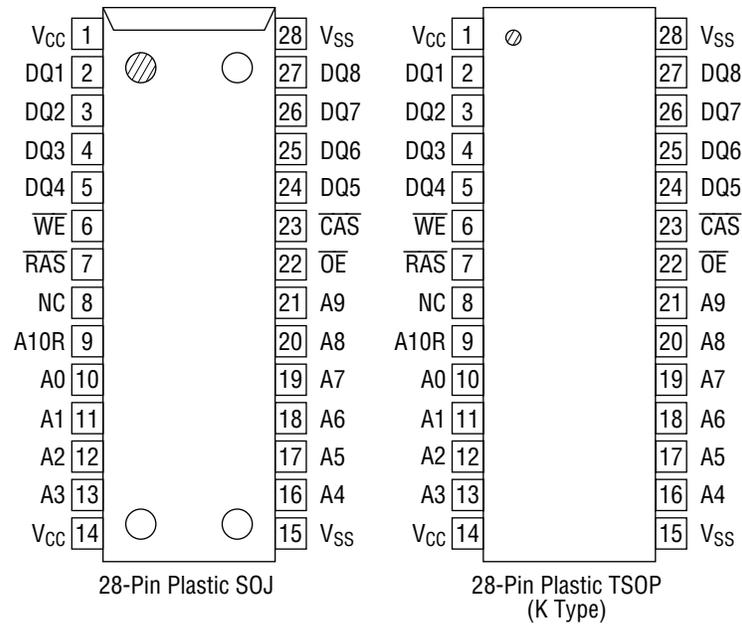
28-pin 400 mil plastic SOJ	(SOJ28-P-400-1.27)	(Product : MSM51V17805B/BSL-xxJS)
28-pin 400 mil plastic TSOP	(TSOPII28-P-400-1.27-K)	(Product : MSM51V17805B/BSL-xxTS-K)

 xx indicates speed rank.

PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t _{RAC}	t _{AA}	t _{CAC}	t _{OEA}		Operating (Max.)	Standby (Max.)
MSM51V17805B/BSL-50	50 ns	25 ns	13 ns	13 ns	84 ns	540 mW	1.8 mW/ 0.72 mW (SL version)
MSM51V17805B/BSL-60	60 ns	30 ns	15 ns	15 ns	104 ns	468 mW	
MSM51V17805B/BSL-70	70 ns	35 ns	20 ns	20 ns	124 ns	396 mW	

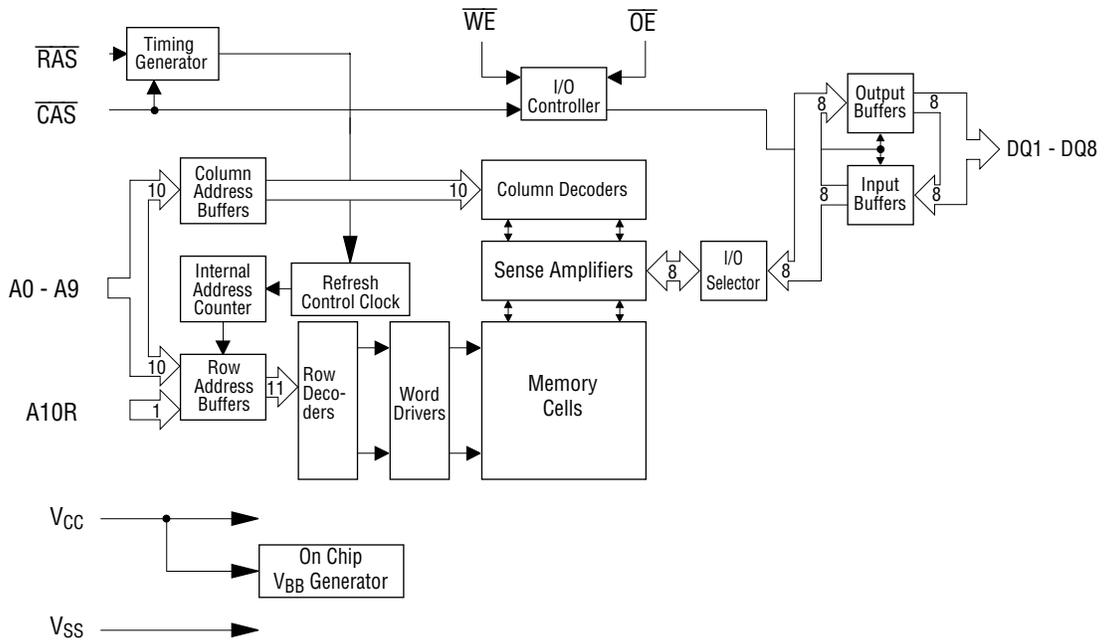
PIN CONFIGURATION (TOP VIEW)



Pin Name	Function
A0 - A9, A10R	Address Input
\overline{RAS}	Row Address Strobe
\overline{CAS}	Column Address Strobe
DQ1 - DQ8	Data Input/Data Output
\overline{OE}	Output Enable
\overline{WE}	Write Enable
V _{CC}	Power Supply (3.3 V)
V _{SS}	Ground (0 V)

Note : The same power supply voltage must be provided to every V_{CC} pin, and the same GND voltage level must be provided to every V_{SS} pin.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS**Absolute Maximum Ratings**

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V _{SS}	V _T	-0.5 to 4.6	V
Short Circuit Output Current	I _{OS}	50	mA
Power Dissipation	P _D *	1	W
Operating Temperature	T _{opr}	0 to 70	°C
Storage Temperature	T _{stg}	-55 to 150	°C

*: T_a = 25°C**Recommended Operating Conditions**(T_a = 0°C to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V _{CC}	3.0	3.3	3.6	V
	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.0	—	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.3	—	0.8	V

Capacitance(V_{CC} = 3.3 V ±0.3 V, T_a = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A9, A10R)	C _{IN1}	—	5	pF
Input Capacitance ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$)	C _{IN2}	—	7	pF
Output Capacitance (DQ1 - DQ8)	C _{I/O}	—	7	pF

DC Characteristics

(V_{CC} = 3.3 V ±0.3 V, T_a = 0°C to 70°C)

Parameter	Symbol	Condition	MSM51V17805 B/BSL-50		MSM51V17805 B/BSL-60		MSM51V17805 B/BSL-70		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
			Output High Voltage	V _{OH}	I _{OH} = -2.0 mA	2.4	V _{CC}	2.4		
Output Low Voltage	V _{OL}	I _{OL} = 2.0 mA	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	I _{LI}	0 V ≤ V _I ≤ V _{CC} + 0.3 V; All other pins not under test = 0 V	-10	10	-10	10	-10	10	μA	
Output Leakage Current	I _{LO}	DQ disable 0 V ≤ V _O ≤ V _{CC}	-10	10	-10	10	-10	10	μA	
Average Power Supply Current (Operating)	I _{CC1}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycling, t _{RC} = Min.	—	150	—	130	—	110	mA	1, 2
Power Supply Current (Standby)	I _{CC2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}} = V_{IH}$	—	2	—	2	—	2	mA	1
		$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ ≥ V _{CC} - 0.2 V	—	0.5	—	0.5	—	0.5	μA	1, 5
			—	200	—	200	—	200	μA	
Average Power Supply Current ($\overline{\text{RAS}}$ -only Refresh)	I _{CC3}	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}} = V_{IH}$, t _{RC} = Min.	—	150	—	130	—	110	mA	1, 2
Power Supply Current (Standby)	I _{CC5}	$\overline{\text{RAS}} = V_{IH}$, $\overline{\text{CAS}} = V_{IL}$, DQ = enable	—	5	—	5	—	5	mA	1
Average Power Supply Current ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	I _{CC6}	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$	—	150	—	130	—	110	mA	1, 2
Average Power Supply Current (Fast Page Mode)	I _{CC7}	$\overline{\text{RAS}} = V_{IL}$, $\overline{\text{CAS}}$ cycling, t _{HPC} = Min.	—	150	—	130	—	110	mA	1, 3
Average Power Supply Current (Battery Backup)	I _{CC10}	t _{RC} = 62.5 μs, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$, t _{RAS} ≤ 1 μs	—	300	—	300	—	300	μA	1, 4, 5
Average Power Supply Current ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self-Refresh)	I _{CC8}	$\overline{\text{RAS}} \leq 0.2$ V, $\overline{\text{CAS}} \leq 0.2$ V	—	300	—	300	—	300	μA	1, 5

- Notes :
1. I_{CC} Max. is specified as I_{CC} for output open condition.
 2. The address can be changed once or less while $\overline{\text{RAS}} = V_{IL}$.
 3. The address can be changed once or less while $\overline{\text{CAS}} = V_{IH}$.
 4. V_{CC} - 0.2 V ≤ V_{IH} ≤ V_{CC} + 0.3 V, -0.3 V ≤ V_{IL} ≤ 0.2 V.
 5. SL version.

AC Characteristics (1/2)

(V_{CC} = 3.3 V ±0.3 V, T_a = 0°C to 70°C) Note 1, 2, 3, 12, 13

Parameter	Symbol	MSM51V17805 B/BSL-50		MSM51V17805 B/BSL-60		MSM51V17805 B/BSL-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
		Random Read or Write Cycle Time	t _{RC}	84	—	104	—		
Read Modify Write Cycle Time	t _{RWC}	110	—	135	—	160	—	ns	
Fast Page Mode Cycle Time	t _{HPC}	20	—	25	—	30	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t _{HPRWC}	58	—	68	—	78	—	ns	
Access Time from $\overline{\text{RAS}}$	t _{RAC}	—	50	—	60	—	70	ns	4, 5, 6
Access Time from $\overline{\text{CAS}}$	t _{CAC}	—	13	—	15	—	20	ns	4, 5
Access Time from Column Address	t _{AA}	—	25	—	30	—	35	ns	4, 6
Access Time from $\overline{\text{CAS}}$ Precharge	t _{CPA}	—	30	—	35	—	40	ns	4
Access Time from $\overline{\text{OE}}$	t _{OEA}	—	13	—	15	—	20	ns	4
Output Low Impedance Time from $\overline{\text{CAS}}$	t _{CLZ}	0	—	0	—	0	—	ns	4
Data Output Hold After $\overline{\text{CAS}}$ Low	t _{DOH}	5	—	5	—	5	—	ns	
$\overline{\text{CAS}}$ to Data Output Buffer Turn-off Delay Time	t _{CEZ}	0	13	0	15	0	20	ns	7, 8
$\overline{\text{RAS}}$ to Data Output Buffer Turn-off Delay Time	t _{REZ}	0	13	0	15	0	20	ns	7, 8
$\overline{\text{OE}}$ to Data Output Buffer Turn-off Delay Time	t _{OEZ}	0	13	0	15	0	20	ns	7
$\overline{\text{WE}}$ to Data Output Buffer Turn-off Delay Time	t _{WEZ}	0	13	0	15	0	20	ns	7
Transition Time	t _T	1	50	1	50	1	50	ns	3
Refresh Period	t _{REF}	—	32	—	32	—	32	ms	
Refresh Period (SL version)	t _{REF}	—	128	—	128	—	128	ms	14
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	30	—	40	—	50	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RAS}	50	10,000	60	10,000	70	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode with EDO)	t _{RASP}	50	100,000	60	100,000	70	100,000	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	7	—	10	—	13	—	ns	
$\overline{\text{RAS}}$ Hold Time referenced to $\overline{\text{OE}}$	t _{ROH}	7	—	10	—	13	—	ns	
$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode with EDO)	t _{CP}	7	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	7	10,000	10	10,000	13	10,000	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	35	—	40	—	45	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	5	—	5	—	5	—	ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	30	—	35	—	40	—	ns	
$\overline{\text{OE}}$ Hold Time from $\overline{\text{CAS}}$ (DQ Disable)	t _{CHO}	5	—	5	—	5	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	11	37	14	45	14	50	ns	5
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	9	25	12	30	12	35	ns	6
Row Address Set-up Time	t _{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t _{RAH}	7	—	10	—	10	—	ns	
Column Address Set-up Time	t _{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t _{CAH}	7	—	10	—	13	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t _{RAL}	25	—	30	—	35	—	ns	

AC Characteristics (2/2)

(V_{CC} = 3.3 V ±0.3 V, T_a = 0°C to 70°C) Note 1, 2, 3, 12, 13

Parameter	Symbol	MSM51V17805 B/BSL-50		MSM51V17805 B/BSL-60		MSM51V17805 B/BSL-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
		Read Command Set-up Time	t _{RCS}	0	—	0	—		
Read Command Hold Time	t _{RCH}	0	—	0	—	0	—	ns	9
Read Command Hold Time referenced to $\overline{\text{RAS}}$	t _{RRH}	0	—	0	—	0	—	ns	9
Write Command Set-up Time	t _{WCS}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t _{WCH}	7	—	10	—	13	—	ns	
Write Command Pulse Width	t _{WP}	7	—	10	—	10	—	ns	
$\overline{\text{WE}}$ Pulse Width (DQ Disable)	t _{WPE}	7	—	10	—	10	—	ns	
$\overline{\text{OE}}$ Command Hold Time	t _{OEH}	7	—	10	—	13	—	ns	
$\overline{\text{OE}}$ Precharge Time	t _{OEP}	7	—	10	—	10	—	ns	
$\overline{\text{OE}}$ Command Hold Time	t _{OCH}	7	—	10	—	10	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t _{RWL}	7	—	10	—	13	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t _{CWL}	7	—	10	—	13	—	ns	
Data-in Set-up Time	t _{DS}	0	—	0	—	0	—	ns	11
Data-in Hold Time	t _{DH}	7	—	10	—	13	—	ns	11
$\overline{\text{OE}}$ to Data-in Delay Time	t _{OED}	13	—	15	—	20	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{CWD}	30	—	34	—	44	—	ns	10
Column Address to $\overline{\text{WE}}$ Delay Time	t _{AWD}	42	—	49	—	59	—	ns	10
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{RWD}	67	—	79	—	94	—	ns	10
$\overline{\text{CAS}}$ Precharge $\overline{\text{WE}}$ Delay Time	t _{CPWD}	47	—	54	—	64	—	ns	10
$\overline{\text{CAS}}$ Active Delay Time from $\overline{\text{RAS}}$ Precharge	t _{RPC}	5	—	5	—	5	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Set-up Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t _{CSR}	5	—	5	—	5	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t _{CHR}	10	—	10	—	10	—	ns	
$\overline{\text{WE}}$ to $\overline{\text{RAS}}$ Precharge Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t _{WRP}	10	—	10	—	10	—	ns	
$\overline{\text{WE}}$ Hold Time from $\overline{\text{RAS}}$ ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t _{WRH}	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Set-up Time (Test Mode)	t _{WTS}	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Hold Time (Test Mode)	t _{WTH}	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ Pulse Width ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self-Refresh)	t _{RASS}	100	—	100	—	100	—	μs	14
$\overline{\text{RAS}}$ Precharge Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self-Refresh)	t _{RPS}	90	—	110	—	130	—	ns	14
$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self-Refresh)	t _{CHS}	-50	—	-50	—	-50	—	ns	14

- Notes:
1. A start-up delay of $200\ \mu\text{s}$ is required after power-up, followed by a minimum of eight initialization cycles ($\overline{\text{RAS}}$ -only refresh or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh) before proper device operation is achieved.
 2. The AC characteristics assume $t_T = 2\ \text{ns}$.
 3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring input timing signals. Transition times (t_T) are measured between V_{IH} and V_{IL} .
 4. This parameter is measured with a load circuit equivalent to 1 TTL load and 100 pF. The output timing reference levels are $V_{OH} = 2.0\ \text{V}$ and $V_{OL} = 0.8\ \text{V}$.
 5. Operation within the t_{RCD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then the access time is controlled by t_{CAC} .
 6. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, then the access time is controlled by t_{AA} .
 7. t_{CEZ} (Max.), t_{REZ} (Max.), t_{WEZ} (Max.) and t_{OEZ} (Max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
 8. t_{CEZ} and t_{REZ} must be satisfied for open circuit condition.
 9. t_{RCH} or t_{RRH} must be satisfied for a read cycle.
 10. t_{WCS} , t_{CWD} , t_{RWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{\text{WCS}} \geq t_{\text{WCS}}$ (Min.), then the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If $t_{\text{CWD}} \geq t_{\text{CWD}}$ (Min.), $t_{\text{RWD}} \geq t_{\text{RWD}}$ (Min.), $t_{\text{AWD}} \geq t_{\text{AWD}}$ (Min.) and $t_{\text{CPWD}} \geq t_{\text{CPWD}}$ (Min.), then the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, then the condition of the data out (at access time) is indeterminate.
 11. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in an early write cycle, and to the $\overline{\text{WE}}$ leading edge in an $\overline{\text{OE}}$ control write cycle, or a read modify write cycle.
 12. The test mode is initiated by performing a $\overline{\text{WE}}$ and $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle. This mode is latched and remains in effect until the exit cycle is generated. The test mode specified in this data sheet is a 2-bit parallel test function. CA9 is not used. In a read cycle, if all internal bits are equal, the DQ pin will indicate a high level. If any internal bits are not equal, the DQ pin will indicate a low level. The test mode is cleared and the memory device returned to its normal operating state by performing a $\overline{\text{RAS}}$ -only refresh cycle or a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle.
 13. In a test mode read cycle, the value of access time parameters is delayed for 5 ns for the specified value. These parameters should be specified in test mode cycle by adding the above value to the specified value in this data sheet.
 14. Only SL version.

See ADDENDUM O for AC Timing Waveforms