

OKI Semiconductor

MSM51V17405A

4,194,304-Word × 4-Bit DYNAMIC RAM : FAST PAGE MODE TYPE WITH EDO

Preliminary

DESCRIPTION

The MSM51V17405A is a 4,194,304-word × 4-bit dynamic RAM fabricated in OKI's CMOS silicon gate technology. The MSM51V17405A achieves high integration, high-speed operation, and low-power consumption due to quadruple polysilicon double metal CMOS. The MSM51V17405A is available in a 26/24-pin plastic SOJ or 26/24-pin plastic TSOP.

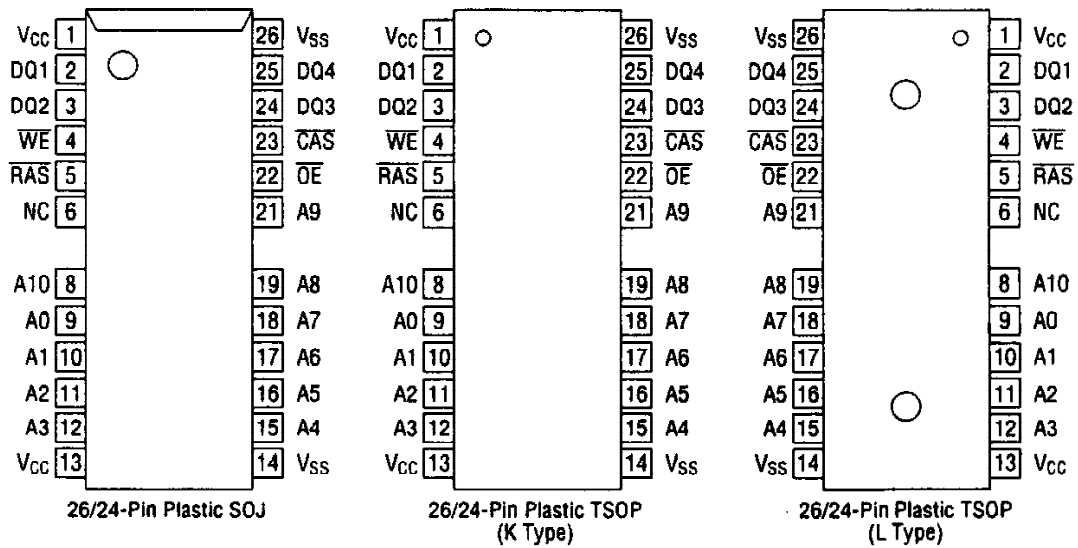
FEATURES

- 4,194,304-word × 4-bit configuration
- Single 3.3 V power supply, ±0.3 V tolerance
- Input : LVTTTL compatible, low input capacitance
- Output : LVTTTL compatible, 3-state
- Refresh : 2048 cycles/32 ms
- Fast page mode with EDO, read modify write capability
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, hidden refresh, $\overline{\text{RAS}}$ -only refresh capability
- Multi-bit test mode capability
- Package options:
 - 26/24-Pin 300 mil plastic SOJ (SOJ26/24-P-300) (Product : MSM51V17405A-xxSJ)
 - 26/24-Pin 300 mil plastic TSOP (TSOP26/24-P-300-K) (Product : MSM51V17405A-xxTS-K)
 - (TSOP26/24-P-300-L) (Product : MSM51V17405A-xxTS-L)xx indicates speed rank.

PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t _{RAC}	t _{AA}	t _{CAC}	t _{OE}		Operating (Max.)	Standby (Max.)
MSM51V17405A-60	60 ns	30 ns	15 ns	15 ns	110 ns	432 mW	3.6 mW
MSM51V17405A-70	70 ns	35 ns	20 ns	20 ns	130 ns	396 mW	
MSM51V17405A-80	80 ns	40 ns	20 ns	20 ns	150 ns	360 mW	

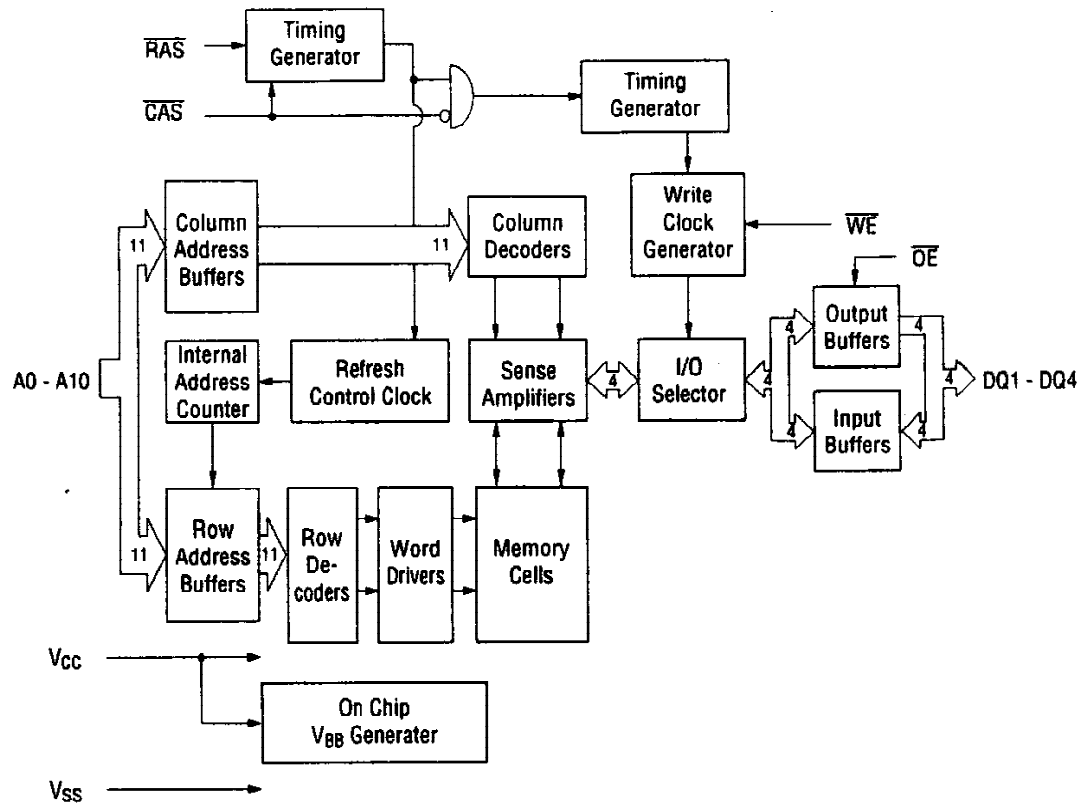
PIN CONFIGURATION (TOP VIEW)



Pin Name	Function
A0 - A10	Address Input
RAS	Row Address Strobe
CAS	Column Address Strobe
DQ1 - DQ4	Data Input/Data Output
OE	Output Enable
WE	Write Enable
V _{CC}	Power Supply (3.3 V)
V _{SS}	Ground (0 V)
NC	No Connection

Note : The same power supply voltage must be provided to every V_{CC} pin, and the same GND voltage level must be provided to every V_{SS} pin.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS**Absolute Maximum Ratings**

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	-0.5 to 4.6	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_D^*	1	W
Operating Temperature	T_{opr}	0 to 70	°C
Storage Temperature	T_{stg}	-55 to 150	°C

*: $T_a = 25^\circ\text{C}$ **Recommended Operating Conditions** $(T_a = 0^\circ\text{C to } 70^\circ\text{C})$

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	3.0	3.3	3.6	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	—	$V_{CC} + 0.3$	V
Input Low Voltage	V_{IL}	-0.3	—	0.8	V

Capacitance $(V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}, T_a = 25^\circ\text{C}, f = 1 \text{ MHz})$

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A10)	C_{IN1}	—	6	pF
Input Capacitance (RAS, CAS, WE, OE)	C_{IN2}	—	7	pF
Output Capacitance (DQ1 - DQ4)	$C_{I/O}$	—	10	pF

DC Characteristics

($V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $T_a = 0^\circ\text{C}$ to 70°C)

Parameter	Symbol	Condition	MSM51V17405 A-60		MSM51V17405 A-70		MSM51V17405 A-80		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	V_{OH}	$I_{OH} = -2.0 \text{ mA}$	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	$I_{OL} = 2.0 \text{ mA}$	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	I_{LI}	$0 \text{ V} \leq V_i \leq V_{CC} + 0.3 \text{ V}$; All other pins not under test = 0 V	-10	10	-10	10	-10	10	μA	
Output Leakage Current	I_{LO}	DQ disable $0 \text{ V} \leq V_O \leq 3.6 \text{ V}$	-10	10	-10	10	-10	10	μA	
Average Power Supply Current (Operating)	I_{CC1}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycling, $t_{RC} = \text{Min.}$	—	120	—	110	—	100	mA	1, 2
Power Supply Current (Standby)	I_{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} = V_{IH}$	—	2	—	2	—	2	mA	1
		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{CC} - 0.2 \text{ V}$	—	1	—	1	—	1		
Average Power Supply Current ($\overline{\text{RAS}}$ -only Refresh)	I_{CC3}	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}} = V_{IH}$, $t_{RC} = \text{Min.}$	—	120	—	110	—	100	mA	1, 2
Power Supply Current (Standby)	I_{CC5}	$\overline{\text{RAS}} = V_{IH}$, $\overline{\text{CAS}} = V_{IL}$, DQ = enable	—	5	—	5	—	5	mA	1
Average Power Supply Current ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	I_{CC6}	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$	—	120	—	110	—	100	mA	1, 2
Average Power Supply Current (Fast Page Mode)	I_{CC7}	$\overline{\text{RAS}} = V_{IL}$, $\overline{\text{CAS}}$ cycling, $t_{PC} = \text{Min.}$	—	140	—	130	—	120	mA	1, 3

- Notes :
1. I_{CC} Max. is specified as I_{CC} for output open condition.
 2. Address can be changed once or less while $\overline{\text{RAS}} = V_{IL}$.
 3. Address can be changed once or less while $\overline{\text{CAS}} = V_{IH}$.

AC Characteristics (1/2)

(V_{CC} = 3.3 V ±0.3 V, T_a = 0°C to 70°C) Note 1, 2, 3, 12, 13

Parameter	Symbol	MSM51V17405 A-60		MSM51V17405 A-70		MSM51V17405 A-80		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t _{RC}	110	—	130	—	150	—	ns	
Read Modify Write Cycle Time	t _{RWC}	155	—	185	—	205	—	ns	
Fast Page Mode Cycle Time	t _{HPC}	25	—	30	—	35	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t _{PRWC}	85	—	100	—	105	—	ns	
Access Time from $\overline{\text{RAS}}$	t _{RAC}	—	60	—	70	—	80	ns	4, 5, 6
Access Time from $\overline{\text{CAS}}$	t _{CAC}	—	15	—	20	—	20	ns	4, 5
Access Time from Column Address	t _{AA}	—	30	—	35	—	40	ns	4, 6
Access Time from $\overline{\text{CAS}}$ Precharge	t _{CPA}	—	35	—	40	—	45	ns	4
Access Time from $\overline{\text{OE}}$	t _{OEA}	—	15	—	20	—	20	ns	4
Output Low Impedance Time from $\overline{\text{CAS}}$	t _{CLZ}	0	—	0	—	0	—	ns	4
Data Output Hold After $\overline{\text{CAS}}$ Low	t _{DOH}	3	15	3	15	3	15	ns	
$\overline{\text{CAS}}$ to Data Output Buffer Turn-off Delay Time	t _{CEZ}	3	15	3	20	3	20	ns	7, 8
$\overline{\text{RAS}}$ to Data Output Buffer Turn-off Delay Time	t _{REZ}	3	15	3	20	3	20	ns	7, 8
$\overline{\text{OE}}$ to Data Output Buffer Turn-off Delay Time	t _{OEZ}	3	15	3	20	3	20	ns	7
$\overline{\text{WE}}$ to Data Output Buffer Turn-off Delay Time	t _{WEZ}	3	15	3	20	3	20	ns	7
Transition Time	t _T	2	50	2	50	2	50	ns	3
Refresh Period	t _{REF}	—	32	—	32	—	32	ms	
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	40	—	50	—	60	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode with EDO)	t _{RASP}	60	100,000	70	100,000	80	100,000	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	15	—	20	—	20	—	ns	
$\overline{\text{RAS}}$ Hold Time referenced to $\overline{\text{OE}}$	t _{ROH}	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode with EDO)	t _{CP}	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	10	10,000	10	10,000	15	10,000	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	40	—	45	—	50	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{RHCP}	35	—	40	—	45	—	ns	
$\overline{\text{OE}}$ Hold Time from $\overline{\text{CAS}}$ (DQ Disable)	t _{CHO}	5	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	20	45	20	50	20	60	ns	5
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	15	30	15	35	15	40	ns	6
$\overline{\text{RAS}}$ to Second $\overline{\text{CAS}}$ Delay Time	t _{RSCD}	60	—	70	—	80	—	ns	
Row Address Set-up Time	t _{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t _{RAH}	10	—	10	—	15	—	ns	
Column Address Set-up Time	t _{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t _{CAH}	10	—	15	—	15	—	ns	
Column Address Hold Time from $\overline{\text{RAS}}$	t _{AR}	40	—	45	—	50	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t _{RAL}	30	—	35	—	40	—	ns	

AC Characteristics (2/2)

(V_{CC} = 3.3 V ±0.3 V, T_a = 0°C to 70°C) Note 1, 2, 3, 12, 13

Parameter	Symbol	MSM51V17405 A-60		MSM51V17405 A-70		MSM51V17405 A-80		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Read Command Set-up Time	t _{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time	t _{RCH}	0	—	0	—	0	—	ns	9
Read Command Hold Time referenced to $\overline{\text{RAS}}$	t _{RRH}	0	—	0	—	0	—	ns	9
Write Command Set-up Time	t _{WCS}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t _{WCH}	10	—	15	—	15	—	ns	
Write Command Hold Time from $\overline{\text{RAS}}$	t _{WCR}	45	—	50	—	55	—	ns	
Write Command Pulse Width	t _{WP}	10	—	10	—	10	—	ns	
$\overline{\text{WE}}$ Pulse Width (DQ Disable)	t _{WPE}	5	—	10	—	10	—	ns	
$\overline{\text{OE}}$ Command Hold Time	t _{OEH}	15	—	20	—	20	—	ns	
$\overline{\text{OE}}$ Precharge Time	t _{OEP}	10	—	10	—	10	—	ns	
$\overline{\text{OE}}$ Command Hold Time	t _{OCH}	10	—	10	—	10	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t _{RWL}	15	—	20	—	20	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t _{CWL}	15	—	20	—	20	—	ns	
Data-in Set-up Time	t _{DS}	0	—	0	—	0	—	ns	11
Data-in Hold Time	t _{DH}	15	—	15	—	15	—	ns	11
Data-in Hold Time from $\overline{\text{RAS}}$	t _{DHR}	40	—	45	—	50	—	ns	
$\overline{\text{OE}}$ to Data-in Delay Time	t _{OED}	15	—	20	—	20	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{CWD}	40	—	50	—	50	—	ns	10
Column Address to $\overline{\text{WE}}$ Delay Time	t _{AWD}	55	—	65	—	70	—	ns	10
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{RWD}	85	—	100	—	110	—	ns	10
$\overline{\text{CAS}}$ Precharge $\overline{\text{WE}}$ Delay Time	t _{CPWD}	60	—	70	—	75	—	ns	10
$\overline{\text{CAS}}$ Active Delay Time from $\overline{\text{RAS}}$ Precharge	t _{APC}	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Set-up Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t _{CSR}	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t _{CHR}	20	—	20	—	20	—	ns	
$\overline{\text{CAS}}$ Precharge Time (Refresh Counter Test)	t _{CPT}	40	—	40	—	40	—	ns	
$\overline{\text{WE}}$ to $\overline{\text{RAS}}$ Precharge Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t _{WRP}	10	—	10	—	10	—	ns	
$\overline{\text{WE}}$ Hold Time from $\overline{\text{RAS}}$ ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t _{WRH}	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Set-up Time (Test Mode)	t _{WTS}	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Hold Time (Test Mode)	t _{WTH}	20	—	20	—	20	—	ns	

- Notes:
1. A start-up delay of 200 μ s is required after power-up, followed by a minimum of eight initialization cycles ($\overline{\text{RAS}}$ -only refresh or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh) before proper device operation is achieved.
 2. The AC characteristics assume $t_f = 5$ ns.
 3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring input timing signals. Transition times (t_T) are measured between V_{IH} and V_{IL} .
 4. This parameter is measured with a load circuit equivalent to 1 TTL load and 100 pF. Output timing reference levels are $V_{OH} = 2.0$ V and $V_{OL} = 0.8$ V.
 5. Operation within the t_{RCD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, access time is controlled by t_{CAC} .
 6. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, access time is controlled by t_{AA} .
 7. t_{CEZ} (Max.), t_{REZ} (Max.), t_{WEZ} (Max.) and t_{OEZ} (Max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
 8. t_{CEZ} and t_{REZ} must be satisfied for open circuit condition.
 9. t_{RCH} or t_{RRH} must be satisfied for a read cycle.
 10. t_{WCS} , t_{CWD} , t_{RWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (Min.), the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (Min.), $t_{RWD} \geq t_{RWD}$ (Min.), $t_{AWD} \geq t_{AWD}$ (Min.) and $t_{CPWD} \geq t_{CPWD}$ (Min.), the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
 11. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in an early write cycle, and to $\overline{\text{WE}}$ leading edge in an $\overline{\text{OE}}$ control write cycle or a read modify write cycle.
 12. The test mode is initiated by performing a $\overline{\text{WE}}$ and $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle. This mode is latched and remains in effect until the exit cycle is generated. In a test mode CA0, CA1 and CA10 are not used and each DQ pin now accesses 8-bit locations. Since all 4 DQ pins are used, a total of 32 data bits can be written in parallel into the memory array. In a read cycle, if 8 data bits are equal the DQ pin will indicate a high level. If the 8 data bits are not equal, the DQ pin will indicate a low level. The test mode is cleared and the memory device returned to its normal operating state by performing a $\overline{\text{RAS}}$ -only refresh cycle or a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle.
 13. In a test mode read cycle, the value of access time parameters is delayed for 5 ns for the specified value. These parameters should be specified in test mode cycle by adding the above value to the specified value in this data sheet.

See ADDENDUM L for AC Timing Waveforms