OKI Semiconductor

MSM51V17100

16,777,216-Word × 1-Bit DYNAMIC RAM : FAST PAGE MODE TYPE

DESCRIPTION

The MSM51V17100 is a new generation dynamic organized as 16,777,216-word × 1-bit.
The technology used to fabricate the MSM51V17100 is OKI's CMOS silicon gate process technology.
The device operates at a single 3.3V power supply. Its I/O pins are LVTTL compatible.

FEATURES

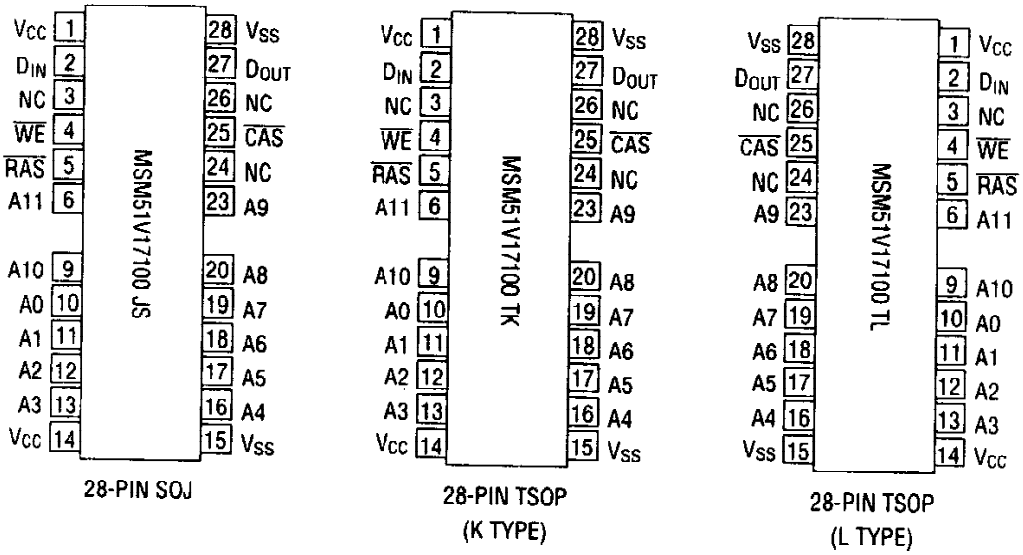
- Silicon gate, quadruple polysilicon CMOS, 1 transistor memory cell
- 16,777,216-word × 1-bit organization
- Single 3.3V power supply, ±10% tolerance
- Input: LVTTL compatible
- Output: LVTTL compatible, tristate
- Refresh: 2048 cycles/32ms
- Common I/O capability using "Early-Write" operation
- Fast Page Mode, Read Modify Write capability
- Read Modify Write capability
- $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh, $\overline{RAS}$ only refresh capability
- Fast Page Mode capability
- Multi bit test mode capability
- Package:

28-Pin 400mil	Plastic SOJ	(SOJ28-P-400)
28-Pin 400mil	Plastic TSOP	(TSOP28-P-400-K) (TSOP28-P-400-L)

PRODUCT FAMILY

Family	Access Time (Max.)			Cycle Time (Min.)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}		Operating (Max.)	Standby (Max.)
MSM51V17100 - 60	60ns	30ns	15ns	110ns	432mW	1.8mW
MSM51V17100 - 70	70ns	35ns	20ns	130ns	396mW	
MSM51V17100 - 80	80ns	40ns	20ns	150ns	360mW	

PIN CONFIGURATION (TOP VIEW)



28-PIN SOJ

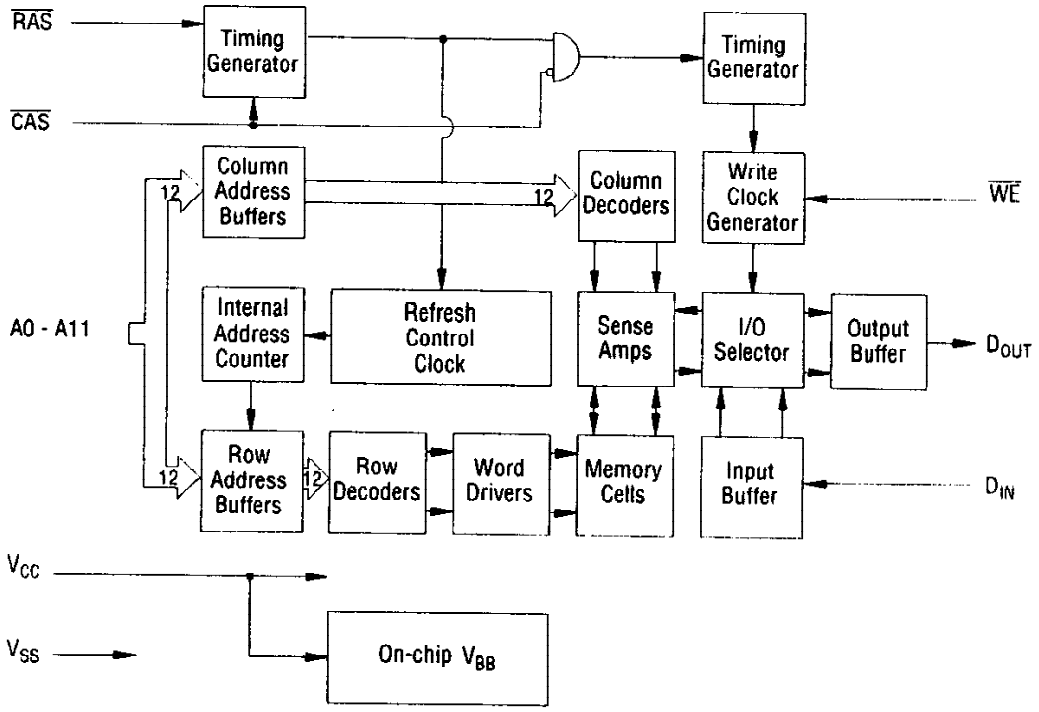
28-PIN TSOP (K TYPE)

28-PIN TSOP (L TYPE)

Pin Name	Function
A0 - A11	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{WE}$	Write Enable
V_{CC}	Power Supply (3.3V)
V_{SS}	Ground (0V)
NC	No Connection

Note: Same power supply voltage must be provided to every V_{CC} pin, and same GND voltage level must be provided to every V_{SS} pin.

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relativeto V_{SS}	V_T	-0.5 to 4.6	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_D*	1	W
Operating Temperature	T_{opr}	0 to 70	°C
Storage Temperature	T_{stg}	-55 to 150	°C

*: Ta = 25°C

Recommended Operating Conditions

(Ta = 0 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	3.0	3.3	3.6	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	—	0.8	V

Capacitance

(V_{CC} = 3.0 to 3.6V, Ta = 25°C, f = 1MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A11, D_{IN})	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	—	7	pF
Output Capacitance (D_{OUT})	C_{OUT}	—	7	pF

DC Characteristics

(V_{CC} = 3.0V to 3.6V, Ta = 0 to 70°C)

Parameter	Symbol	Condition	MSM 51V17100-60		MSM 51V17100-70		MSM 51V17100-80		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	V_{OH}	I_{OH} = −2.0mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	I_{OL} = 2.0mA	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	I_{LI}	0V < V_I < V_{CC} + 0.3V; All other pins not under test = 0V	−10	10	−10	10	−10	10	µA	
Output Leakage Current	I_{LO}	D_{OUT} = Disable 0V < V_O < 3.6V	−10	10	−10	10	−10	10	µA	
Average Power Supply Current (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = Min.	—	120	—	110	—	100	mA	1, 2
Power Supply Current (Standby)	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	—	2	—	2	—	2	mA	1
		$\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} −0.2V	—	0.5	—	0.5	—	0.5		
Average Power Supply Current ($\overline{RAS}$ Only Refresh)	I_{CC3}	$\overline{RAS}$ cycling $\overline{CAS}$ = V_{IH} t_{RC} = Min.	—	120	—	110	—	100	mA	1, 2
Power Supply Current (Standby)	I_{CC5}	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{OUT} = Enable	—	5	—	5	—	5	mA	1
Average Power Supply Current ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	I_{CC6}	$\overline{RAS}$ cycling $\overline{CAS}$ before $\overline{RAS}$	—	120	—	110	—	100	mA	1, 2
Average Power Supply Current (Fast Page Mode)	I_{CC7}	$\overline{RAS}$ = V_{IL} $\overline{CAS}$ cycling t_{PC} = Min.	—	110	—	100	—	90	mA	1, 3

Notes: 1. Specified values are obtained with the output open.
2. Address can be changed once or less while $\overline{RAS}$=V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$=V_{IH}.

AC Characteristics (1/2)

(V_{CC} = 3.0V to 3.6V, Ta = 0 to 70°C) Note 1, 2, 3, 10,11

Parameter	Symbol	MSM 51V17100-60		MSM 51V17100-70		MSM 51V17100-80		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	110	—	130	—	150	—	ns	
Read Modify Write Cycle Time	t_{RMW}	130	—	155	—	175	—	ns	
Fast Page Mode Cycle Time	t_{PC}	40	—	45	—	50	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t_{PRMW}	85	—	100	—	105	—	ns	
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	ns	4, 5, 6
Access Time from $\overline{CAS}$	t_{CAC}	—	15	—	20	—	20	ns	4, 5
Access Time from Column Address	t_{AA}	—	30	—	35	—	40	ns	4, 6
Access Time from $\overline{CAS}$ Precharge	t_{CPA}	—	35	—	40	—	45	ns	4
Output Low Impedance Time from $\overline{CAS}$	t_{CLZ}	0	—	0	—	0	—	ns	4
Output Buffer Turn-off Delay Time	t_{OFF}	0	15	0	20	0	20	ns	7
Transition Time	t_T	3	50	3	50	3	50	ns	3
Refresh Period	t_{REF}	—	32	—	32	—	32	ms	
$\overline{RAS}$ Precharge Time	t_{RP}	40	—	50	—	60	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15	—	20	—	20	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	20	60	ns	5
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	15	40	ns	6
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	10	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	15	—	ns	
Column Address Hold Time from $\overline{RAS}$	t_{AR}	50	—	55	—	60	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	40	—	ns	

AC Characteristics (2/2)

(V_{CC} = 3.0V to 3.6V, Ta = 0 to 70°C) Note 1, 2, 3, 10, 11

Parameter	Symbol	MSM 51V17100-60		MSM 51V17100-70		MSM 51V17100-80		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	ns	8
Read Command Hold Time Reference to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	ns	8
Write Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	9
Write Command Hold Time	t_{WCH}	10	—	15	—	15	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	10	—	ns	
Write Command Hold Time from $\overline{RAS}$	t_{WCR}	45	—	55	—	60	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	15	—	20	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	15	—	20	—	20	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	ns	12
Data-in Hold Time	t_{DH}	15	—	15	—	15	—	ns	12
Data-in Hold Time from $\overline{RAS}$	t_{DHR}	50	—	55	—	60	—	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	15	—	20	—	20	—	ms	9
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	30	—	35	—	40	—	ns	9
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	60	—	90	—	80	—	ns	9
$\overline{CAS}$ Precharge $\overline{WE}$ Delay Time	t_{CPWD}	35	—	40	—	45	—	ns	9
$\overline{CAS}$ Active Delay from $\overline{RAS}$ Precharge	t_{RPC}	10	—	10	—	10	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Set-up Time ($\overline{CAS}$ Before $\overline{RAS}$)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$)	t_{CHR}	20	—	20	—	20	—	ns	
$\overline{CAS}$ Precharge Time (Refresh Counter Test)	t_{CPT}	40	—	40	—	40	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ Before $\overline{RAS}$)	t_{WRP}	10	—	10	—	10	—	ns	
$\overline{WE}$ Hold Time from ($\overline{CAS}$ Before $\overline{RAS}$)	t_{WRH}	10	—	10	—	10	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Set-up Time (Test Mode)	t_{WSR}	10	—	10	—	10	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Hold Time (Test Mode)	t_{WHR}	20	—	20	—	20	—	ns	

Notes:

1. An initial pause of 200μs is required after power-up followed by a minimum of eight initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle) before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ initialization cycles is required.

2. The AC characteristics assume t_T = 5ns.

3. V_{IH}(Min.) and V_{IL}(Max.) are reference levels of input signals for timing measurement. Transition times (t_T) are measured between V_{IH} and V_{IL}.

4. Measured with a load circuit equivalent to 1 TLL load and 100pF. Output timing reference levels are V_{OH} = 2.0V and V_{OL} = 0.8V.

5. Operation within the t_{RCD}(Max.) limit insures that t_{RAC}(Max.) can be met. t_{RCD}(Max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(Max.) limit, then access time is controlled by t_{CAC}.

6. Operation within the t_{RAD}(Max.) limit insures that t_{RAC}(Max.) can be met. t_{RAD}(Max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD}(Max.) limit, then access time is controlled by t_{AA}.

7. t_{OFF}(Max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$(Min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle; if $t_{RWD} \geq t_{RWD}$(Min.), $t_{CWD} \geq t_{CWD}$(Min.), $t_{AWD} \geq t_{AWD}$(Min.), and $t_{CPWD} \geq t_{CPWD}$(Min.), the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

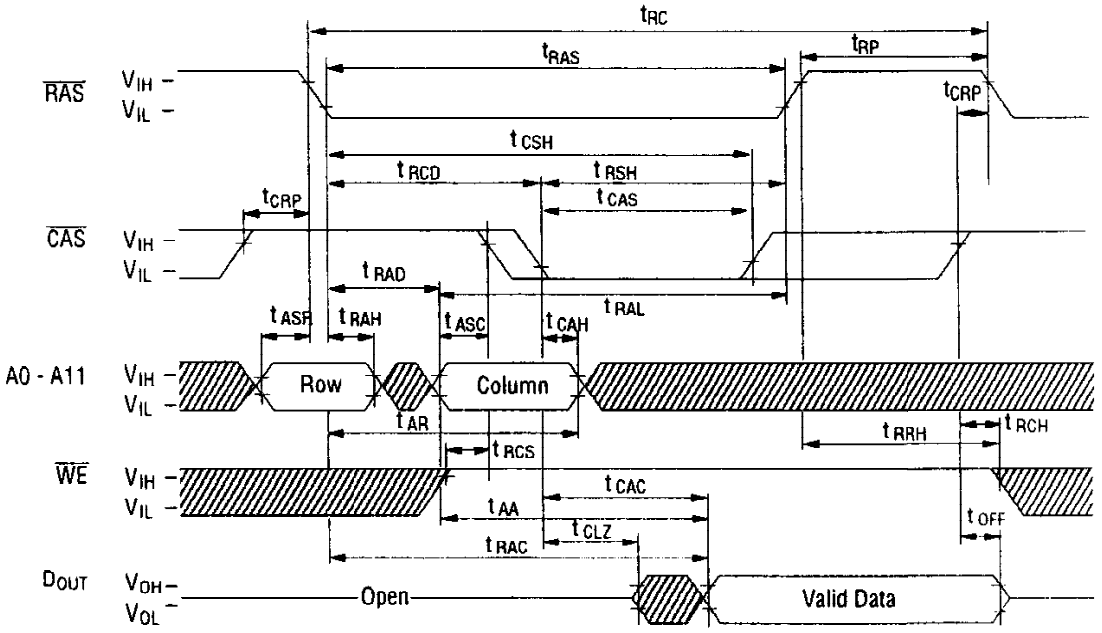
10. The test mode is initiated by performing a $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. This mode is latched and remain in effect until the exit cycle is generated. The test mode specified in this data sheet is 32-bit parallel test function. RA11, CA0, CA1, CA10 and CA11 are not used. In a read cycle, if all internal bits are equal, the data output pin will indicate a high level. If any internal bits are not equal, the data ouput pin will indicate a low level. The test mode is cleared and the memory device returned to its normal operational state by performing a $\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.

11. In a test mode read cycle, the value of access time parameters is delayed for 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to specified value in this data sheet.

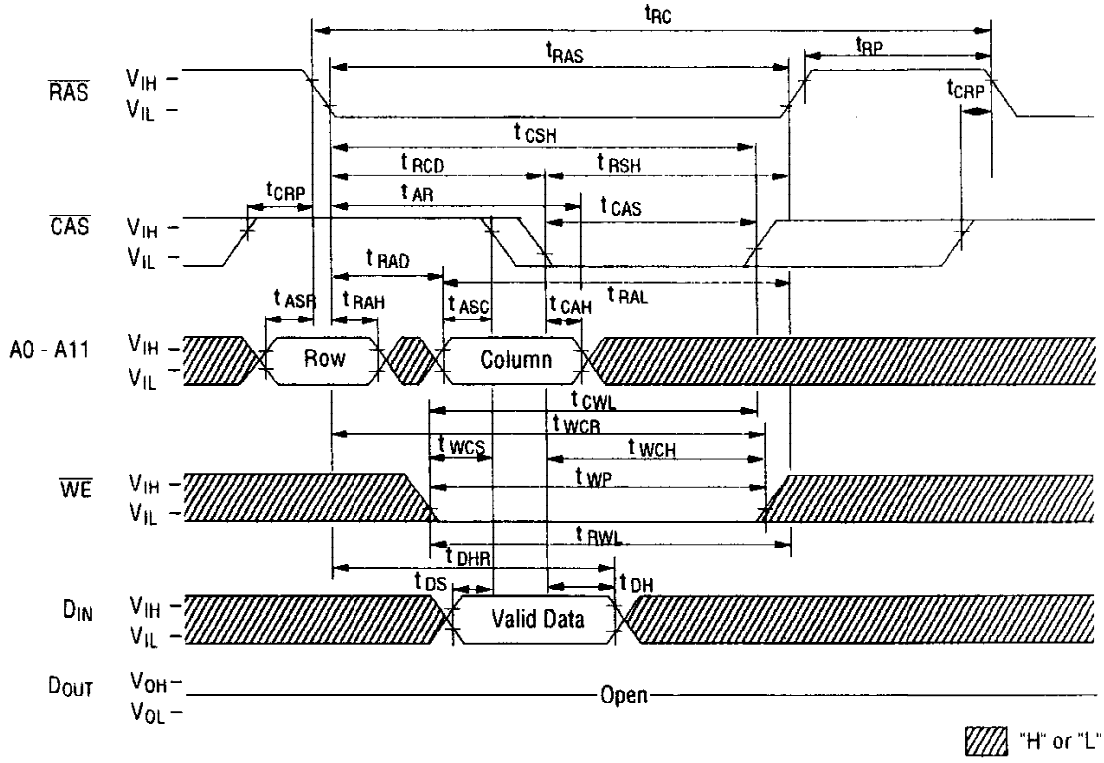
12. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle or to $\overline{WE}$ leading edge in a read modify write cycle.

TIMING WAVEFORM

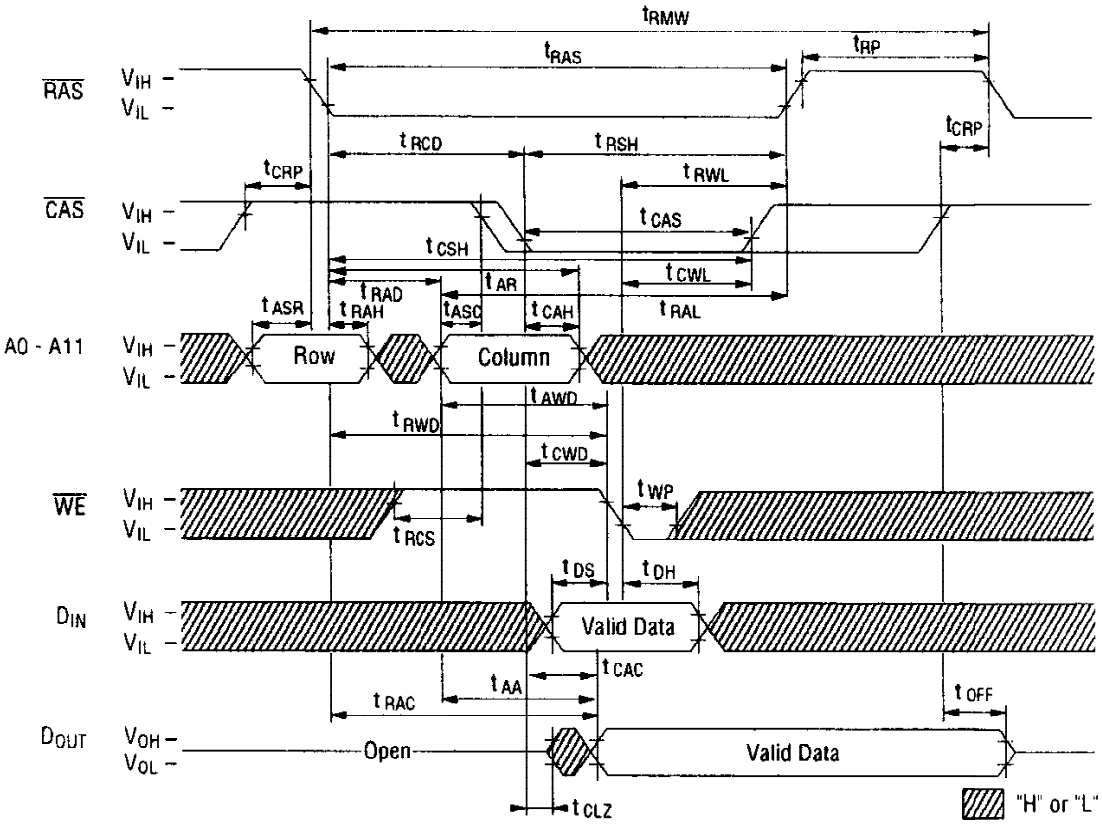
Read Cycle



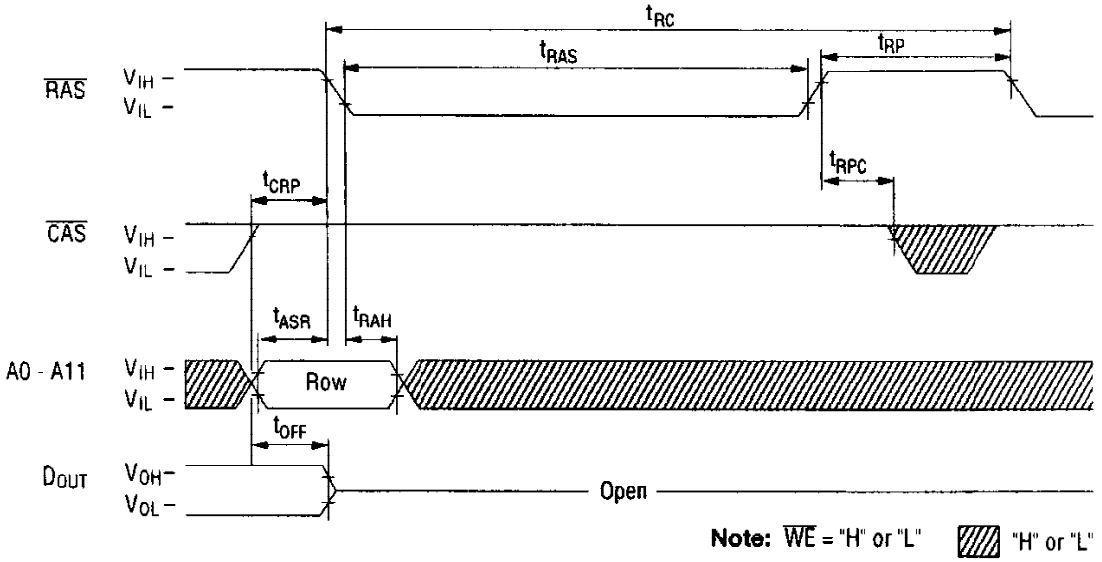
Early Write Cycle



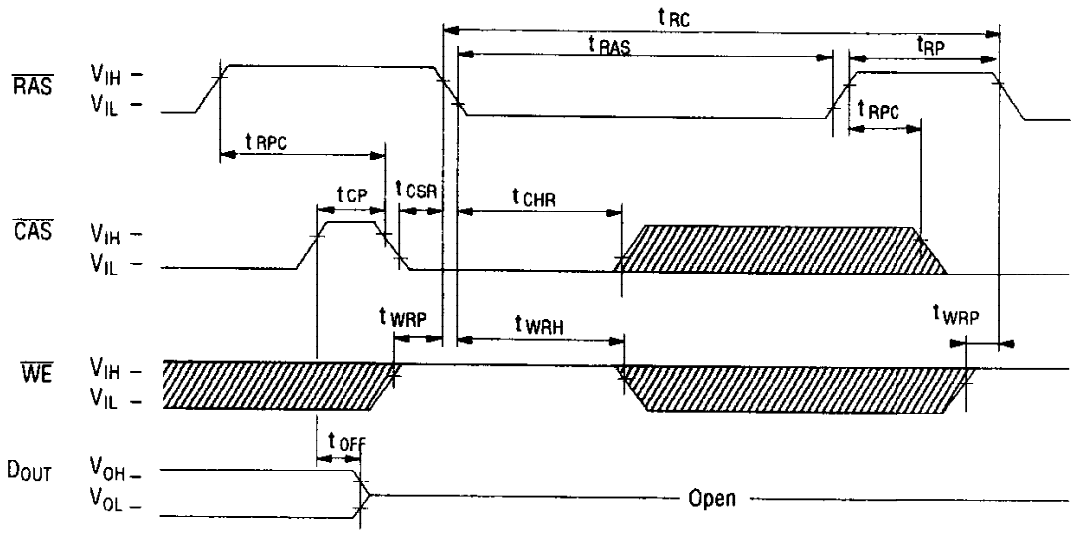
Read Modify Write Cycle



RAS Only Refresh Cycle

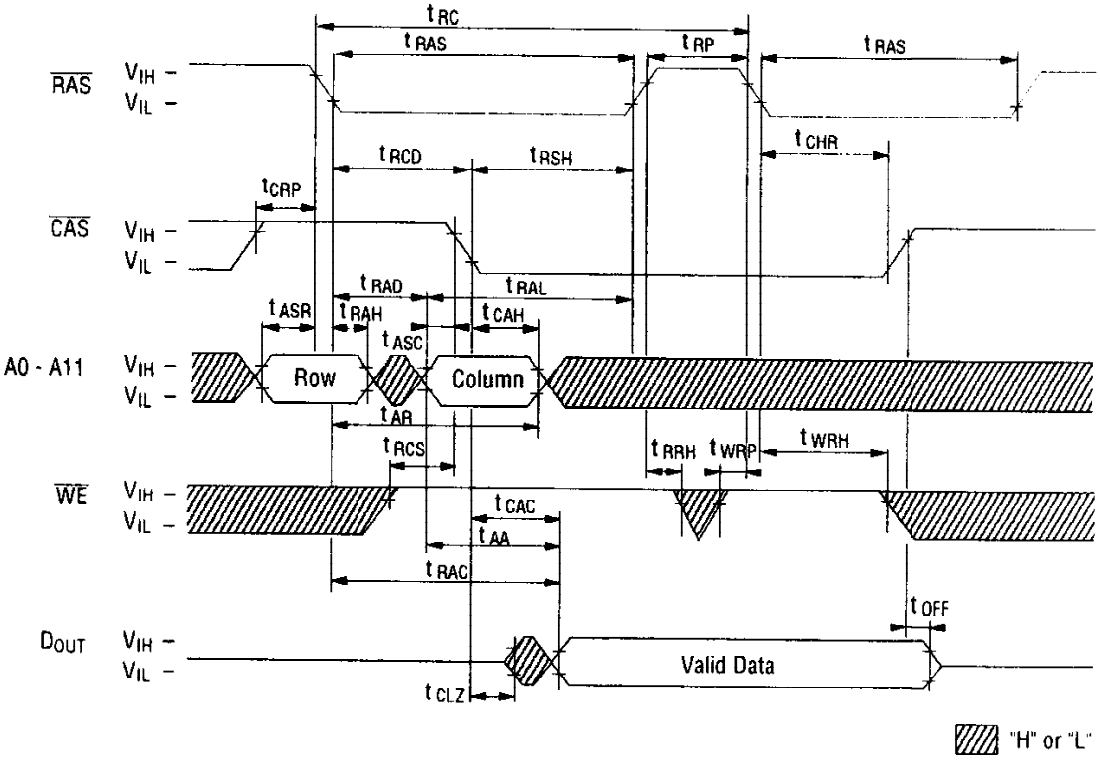


$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

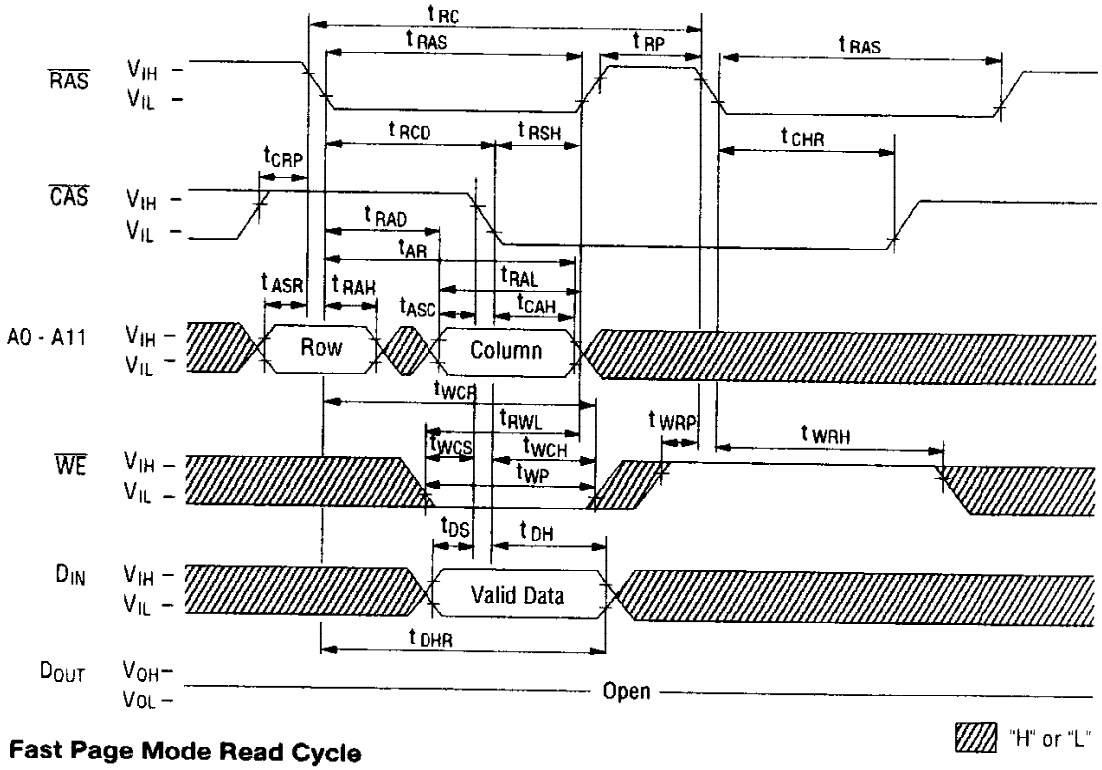


Note: A0 - A11 = "H" or "L" "H" or "L"

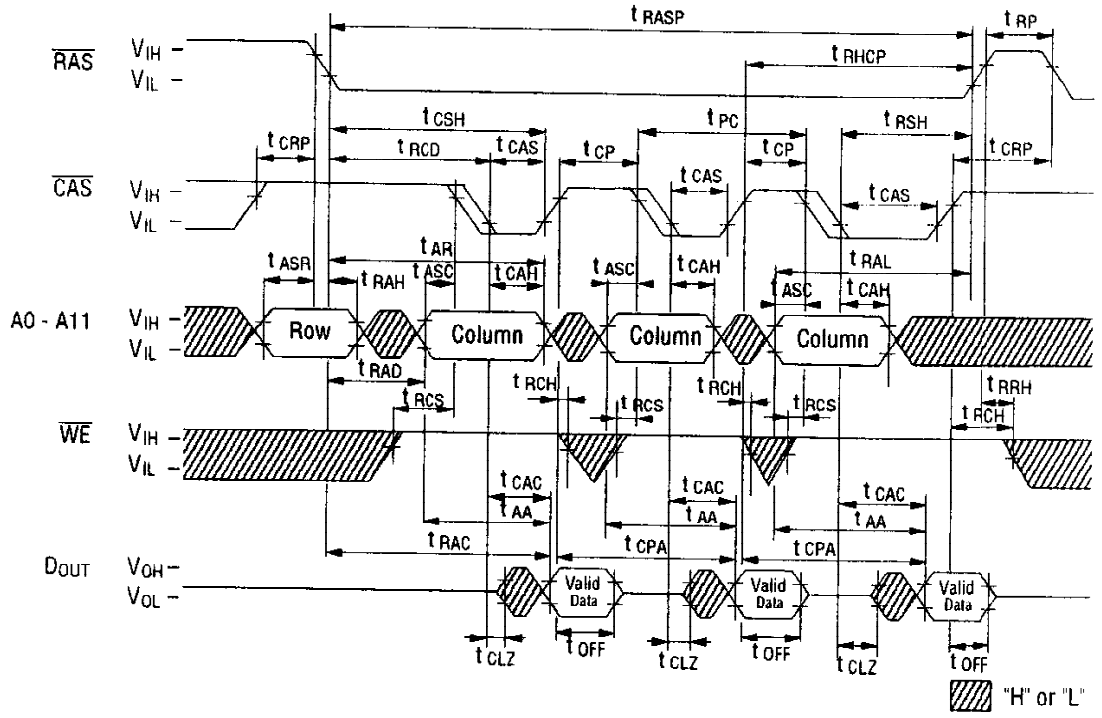
Hidden Refresh Read Cycle



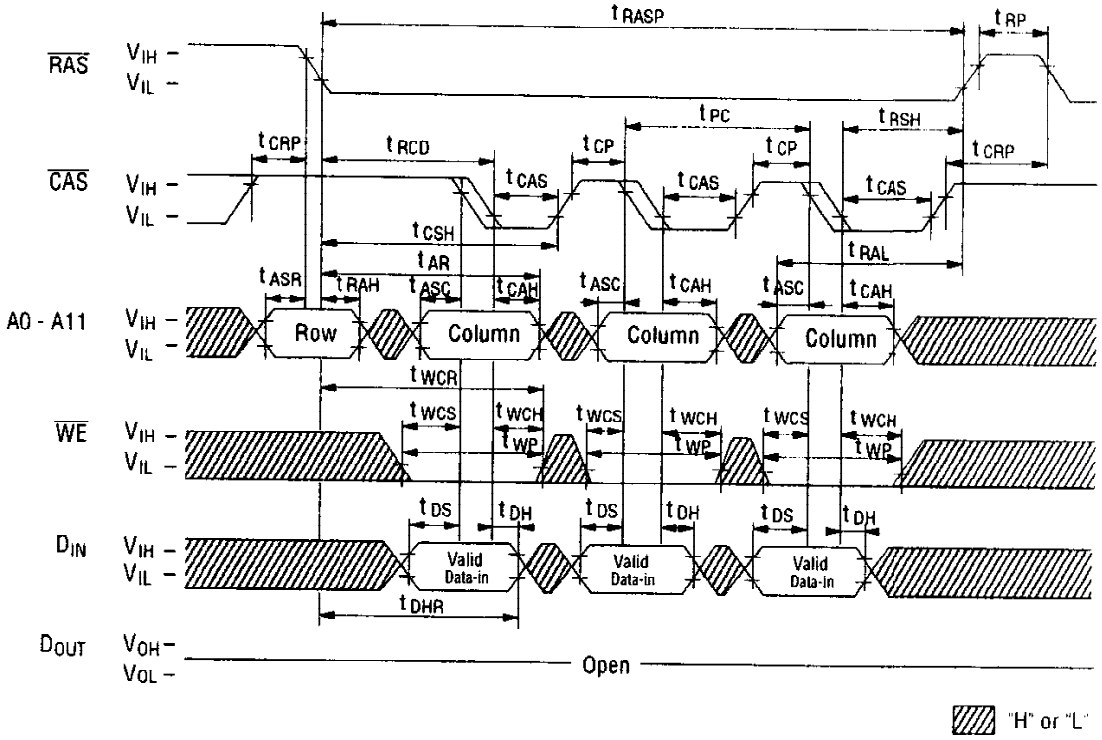
Hidden Refresh Write Cycle



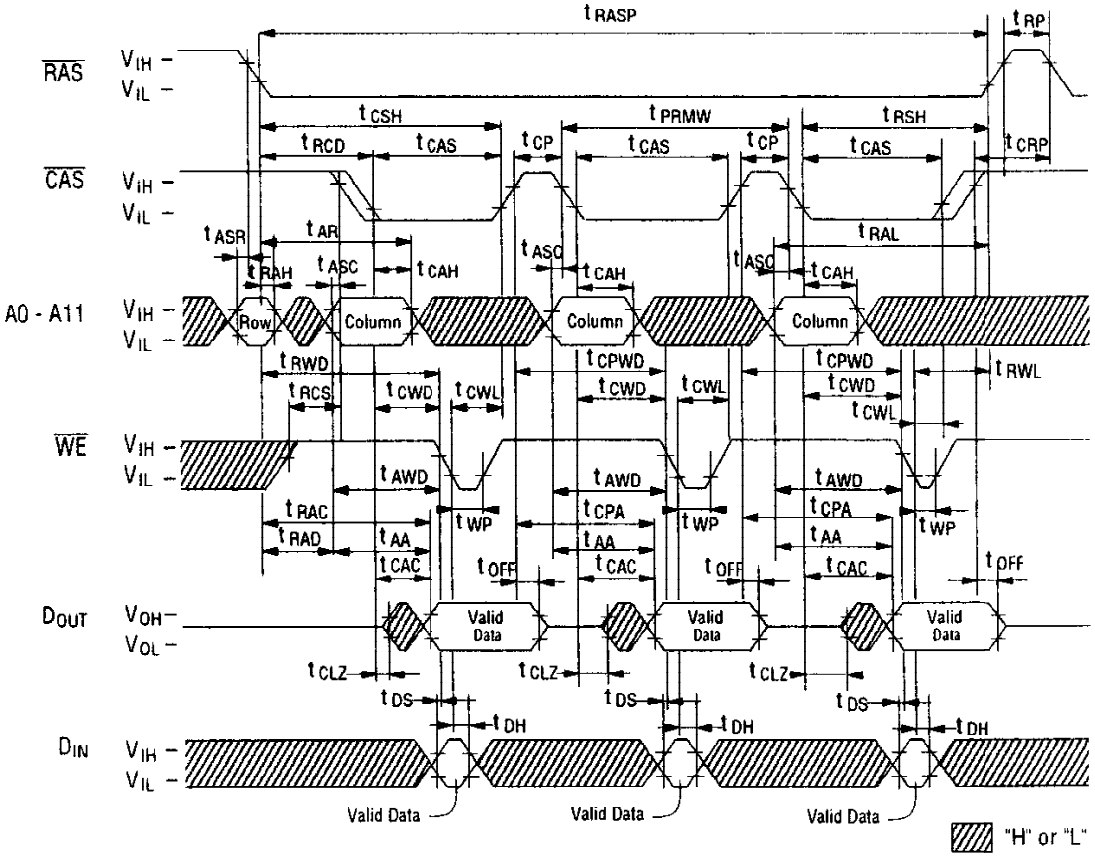
Fast Page Mode Read Cycle



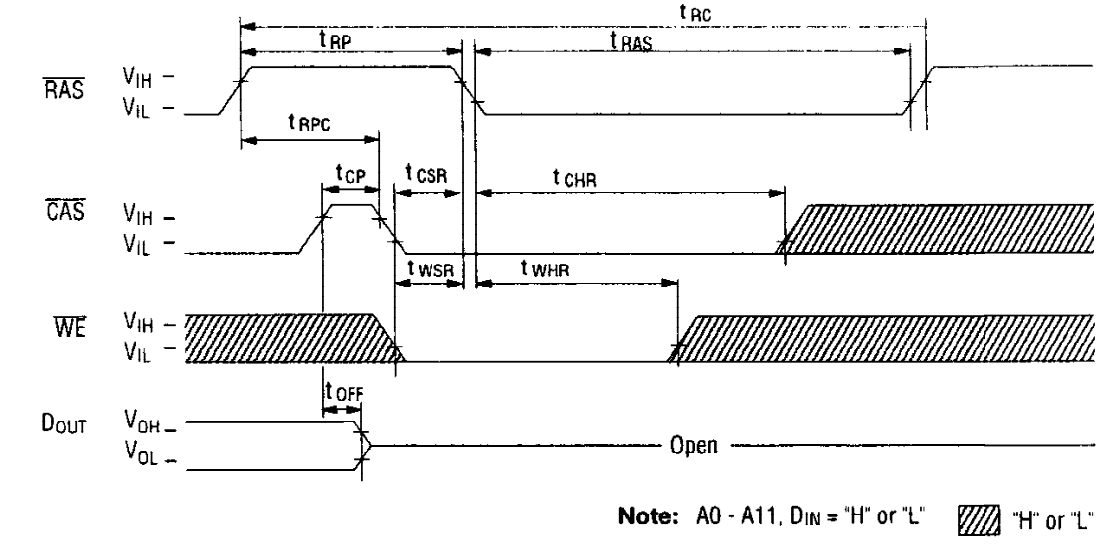
Fast Page Mode Write Cycle



Fast Page Mode Read Modify Write Cycle



Test Mode in Cycle



Note: A0 - A11, D_{IN} = "H" or "L" "H" or "L"

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Cycle