

OKI Semiconductor

MSM5117100

16 Meg x 1-Bit DYNAMIC RAM

Preliminary

DESCRIPTION

The MSM5117100 is a 16 Megabit dynamic memory organized as 16,777,216 word by 1 bit. The technology used to fabricate the MSM5117100 is OKI's CMOS silicon gate process technology. The device operates at a single + 5 V power supply. All inputs and outputs are TTL compatible. This 16-Meg DRAM can be used for high end PC's & work stations which need high density main memory.

FEATURES

- Silicon gate, quadruple polysilicon CMOS, 1 transistor memory cell
- 16 Meg density: 16Mx1
- 400mil 28 pin plastic SOJ, 400mil 28 pin plastic TSOP
- Single +5V Supply, $\pm 10\%$ tolerance
- Input : TTL compatible
- Output: TTL compatible, tri-state, non-latch
- Refresh: 2048 cycles/32ms: provides backward compatibility with 4-Meg sockets.
- Read Modify Write capability
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ hidden refresh, $\overline{\text{RAS}}$ only refresh capability
- Fast Page Mode capability
- Multi bit test mode capability
- Built-in V_{BB} generator circuit
- Package
 - 28PIN PLASTIC SOJ (SOJ28-P-400)
 - 28PIN PLASTIC TSOP (TSOP28-P-400-K)
 - (TSOP28-P-400-L)

MSM5117100 FAMILY

Family	Access Time (Max.)			Cycle Time (Min.)	Power Dissipation (Max.)	
	t_{RAC}	t_{AA}	t_{CAC}		Operating	Standby
MSM5117100 - 60JS/TK/TL	60ns	30ns	15ns	110ns	660mW	5.5mW (MOS level)
MSM5117100 - 70JS/TK/TL	70ns	35ns	20ns	130ns	605mW	
MSM5117100 - 80JS/TK/TL	80ns	40ns	20ns	150ns	550mW	

JS ; SOJ / TK ; TSOP(NORMAL) / TL ; TSOP (REVERSE)

PIN CONFIGURATION (TOP VIEW)

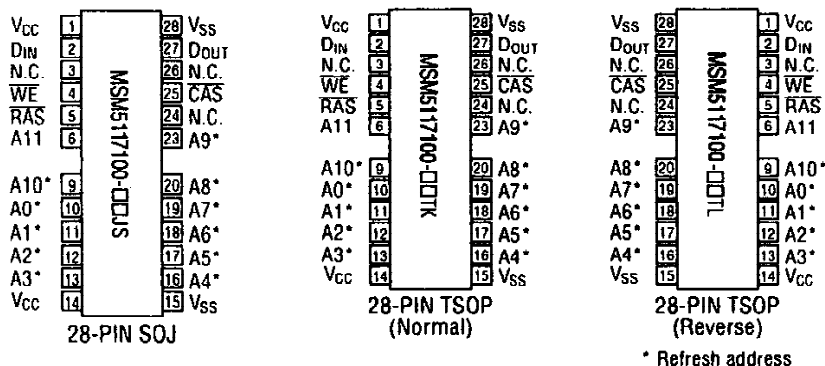


Figure 1. Pin Configuration

Pin Names	Function
A0-A11	Address Input
RAS	Row Address Strobe
CAS	Column Address Strobe
D _{IN}	Data Input
D _{OUT}	Data Output
WE	Write Enable
V _{CC}	Power Supply (+5V)
V _{SS}	Ground (0V)
N.C.	No Connection

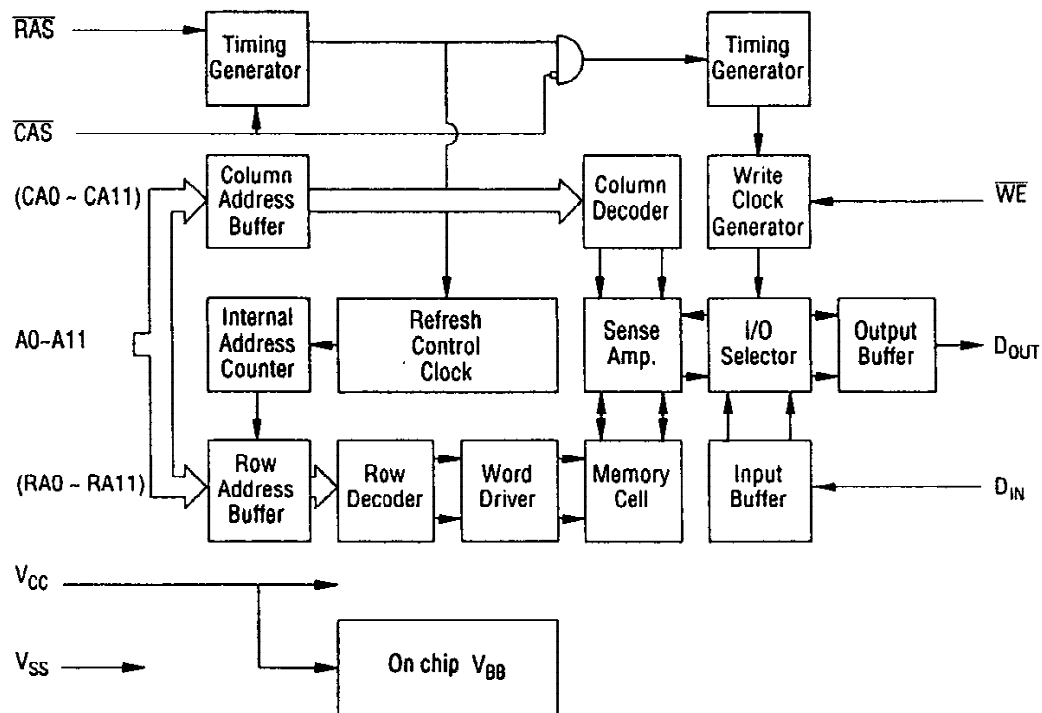


Figure 2. Block Diagram

ELECTRICAL CHARACTERISTICS**Absolute Maximum Ratings**

Parameter	Symbol	Condition	Rating	Unit
Voltage on any Pin Relative to V _{SS}	V _T	T _a = 25°C	-1.0 ~ +7.0	V
Short Circuit Output Current	I _{OS}	T _a = 25°C	50	mA
Power Dissipation	P _D	T _a = 25°C	1	W
Operating Temperature	T _{opr}	—	0 ~ +70	°C
Storage Temperature	T _{stg}	—	-55 ~ +150	°C

Recommended Operating Conditions (T_a = 0 ~ 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	V _{CC}	—	4.5	5.0	5.5	V
	V _{SS}	—	0	0	0	V
Input High Voltage	V _{IH}	—	2.4	—	6.5	V
Input Low Voltage	V _{IL}	—	-1.0	—	0.8	V

- Notes: 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. All voltages are referenced to V_{SS}.

DC Characteristics ($V_{CC} = 5.0\text{ V} \pm 10\%$, $T_a = 0 \sim +70^\circ\text{C}$)

Parameter	Symbol	Condition	MSM 5117100-60 JS/TK/TL		MSM 5117100-70 JS/TK/TL		MSM 5117100-80 JS/TK/TL		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	V_{OH}	$I_{OH} = -5.0\text{mA}$	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	—
Output Low Voltage	V_{OL}	$I_{OL} = 4.2\text{mA}$	0	0.4	0	0.4	0	0.4	V	—
Input Leakage Current	I_{LI}	$0\text{V} \leq V_i \leq 6.5\text{V}$ All other pins not under test = 0V	-10	10	-10	10	-10	10	μA	—
Output Leakage Current	I_{LO}	DOUT disable $0\text{V} \leq V_O \leq 5.5\text{V}$	-10	10	-10	10	-10	10	μA	—
Average Power Supply Current (Operating)	I_{CC1}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycling $t_{RC} = \text{min.}$	—	120	—	110	—	100	mA	1, 2
Power Supply Current (Standby)	I_{CC2}	$\overline{\text{RAS}} = V_{IH}$ $\overline{\text{CAS}} = V_{IH}$ DOUT = HZ	—	2	—	2	—	2	mA	TTL
Average Power Supply Current ($\overline{\text{RAS}}$ only Refresh)	I_{CC3}	$\overline{\text{RAS}}$ cycling $\overline{\text{CAS}} = V_{IH}$ $t_{RC} = \text{min.}$	—	120	—	110	—	100	mA	2
Power Supply Current (Standby)	I_{CC5}	$\overline{\text{RAS}} = V_{CC} - 0.2\text{V}$ $\overline{\text{CAS}} = V_{CC} - 0.2\text{V}$ DOUT = HZ	—	1	—	1	—	1	mA	MOS
Average Power Supply Current ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	I_{CC6}	$\overline{\text{RAS}}$ cycling $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$	—	120	—	110	—	100	mA	1
Average Power Supply Current (Fast Page Mode)	I_{CC7}	$\overline{\text{RAS}} = V_{IL}$ $\overline{\text{CAS}}$ cycling $t_{PC} = \text{min.}$	—	110	—	100	—	90	mA	1, 3

- Notes: 1. I_{CC} is dependent on output loading and cycle rates.
Specified values are obtained with the output open.
2. Address can be changed once or less while $\overline{\text{RAS}} = V_{IL}$.
3. Address can be changed once or less while $\overline{\text{CAS}} = V_{IH}$.

Capacitance ($V_{CC} = 5.0\text{ V} \pm 10\%$, $T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

Parameter	Symbol	Condition	Typ.	Max.	Unit
Input Capacitance (A_0 to A_{11} , D_{IN})	C_{IN1}	—	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	—	—	7	pF
Output Capacitance (D_{OUT})	C_{OUT}	—	—	7	pF

AC Characteristics ($V_{CC} = 5.0\text{ V} \pm 10\%$, $T_a = 0 \sim +70^\circ\text{C}$)

(For the following tables under the AC Characteristics, please refer to the Notes listed on page 13.)

Parameter	Symbol	MSM 5117100-60 JS/TK/TL		MSM 5117100-70 JS/TK/TL		MSM 5117100-80 JS/TK/TL		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	110	—	130	—	150	—	ns	—
RAS Precharge Time	t_{RP}	40	—	50	—	60	—	ns	—
RAS Pulse Width	t_{RAS}	60	10000	70	10000	80	10000	ns	—
CAS Pulse Width	t_{CAS}	15	10000	20	10000	20	10000	ns	—
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	ns	—
Row Address Hold Time	t_{RAH}	10	—	10	—	10	—	ns	—
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	—
Column Address Hold Time	t_{CAH}	15	—	15	—	15	—	ns	—
Column Address Hold Time referenced to $\overline{RAS}$	t_{AR}	50	—	55	—	60	—	ns	—
RAS to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	20	60	ns	5
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	15	40	ns	6
RAS Hold Time	t_{RSH}	15	—	20	—	20	—	ns	—
CAS Hold Time	t_{CSH}	60	—	70	—	80	—	ns	—
CAS to RAS Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	—
Transition Time	t_T	3	50	3	50	3	50	ns	3
Refresh Period	t_{REF}	—	32	—	32	—	32	ms	—

Read Cycle

Parameter	Symbol	MSM 5117100-60 JS/TK/TL		MSM 5117100-70 JS/TK/TL		MSM 5117100-80 JS/TK/TL		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Access Time from $\overline{\text{RAS}}$	t _{RAC}	—	60	—	70	—	80	ns	4, 5
Access Time from $\overline{\text{CAS}}$	t _{CAC}	—	15	—	20	—	20	ns	4, 5
Access Time from Column Address	t _{AA}	—	30	—	35	—	40	ns	4, 6
Read Command Set-up Time	t _{RCS}	0	—	0	—	0	—	ns	—
Read Command Hold Time referenced to $\overline{\text{CAS}}$	t _{RCH}	0	—	0	—	0	—	ns	8
Read Command Hold Time referenced to $\overline{\text{RAS}}$	t _{RRH}	0	—	0	—	0	—	ns	8
Column Address to $\overline{\text{RAS}}$ Lead Time	t _{RAL}	30	—	35	—	40	—	ns	—
$\overline{\text{CAS}}$ to Output in Low-Z	t _{CLZ}	0	—	0	—	0	—	ns	4
Output Buffer Turn-off Delay	t _{OFF}	0	15	0	20	0	20	ns	7

Write Cycle

Parameter	Symbol	MSM 5117100-60 JS/TK/TL		MSM 5117100-70 JS/TK/TL		MSM 5117100-80 JS/TK/TL		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Command Set-up Time	t _{WCS}	0	—	0	—	0	—	ns	9
Write Command Hold Time	t _{WCH}	10	—	15	—	15	—	ns	—
Write Command Hold Time referenced to $\overline{\text{RAS}}$	t _{WCR}	45	—	55	—	60	—	ns	—
Write Command Pulse Width	t _{WP}	10	—	10	—	10	—	ns	—
Write Command to $\overline{\text{RAS}}$ Lead Time	t _{RWL}	15	—	20	—	20	—	ns	—
Write Command to $\overline{\text{CAS}}$ Lead Time	t _{CWL}	15	—	20	—	20	—	ns	—
Data Set-up Time	t _{DS}	0	—	0	—	0	—	ns	—
Data Hold Time	t _{DH}	15	—	15	—	15	—	ns	—
Data Hold Time referenced to $\overline{\text{RAS}}$	t _{DHR}	50	—	55	—	60	—	ns	—

Read/Write Cycle

Parameter	Symbol	MSM 5117100-60 JS/TK/TL		MSM 5117100-70 JS/TK/TL		MSM 5117100-80 JS/TK/TL		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Read/Write Cycle Time	trWC	130	—	155	—	175	—	ns	—
RAS to WE Delay Time	trWD	60	—	70	—	80	—	ns	9
CAS to WE Delay Time	tcWD	15	—	20	—	20	—	ns	9
Column Address to WE Delay Time	tawD	30	—	35	—	40	—	ns	9

Refresh Cycle

Parameter	Symbol	MSM 5117100-60 JS/TK/TL		MSM 5117100-70 JS/TK/TL		MSM 5117100-80 JS/TK/TL		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
CAS Set-up Time (CAS before RAS)	tCSR	10	—	10	—	10	—	ns	—
CAS Hold Time (CAS before RAS)	tCHR	20	—	20	—	20	—	ns	—
WE to RAS Precharge Time (CAS before RAS)	tWRP	10	—	10	—	10	—	ns	—
WE to RAS Hold Time (CAS before RAS)	tWRH	10	—	10	—	10	—	ns	—
RAS to CAS Precharge Time	trPC	10	—	10	—	10	—	ns	—
CAS Precharge Time	tcPN	10	—	10	—	10	—	ns	—

Fast Page Mode Cycle

Parameter	Symbol	MSM 5117100-60 JS/TK/TL		MSM 5117100-70 JS/TK/TL		MSM 5117100-80 JS/TK/TL		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Fast Page Mode Cycle time	tPC	40	—	45	—	50	—	ns	—
CAS Precharge Time (Fast Page Mode)	tCP	10	—	10	—	10	—	ns	—
RAS Pulse Width (Fast Page Mode)	trASP	60	100000	70	100000	80	100000	ns	—
Access Time from CAS Precharge	tCPA	—	35	—	40	—	45	ns	4
RAS Hold Time referenced to CAS Precharge	trHCP	35	—	40	—	45	—	ns	—

Fast Page Mode Read /Write Cycle

Parameter	Symbol	MSM 5117100-60 JS/TK/TL		MSM 5117100-70 JS/TK/TL		MSM 5117100-80 JS/TK/TL		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Fast Page Mode Read/Write Cycle Time	t _{PRWC}	60	—	70	—	75	—	ns	—
CAS Precharge to $\overline{WE}$ Delay Time	t _{CPW}	35	—	40	—	45	—	ns	9

Counter Test Cycle

Parameter	Symbol	MSM 5117100-60 JS/TK/TL		MSM 5117100-70 JS/TK/TL		MSM 5117100-80 JS/TK/TL		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
CAS Precharge Time (CAS before RAS Counter Test)	t _{CPT}	40	—	40	—	40	—	ns	—

Read,Write, Read/Write Refresh Cycle in the Test Mode

Parameter	Symbol	MSM 5117100-60 JS/TK/TL		MSM 5117100-70 JS/TK/TL		MSM 5117100-80 JS/TK/TL		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t _{RC}	115	—	135	—	155	—	ns	—
RAS Precharge Time	t _{RP}	40	—	50	—	60	—	ns	—
RAS Pulse Width	t _{RAS}	65	10000	75	10000	85	10000	ns	—
CAS Pulse Width	t _{CAS}	20	10000	25	10000	25	10000	ns	—
Row Address Set-up Time	t _{ASR}	0	—	0	—	0	—	ns	—
Row Address Hold Time	t _{RAH}	10	—	10	—	10	—	ns	—
Column Address Set-up Time	t _{ASC}	0	—	0	—	0	—	ns	—
Column Address Hold Time	t _{CAH}	15	—	15	—	15	—	ns	—
Column Address Hold Time referenced to $\overline{RAS}$	t _{AR}	50	—	55	—	60	—	ns	—
RAS to CAS Delay Time	t _{RCD}	20	45	20	50	20	60	ns	5
RAS to Column Address Delay Time	t _{RAD}	15	30	15	35	15	40	ns	6
RAS Hold Time	t _{RSH}	20	—	25	—	25	—	ns	—
CAS Hold Time	t _{CSH}	65	—	75	—	85	—	ns	—
CAS to RAS Precharge Time	t _{CRP}	10	—	10	—	10	—	ns	—
Transition Time	t _T	3	50	3	50	3	50	ns	3
Refresh Period	t _{REF}	—	32	—	32	—	32	ms	—

Read Cycle In the Test Mode

Parameter	Symbol	MSM 5117100-60 JS/TK/TL		MSM 5117100-70 JS/TK/TL		MSM 5117100-80 JS/TK/TL		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Access Time from $\overline{\text{RAS}}$	tRAC	—	65	—	75	—	85	ns	4, 5
Access Time from $\overline{\text{CAS}}$	tCAC	—	20	—	25	—	25	ns	4, 5
Access Time from Column Address	tAA	—	35	—	40	—	45	ns	4, 6
Read Command Set-up Time	tRCS	0	—	0	—	0	—	ns	—
Read Command Hold Time referenced to $\overline{\text{CAS}}$	tRCH	0	—	0	—	0	—	ns	8
Read Command Hold Time referenced to $\overline{\text{RAS}}$	tRRH	0	—	0	—	0	—	ns	8
Column Address to $\overline{\text{RAS}}$ Lead Time	tRAL	35	—	40	—	45	—	ns	—
$\overline{\text{CAS}}$ to Output in Low-Z	tCLZ	0	—	0	—	0	—	ns	4
Output Buffer Turn-off Delay	tOFF	0	15	0	20	0	20	ns	7

Write Cycle In the Test Mode

Parameter	Symbol	MSM 5117100-60 JS/TK/TL		MSM 5117100-70 JS/TK/TL		MSM 5117100-80 JS/TK/TL		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Command Set-up Time	twCS	0	—	0	—	0	—	ns	9
Write Command Hold Time	twCH	10	—	15	—	15	—	ns	—
Write Command Hold Time referenced to $\overline{\text{RAS}}$	twCR	45	—	55	—	60	—	ns	—
Write Command Pulse Width	tWP	10	—	10	—	10	—	ns	—
Write Command to $\overline{\text{RAS}}$ Lead Time	trWL	15	—	20	—	20	—	ns	—
Write Command to $\overline{\text{CAS}}$ Lead Time	tcWL	15	—	20	—	20	—	ns	—
Data Set-up Time	tDS	0	—	0	—	0	—	ns	—
Data Hold Time	tDH	15	—	15	—	15	—	ns	—
Data Hold Time referenced to $\overline{\text{RAS}}$	tDHR	50	—	55	—	60	—	ns	—

Read/Write Cycle In the Test Mode

Parameter	Symbol	MSM 5117100-60 JS/TK/TL		MSM 5117100-70 JS/TK/TL		MSM 5117100-80 JS/TK/TL		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Read/Write Cycle Time	trWC	135	—	160	—	180	—	ns	—
RAS to WE Delay Time	trWD	65	—	75	—	85	—	ns	9
CAS to WE Delay Time	tcWD	20	—	25	—	25	—	ns	9
Column Address to WE Delay Time	tawD	35	—	40	—	45	—	ns	9

Refresh Cycle In the Test Mode

Parameter	Symbol	MSM 5117100-60 JS/TK/TL		MSM 5117100-70 JS/TK/TL		MSM 5117100-80 JS/TK/TL		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
CAS Set-up Time (CAS before RAS)	tCSR	10	—	10	—	10	—	ns	—
CAS Hold Time (CAS before RAS)	tCHR	20	—	20	—	20	—	ns	—
WE to RAS Precharge Time (CAS before RAS)	tWRP	10	—	10	—	10	—	ns	—
WE to RAS Hold Time (CAS before RAS)	tWRH	10	—	10	—	10	—	ns	—
RAS to CAS Precharge Time	trPC	10	—	10	—	10	—	ns	—
CAS Precharge Time	tCPN	10	—	10	—	10	—	ns	—

Fast Page Mode Cycle In the Test Mode

Parameter	Symbol	MSM 5117100-60 JS/TK/TL		MSM 5117100-70 JS/TK/TL		MSM 5117100-80 JS/TK/TL		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Fast Page Mode Cycle time	tpc	45	—	50	—	55	—	ns	—
CAS Precharge Time (Fast Page Mode)	tCP	10	—	10	—	10	—	ns	—
RAS Pulse Width (Fast Page Mode)	trASP	65	100000	75	100000	85	100000	ns	—
Access Time from CAS Precharge	tCPA	—	40	—	45	—	50	ns	4
RAS Hold Time referenced to CAS Precharge	trHCP	40	—	45	—	50	—	ns	—

Fast Page Mode Read /Write Cycle in the Test Mode

Parameter	Symbol	MSM 5117100-60 JS/TK/TL		MSM 5117100-70 JS/TK/TL		MSM 5117100-80 JS/TK/TL		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Fast Page Mode Read/Write Cycle Time	t _{PRWC}	65	—	75	—	80	—	ns	—
CAS Precharge to WE Delay Time	t _{CPW}	40	—	45	—	50	—	ns	9

Test Mode Cycle in the Test Mode

Parameter	Symbol	MSM 5117100-60 JS/TK/TL		MSM 5117100-70 JS/TK/TL		MSM 5117100-80 JS/TK/TL		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
WE Set-up Time	t _{WSR}	10	—	10	—	10	—	ns	—
WE Hold Time	t _{WHR}	20	—	20	—	20	—	ns	—

Counter Test Cycle in the Test Mode

Parameter	Symbol	MSM 5117100-60 JS/TK/TL		MSM 5117100-70 JS/TK/TL		MSM 5117100-80 JS/TK/TL		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
CAS Precharge Time (CAS before RAS Counter Test)	t _{CPT}	40	—	40	—	40	—	ns	—

- Notes :
1. An initial pause of 200 μ s is required after power-up, followed by 8 $\overline{\text{RAS}}$ cycles before the proper device operation is achieved. In the case of using an internal refresh counter, a minimum of 8 $\overline{\text{CAS}}$ cycles before $\overline{\text{RAS}}$ initialization cycles instead of 8 $\overline{\text{RAS}}$ cycles are required.
 2. AC measurements assume $t_T = 5\text{ns}$
 3. $V_{IH}(\text{min.})$ and $V_{IL}(\text{max.})$ are reference levels for measuring the timing of input signals. Also transition times are measured between V_{IH} and V_{IL} .
 4. Measured with a load circuit equivalent to 2 TLL loads and 100pF.
 5. Operation within the $t_{\text{RCD}}(\text{max.})$ limit insures that $t_{\text{RAC}}(\text{max.})$ can be met. $t_{\text{RCD}}(\text{max.})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{max.})$ limit, then the access time is controlled by t_{CAC} .
 6. Operation within the $t_{\text{RAD}}(\text{max.})$ limit insures that $t_{\text{RAC}}(\text{max.})$ can be met. $t_{\text{RAD}}(\text{max.})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max.})$ limit, then the access time is controlled by t_{AA} .
 7. $t_{\text{OFF}}(\text{max.})$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
 8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
 9. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{\text{WSC}} \geq t_{\text{WCS}}(\text{min.})$, the cycle is an early write cycle and the data out pin will remain as an open circuit (high impedance) through the entire cycle. If $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min.})$, $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min.})$, $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min.})$, and $t_{\text{CPW}} \geq t_{\text{CPW}}(\text{min.})$, then the cycle is a read/write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, then the condition of the data out (at access time) is indeterminate.
 10. $\overline{\text{WE}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Cycle (Test mode in Cycle) puts the device into "Test Mode". And " $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle" or " $\overline{\text{RAS}}$ only Refresh Cycle" puts it back into "Normal Mode". In "Test Mode", the RAM is internally organized by 512K words by 32 bits, and data is written into 32 sectors in parallel and is retrieved the same way. A0 (Column), A1 (Column), A10 (Column), A11 (Row), A11 (Column) are not used. If upon reading, all bits are equal (all "H"s or "L"s), the data output pin indicates an "H". If any of the bits differed, the data output pin would indicate an "L". In "Test Mode", the 16M x 1 DRAM can be tested as if it were a 512K x 1 DRAM.

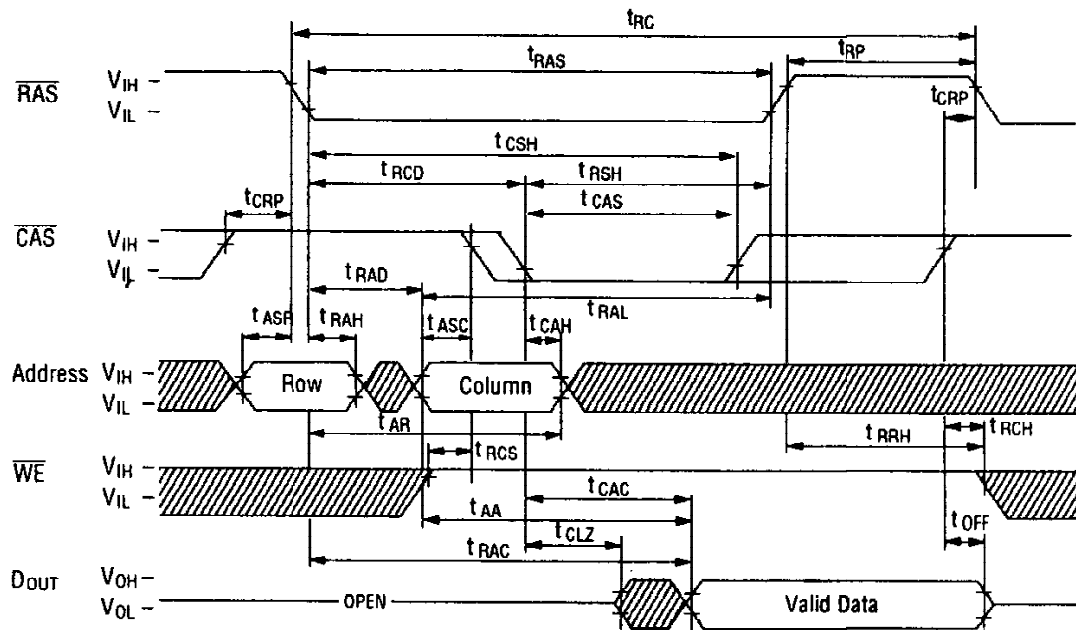


Figure 3. Read Cycle

H or L

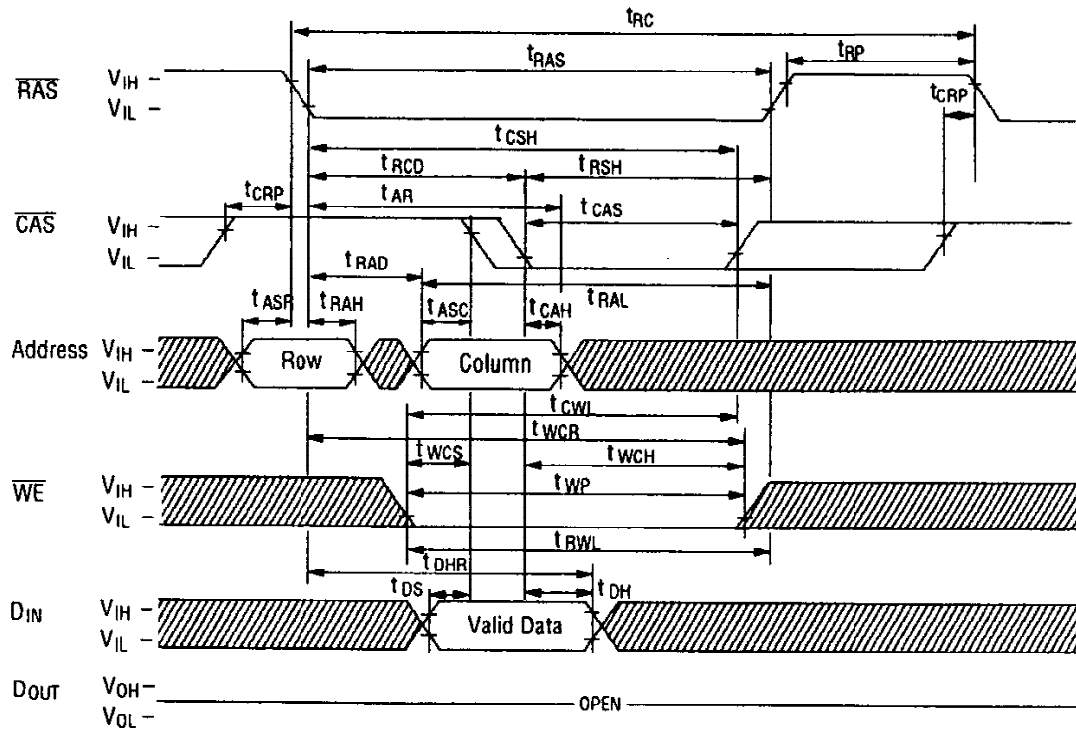


Figure 4. Write Cycle (Early Write)

H or L

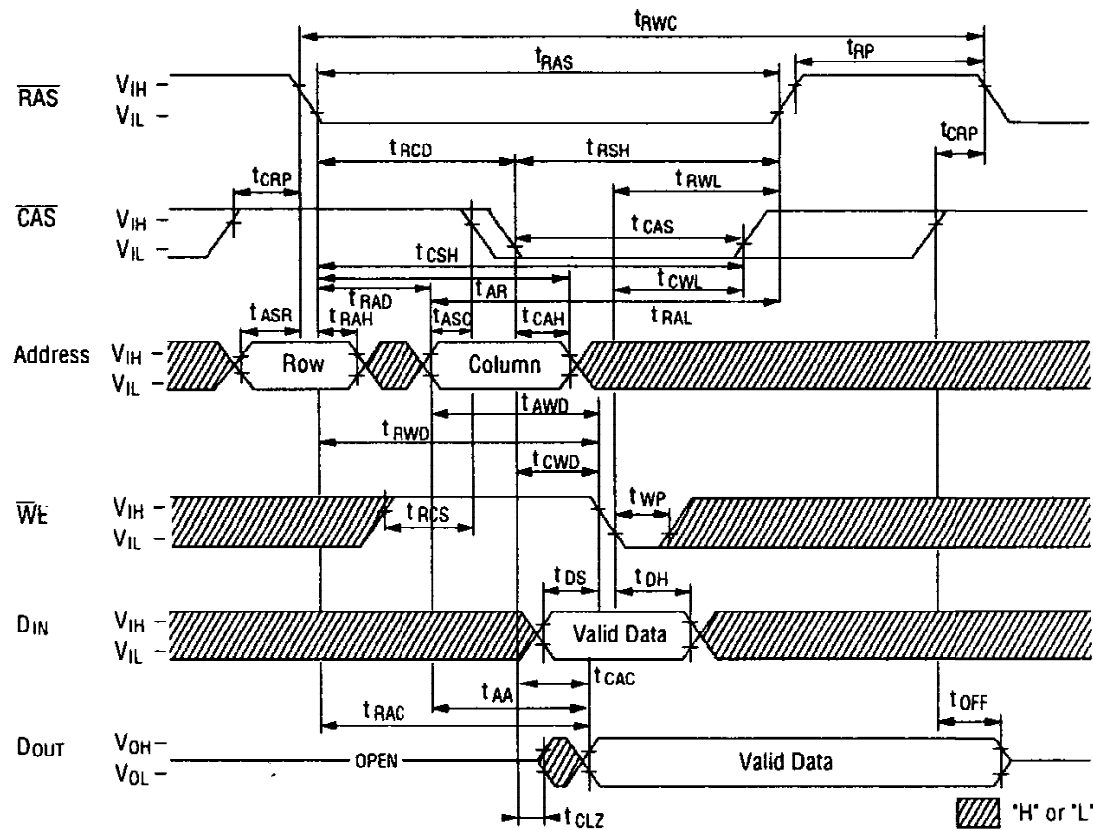


Figure 5. Read/Write Cycle

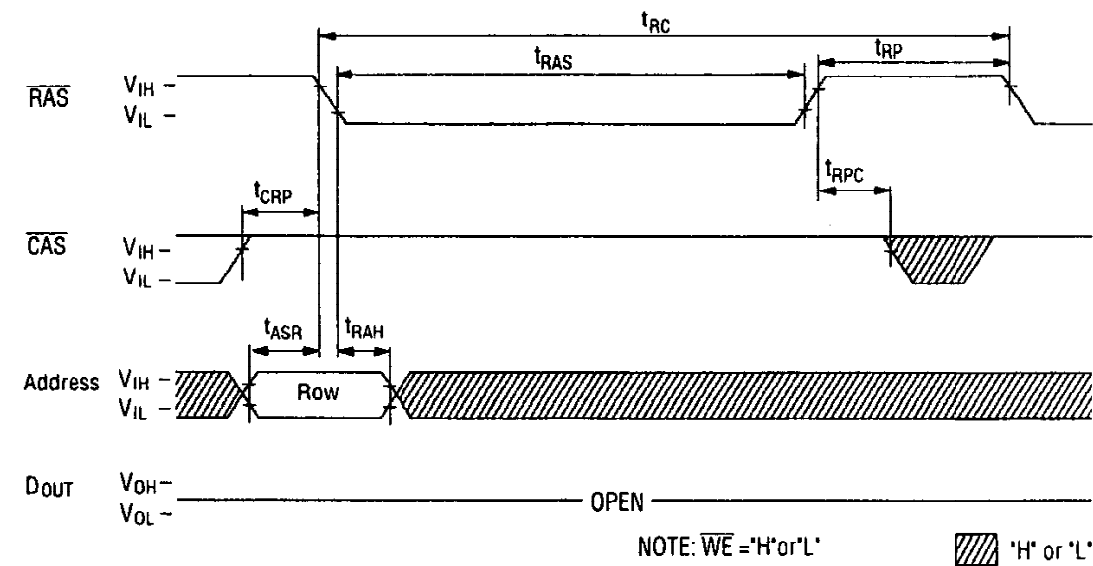


Figure 6. RAS Only Refresh Cycle

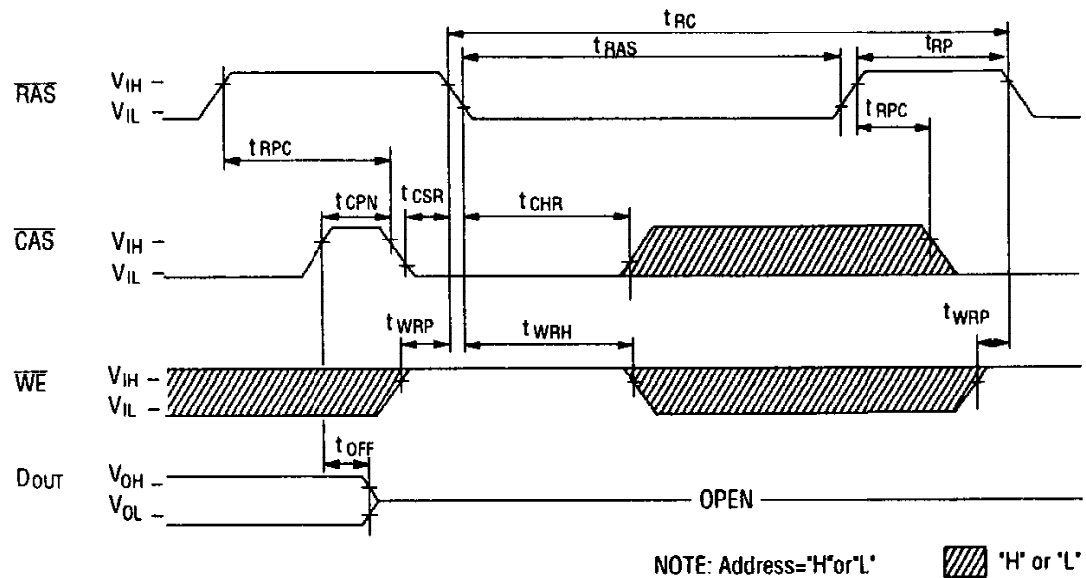


Figure 7. CAS Before RAS Refresh Cycle

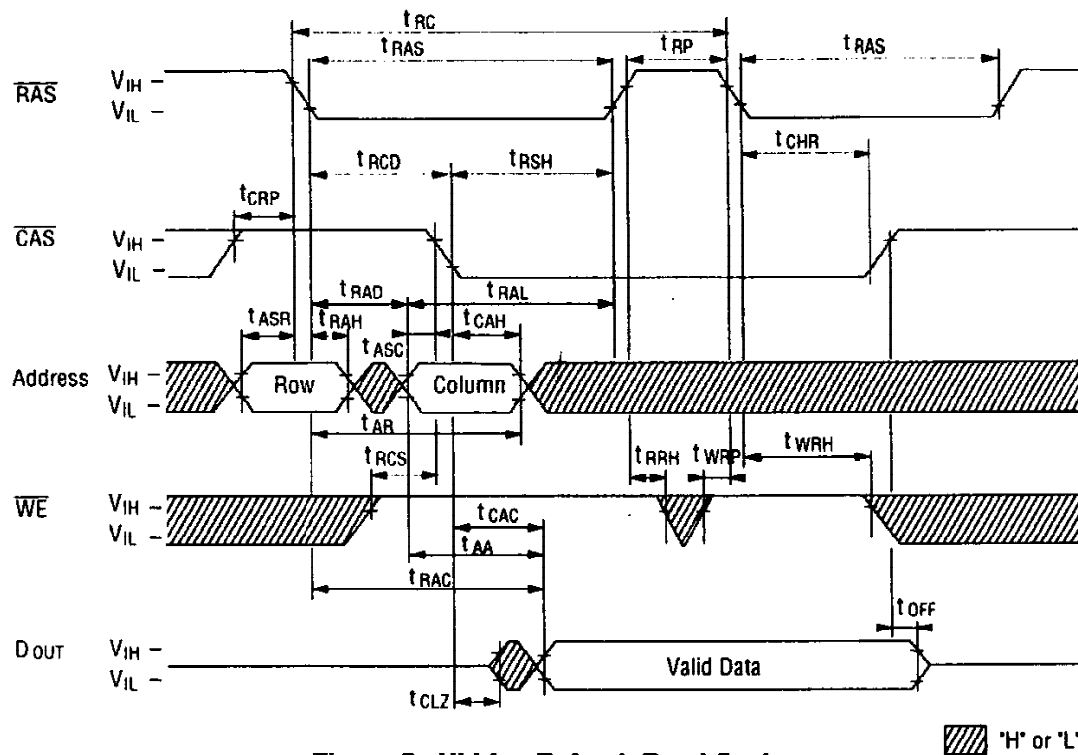
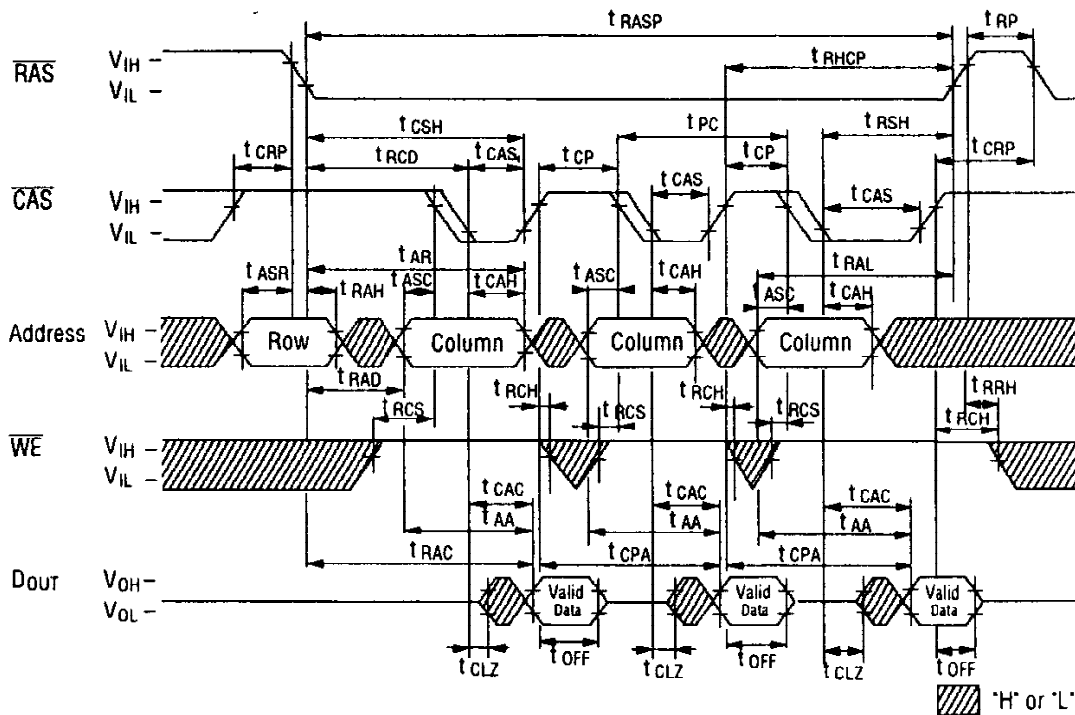
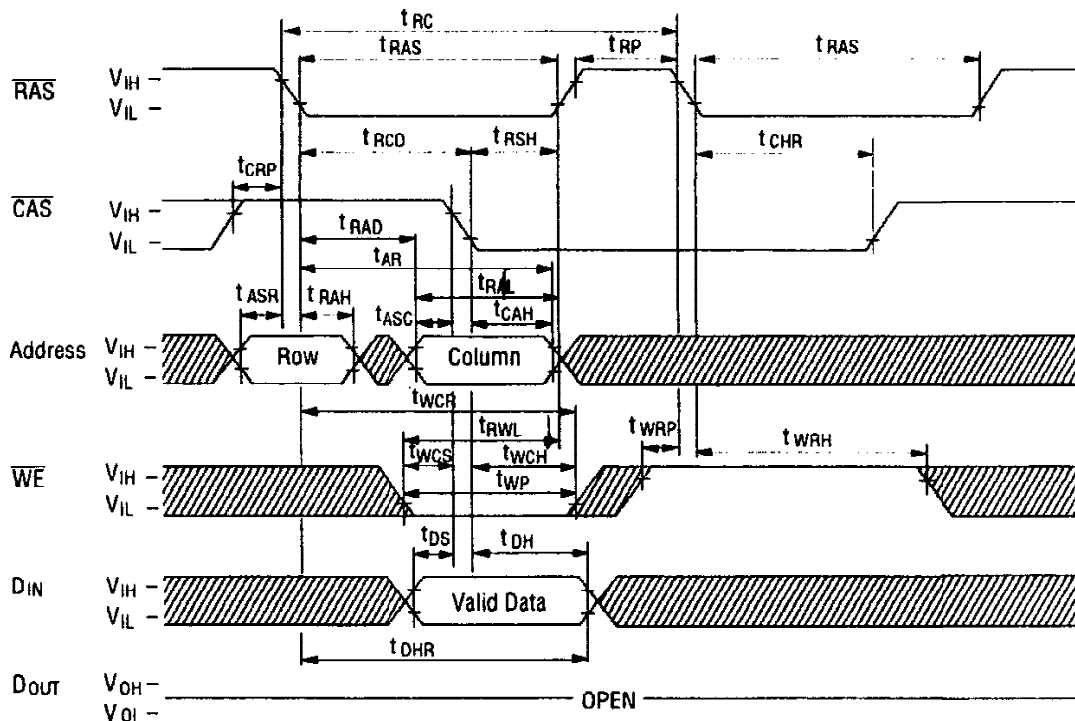


Figure 8. Hidden Refresh Read Cycle



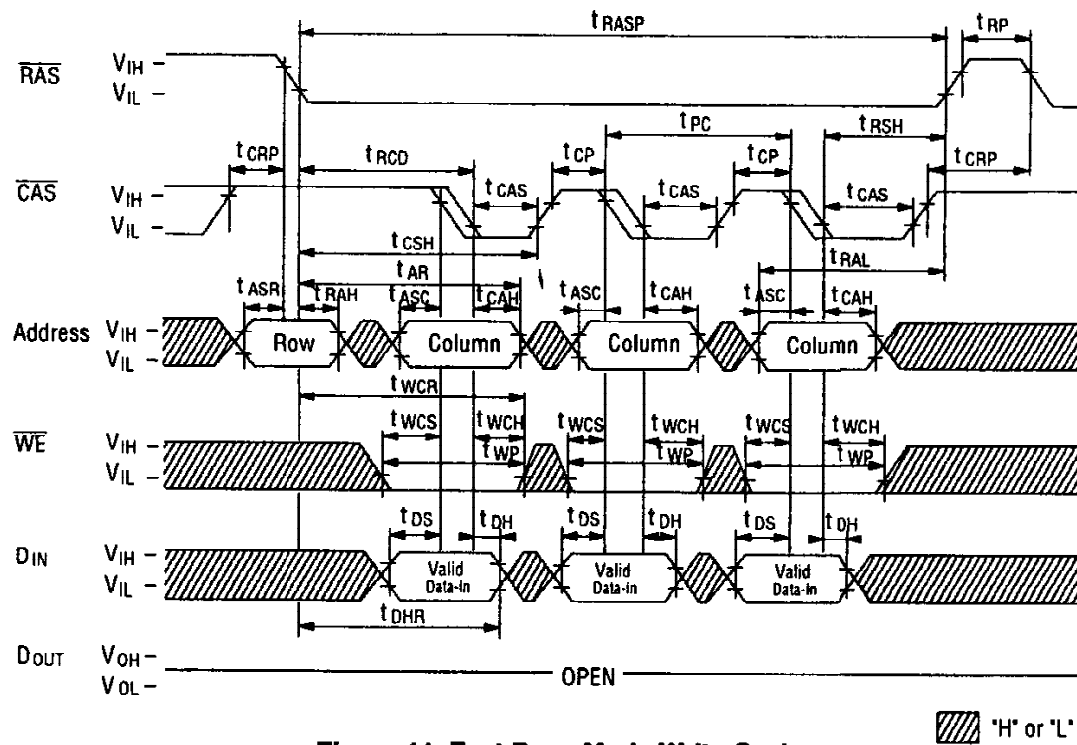


Figure 11. Fast Page Mode Write Cycle

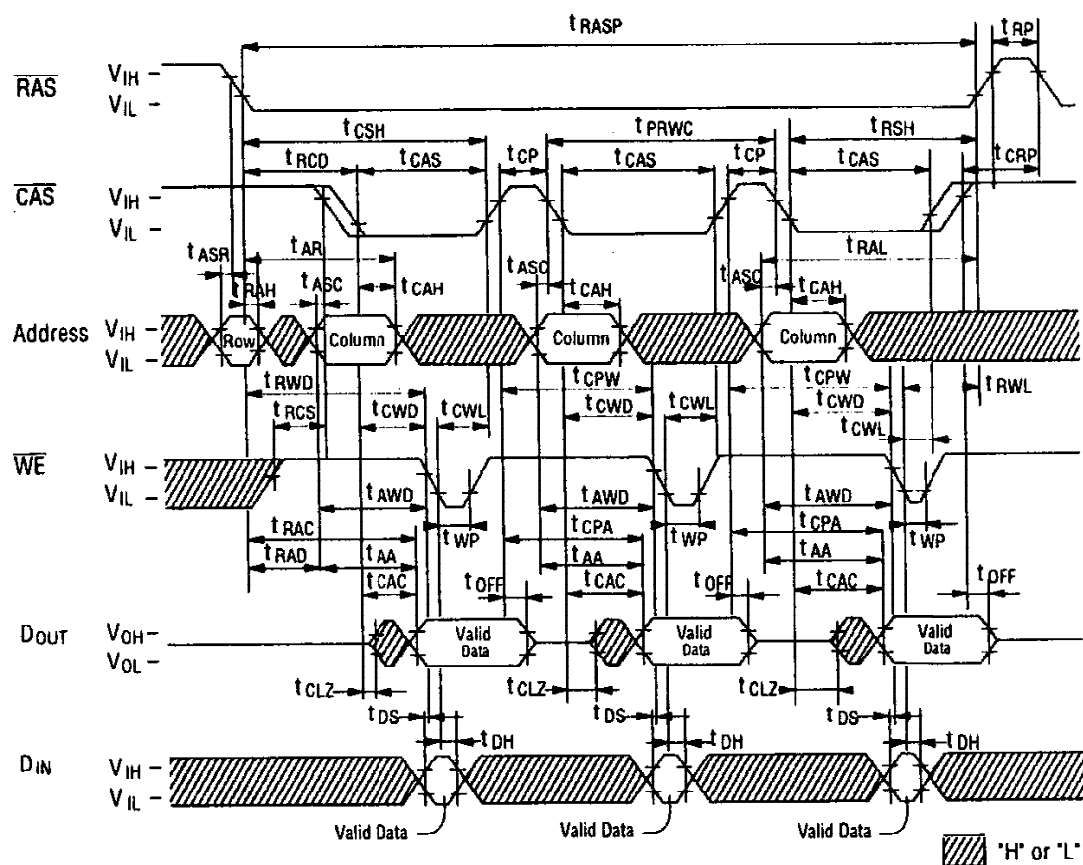


Figure 12. Fast Page Mode Read/Write Cycle

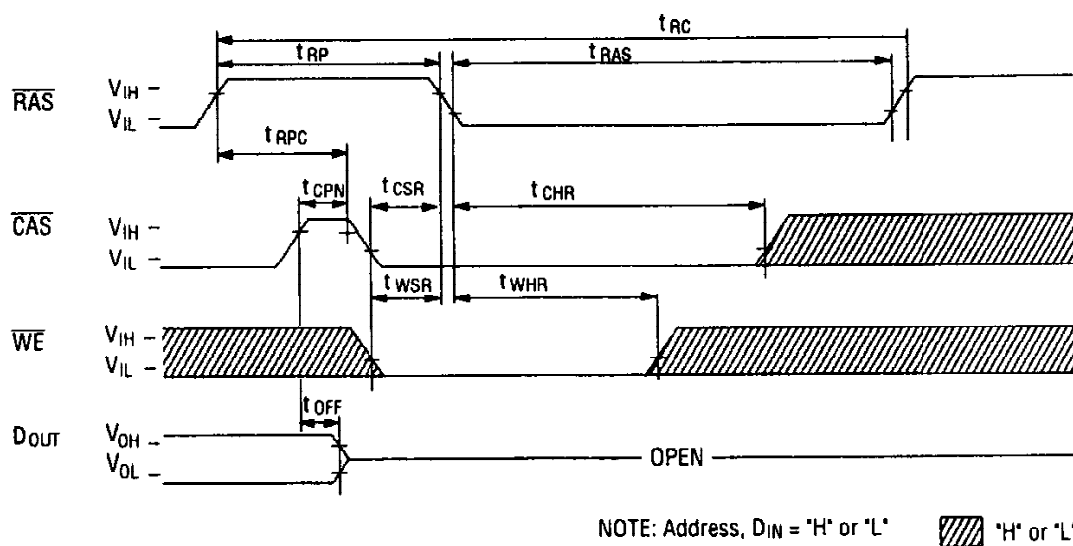
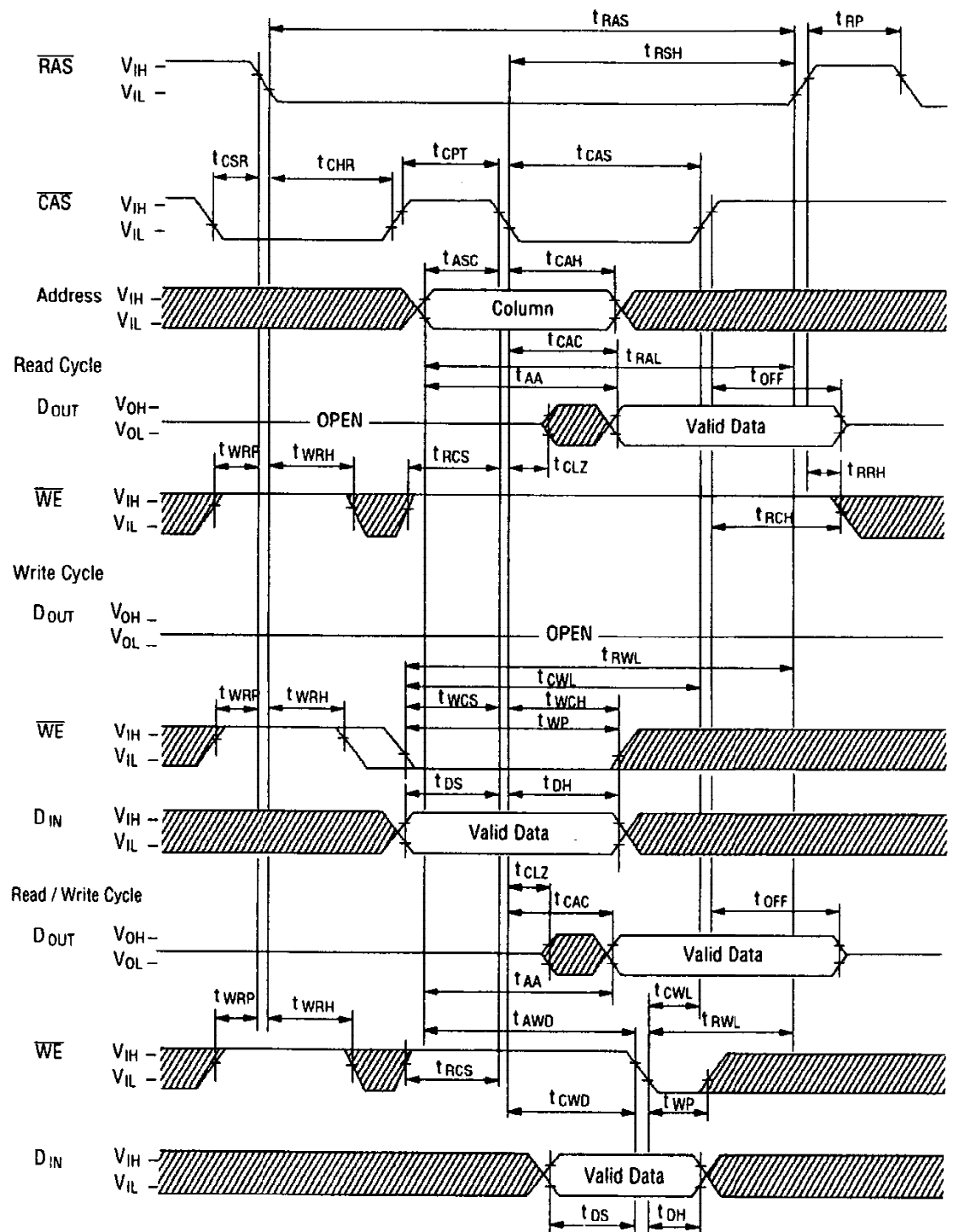


Figure 13. Test Mode In Cycle

Figure 14. $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Counter Test Cycle

'H' or 'L'