

MSM64172

4-Bit Microcontroller with Built-in Serial Port and LCD Driver

GENERAL DESCRIPTION

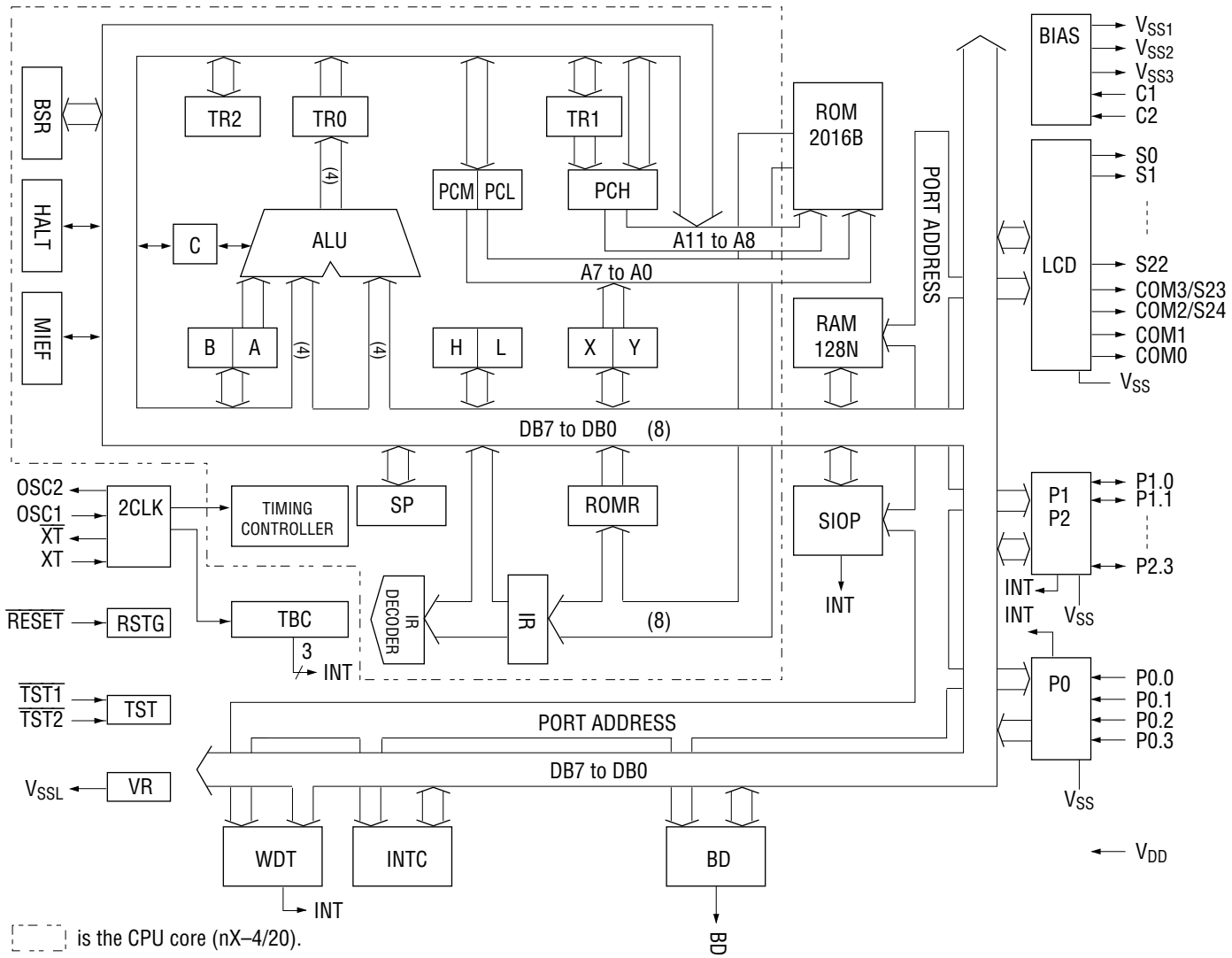
The MSM64172 is a low-power 4-bit microcontroller that incorporates Oki's original CPU core nX-4/20. The MSM64172 has a minimum instruction execution time of 5 μ s (@ 600 kHz and 3.0 V). The device includes an internal 2016-byte program memory, 128-nibble data memory, two 4-bit input-output ports, 4-bit input port, 8-bit synchronous serial port, LCD driver for up to 92 segments, and buzzer output port. Applications include low-power products with LCD functions.

FEATURES

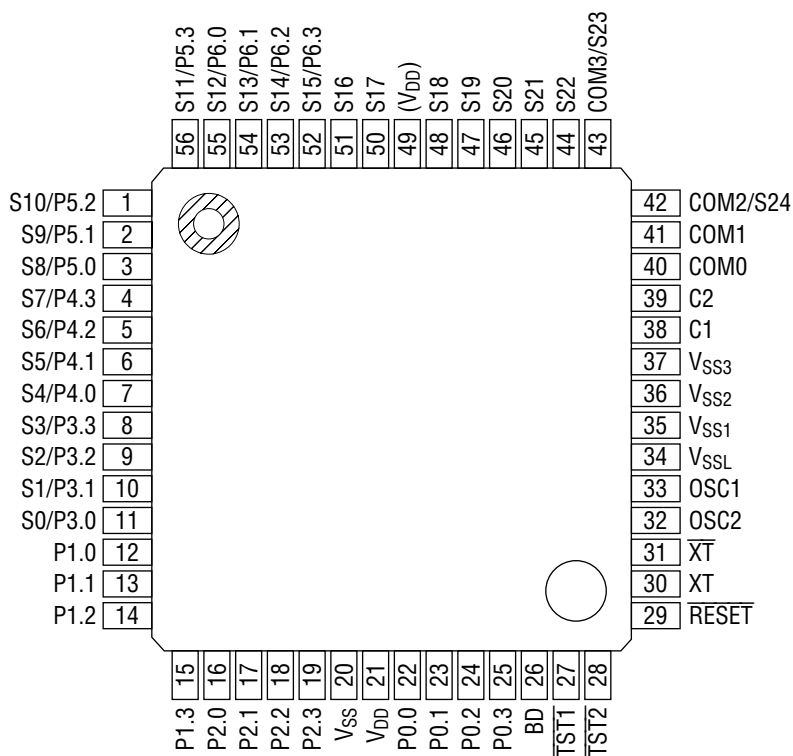
- Operating range
 - Operating frequencies
 - 1.5 V spec. : 32.768 kHz (crystal oscillation)
 - 3.0 V spec. low-speed clock : 32.768 kHz (crystal oscillation)
 - 3.0 V spec. high-speed clock : 600 kHz maximum
(RC oscillation/ceramic resonator oscillation)
 - Operating voltage : 0.9 to 1.8 V (1.5 V spec.)
1.8 to 3.6 V (3.0 V spec.)
 - Operating temperature : -10 to +65°C
- Memory space
 - Internal program memory : 2016 bytes
 - Internal data memory : 128 nibbles
- Minimum instruction execution time : 5 μ s @ 600 kHz (3.0 V spec. only)
91.6 μ s @ 32.768 kHz
- Serial port : Clock synchro, 8-bit data transfer
- LCD driver : 27 outputs (duty ratio switchable by software)
 - (1) At 1/4 duty and 1/3 bias : 92 segments (max.)
 - (2) At 1/3 duty and 1/3 bias : 72 segments (max.)
 - (3) At 1/2 duty and 1/2 bias : 50 segments (max.)
- Buzzer driver : 1 output; ON/OFF controllable in four modes
- Watchdog timer
- Clock : 32.768 kHz crystal oscillator
RC oscillator/ceramic oscillator (600 kHz max.)
for high-speed clock (only for 3.0 V spec.)
- CPU clock : 32.768 kHz
Switchable to high-speed clock by software
(only for 3.0 V spec.)
- Time base clock : 32.768 kHz
- Power supply voltage : 1.5 V/3.0 V (selectable by mask option), low power consumption

- I/O port
 - Input-output port : 2 ports × 4 bits
 - Input port : 1 port × 4 bits
(16 out of the 27 LCD driver outputs can be used as output-only ports by a mask option.)
- Interrupt sources
 - External interrupt : 2 sources
 - Internal interrupt : 5 sources
- Package options:
 - 56-pin plastic QFP (QFP56-P-910-0.65-K) : (Product name : MSM64172-xxxGS-K)
 - 56-pin plastic QFP (QFP56-P-910-0.65-2K) : (Product name : MSM64172-xxxGS-2K)
 - Chip : (Product name : MSM64172-xxx)
xxx indicates a code number.

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



56-Pin Plastic QFP

Note: Pin 49 is internally connected to V_{DD} , and V_{DD} should be supplied from pin 21.

PIN DESCRIPTIONS

Basic Functions

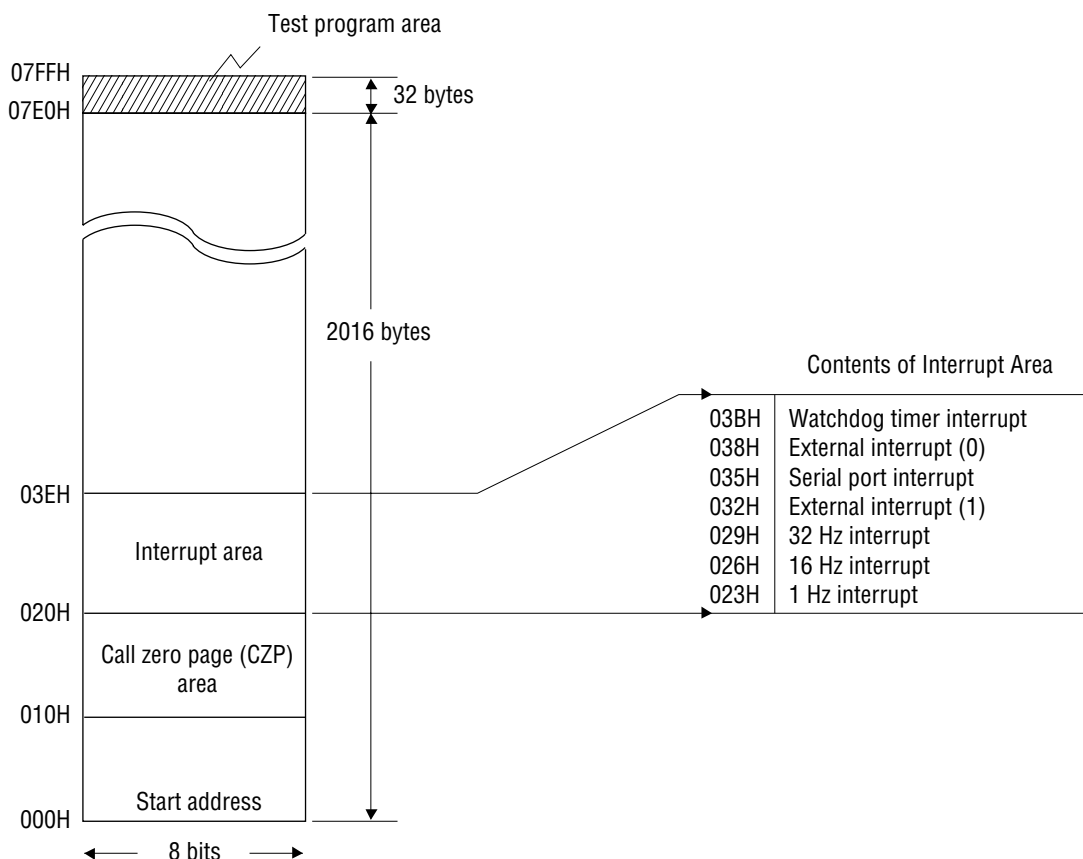
Function	Symbol	Type	Description
Power Supply	V _{DD}	—	0 V power supply
	V _{SS1}	—	Bias output for driving LCD (−1.5 V), or negative power supply at 1.5 V spec.
	V _{SS2}	—	Bias output for driving LCD (−3.0 V), or negative power supply at 3.0 V spec.
	V _{SS3}	—	Bias output for driving LCD (−4.5 V).
	V _{SS}	—	Negative power supply for I/O port interface
	V _{SSL}	—	Negative power supply for internal logic (internally generated constant voltage)
	C1, C2	—	Pins for connecting a capacitor for generating V _{SS1} , V _{SS2} , and V _{SS3} .
Oscillation	XT	I	32.768 kHz crystal connection pins
	$\overline{\text{XT}}$	O	
	OSC1	I	High-speed clock pins : A ceramic resonator and capacitors, or an external oscillation resistor (R _{OS}), should be connected to these pins.
	OSC2	O	
Ports	P0.0 to P0.3	I	Input port
	P1.0 to P2.3	I/O	Input-output ports
	BD	O	Buzzer driver pin
	S16 to S22	O	LCD driver pins
	S0/P3.0 to S15/P6.3	O	LCD driver pins or output ports by mask option
	COM3/S23	O	LCD common 3 signal output pin, or segment signal output pin during 1/3 or 1/2 duty
	COM2/S24	O	LCD common 2 signal output pin, or segment signal output pin during 1/2 duty
	COM1	O	LCD common 1 signal output pin
	COM0	O	LCD common 0 signal output pin
Reset	$\overline{\text{RESET}}$	I	Reset pin
Test	$\overline{\text{TST1}}$	I	Input pins for testing
	$\overline{\text{TST2}}$	I	

Secondary Functions

Symbol	Type	Description
P1.3	I	Serial data input pin (SIN)
P2.0	O	Serial data output pin (SOUT)
P2.1	O	Serial communication ready signal output pin (SPR)
P2.2	I/O	Serial communication clock input-output pin (SCLK)
P2.3	O	High-speed oscillation clock monitor pin for system clock (MON)

MEMORY MAPS

Program Memory



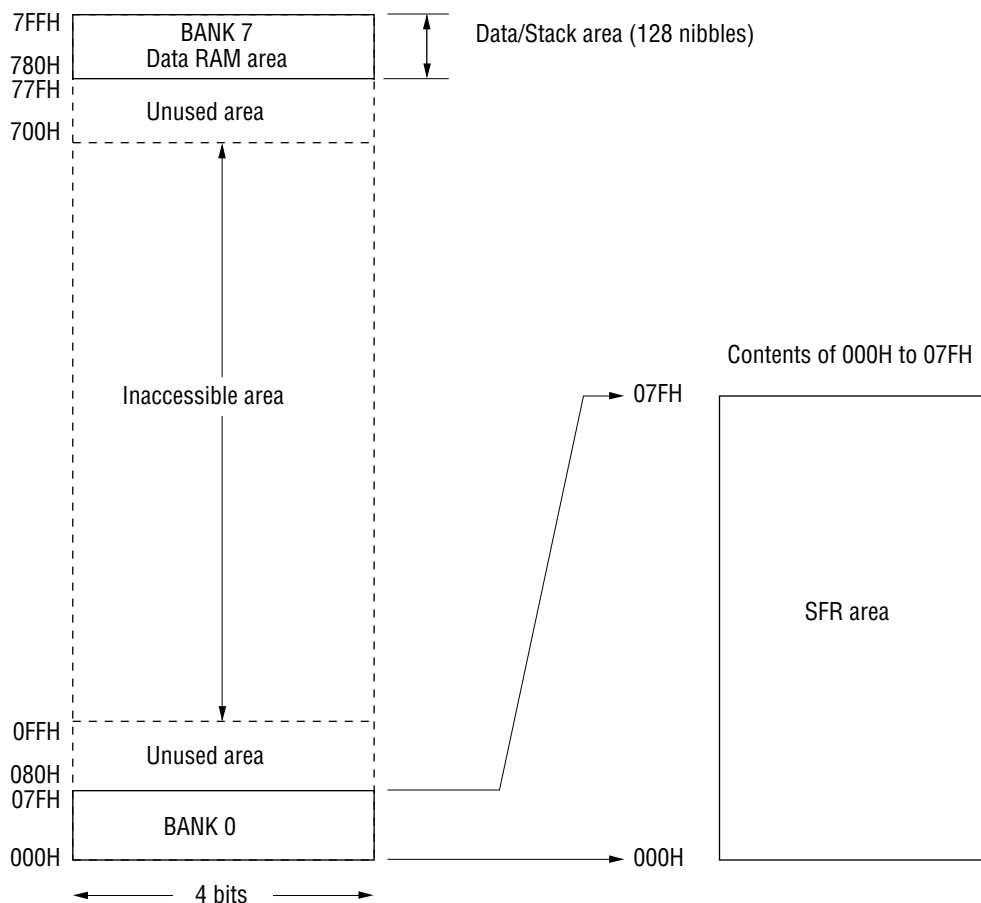
Program Memory Map

Address 000H is the instruction execution start address after a system reset. The call zero page (CZP) area from address 010H to address 01FH assigns the start address for the CZP subroutine of one-byte call instruction.

The start address of an interrupt subroutine is assigned to the interrupt address from address 02DH to 03DH. The user area has 2016 bytes at addresses 000H to 07DFH. No program can be stored in the test program area.

Data Memory

The data memory area consists of 8 banks and each bank has 256 nibbles (256×4 bits). The data RAM is assigned to BANK 7 and peripheral ports are assigned to BANK 0.



Data Memory Map

The data RAM area (128 nibbles) is shared by the stack area. The stack is a memory starting from address 7FFH toward the low-order addresses where 4 nibbles are used by Subroutine Call Instruction and 8 nibbles are used by an interrupt.

The addresses 080H to 0FFH of BANK 0 and the addresses 700H to 77FH of BANK 7 are not assigned as the data memory, so access to these addresses has no effect. Moreover, it is impossible to access BANK 1 to BANK 6.

ABSOLUTE MAXIMUM RATINGS (1.5 V Spec.)(V_{DD} = 0 V)

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage 1	V _{SS1}	Ta = 25°C	−2.0 to +0.3	V
Power Supply Voltage 2	V _{SS2}	Ta = 25°C	−4.0 to +0.3	V
Power Supply Voltage 3	V _{SS3}	Ta = 25°C	−5.5 to +0.3	V
Power Supply Voltage 4	V _{SSL}	Ta = 25°C	−2.0 to +0.3	V
Power Supply Voltage 5	V _{SS}	Ta = 25°C	−5.5 to +0.3	V
Input Voltage 1	V _{IN1}	V _{SS1} Input, Ta = 25°C	V _{SS1} − 0.3 to +0.3	V
Input Voltage 2	V _{IN2}	V _{SS} Input, Ta = 25°C	V _{SS} − 0.3 to +0.3	V
Input Voltage 3	V _{IN3}	V _{SSL} Input, Ta = 25°C	V _{SSL} − 0.3 to +0.3	V
Output Voltage 1	V _{OUT1}	V _{SS1} Output, Ta = 25°C	V _{SS1} − 0.3 to +0.3	V
Output Voltage 2	V _{OUT2}	V _{SS2} Output, Ta = 25°C	V _{SS2} − 0.3 to +0.3	V
Output Voltage 3	V _{OUT3}	V _{SS3} Output, Ta = 25°C	V _{SS3} − 0.3 to +0.3	V
Output Voltage 4	V _{OUT4}	V _{SS} Output, Ta = 25°C	V _{SS} − 0.3 to +0.3	V
Output Voltage 5	V _{OUT5}	V _{SSL} Output, Ta = 25°C	V _{SSL} − 0.3 to +0.3	V
Storage Temperature	T _{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS (1.5 V Spec.)(V_{DD} = 0 V)

Parameter	Symbol	Condition	Range	Unit
Operating Temperature	T _{op}	—	−10 to +65	°C
Operating Voltage	V _{SS1}	—	−1.8 to −0.9	V
	V _{SS}	—	−5.25 to V _{SS1}	V
Crystal Oscillation Frequency	f _{XT}	—	30 to 35	kHz

ELECTRICAL CHARACTERISTICS (1.5 V Spec.)

DC Characteristics

($V_{DD} = 0\text{ V}$, $V_{SS1} = V_{SS} = -1.5\text{ V}$, $T_a = -10\text{ to }+65^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
V_{SS2} Voltage	V_{SS2}	$C_a, C_b, C_{12} = 0.2\text{ }\mu\text{F}$ +100% -10%	-3.2	-3.0	-2.7	V	1
V_{SS3} Voltage	V_{SS3}	$C_a, C_b, C_{12} = 0.2\text{ }\mu\text{F}$ +100% -10%	-4.7	-4.5	-4.1	V	
V_{SSL} Voltage	V_{SSL}	—	-1.9	-1.3	-0.6	V	
Crystal Oscillation Start Voltage	V_{STA}	Oscillation start time: within 5 seconds	—	—	-0.9	V	
Crystal Oscillation Hold Voltage	V_{HOLD}	—	—	—	-0.9	V	
Crystal Oscillation Stop Detection Time	T_{STOP}	—	0.1	—	1000	ms	
Internal Crystal Oscillator Capacitance	C_G	—	12	15	20	pF	
External Crystal Oscillator Capacitance	C_{GEX}	When external C_G used	12	—	30	pF	
Internal Crystal Oscillator Capacitance	C_D	—	12	15	20	pF	
POR Generation Voltage	V_{POR1}	When V_{SS1} is between V_{POR1} and -1.5 V	-0.4	—	0	V	
POR Non-generation Voltage	V_{POR2}	No POR when V_{SS1} is between V_{POR2} and -1.5 V	-1.5	—	-1.2	V	
Supply Current 1	I_{DD1}	CPU in halt state	$T_a = -10\text{ to }+30^\circ\text{C}$	—	3	5	μA
			$T_a = +30\text{ to }+65^\circ\text{C}$	—	3	20	μA
Supply Current 2	I_{DD2}	CPU in operating state	$T_a = -10\text{ to }+30^\circ\text{C}$	—	8	15	μA
			$T_a = +30\text{ to }+65^\circ\text{C}$	—	8	25	μA
Supply Current 3	I_{DD3}	Serial transfer, $f_{SCK} = 300\text{ kHz}$, CPU in operating state	$T_a = -10\text{ to }+30^\circ\text{C}$	—	10	25	μA
			$T_a = +30\text{ to }+65^\circ\text{C}$	—	10	40	μA

Notes: 1. "POR" denotes Power On Reset.

2. " T_{STOP} " indicates that if the crystal oscillator stops over the value of T_{STOP} , the system reset occurs.

DC Characteristics (continued)

($V_{DD} = 0\text{ V}$, $V_{SS1} = V_{SSL} = V_{SS} = -1.5\text{ V}$, $V_{SS2} = -3.0\text{ V}$, $V_{SS3} = -4.5\text{ V}$,
 $T_a = -10\text{ to }+65^\circ\text{C}$ unless otherwise specified)

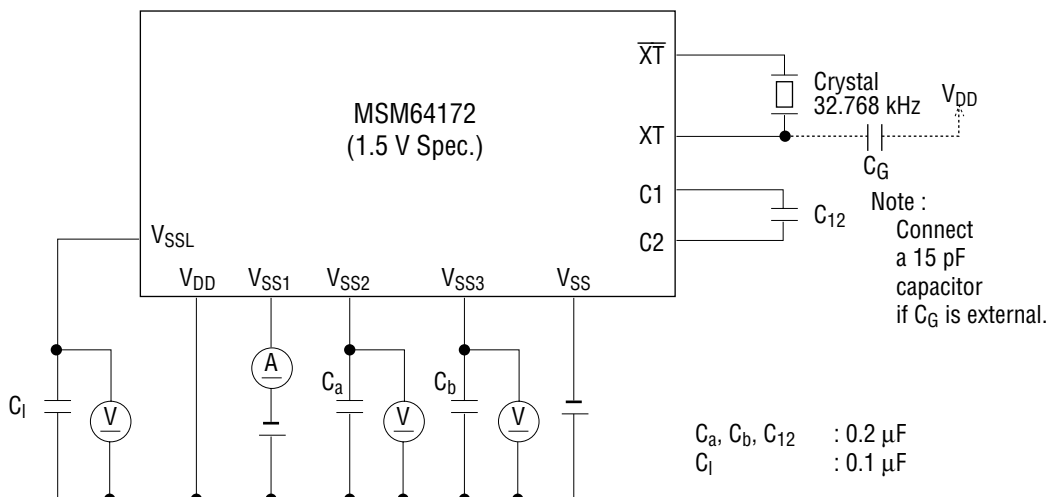
Parameter (Pin Name)	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Output Current 1 (P1.0 to P1.3) (P2.0 to P2.3)	I_{OH1}	$V_{OH1} = -0.5\text{ V}$	-2.1	-0.7	-0.2	mA	2
	I_{OL1}	$V_{OL1} = V_{SS} + 0.5\text{ V}$	0.2	0.7	2.1	mA	
	I_{OH1S}	$V_{SS} = -5\text{ V}$, $V_{OH1S} = -0.5\text{ V}$	-9.0	-3.0	-1.0	mA	
	I_{OL1S}	$V_{SS} = -5\text{ V}$, $V_{OL1} = V_{SS} + 0.5\text{ V}$	1.0	3.0	9.0	mA	
Output Current 2 (BD)	I_{OH2}	$V_{OH2} = -0.7\text{ V}$	-1.8	-0.6	-0.2	mA	
	I_{OL2}	$V_{OL2} = V_{SS1} + 0.7\text{ V}$	0.2	0.6	1.8	mA	
Output Current 3 (When S0 to S15 are configured as output ports) (P3.0 to P3.3) (P4.0 to P4.3) (P5.0 to P5.3) (P6.0 to P6.3)	I_{OH3}	$V_{OH3} = -0.5\text{ V}$	-1.5	-0.5	-0.1	mA	
	I_{OL3}	$V_{OL3} = V_{SS} + 0.5\text{ V}$	0.1	0.5	1.5	mA	
	I_{OH3S}	$V_{SS} = -5\text{ V}$, $V_{OH3S} = -0.5\text{ V}$	-2.0	-0.7	-0.2	mA	
	I_{OL3S}	$V_{SS} = -5\text{ V}$, $V_{OL3S} = V_{SS} + 0.5\text{ V}$	0.2	0.7	2.0	mA	
Output Current 4 (S0 to S22) (COM0 to COM3)	I_{OH4}	$V_{OH4} = -0.2\text{ V}$ (V_{DD} level)	—	—	-4.0	μA	
	I_{OMH4}	$V_{OMH4} = V_{SS1} + 0.2\text{ V}$ (V_{SS1} level)	4.0	—	—	μA	
	I_{OMH4S}	$V_{OMH4S} = V_{SS1} - 0.2\text{ V}$ (V_{SS1} level)	—	—	-4.0	μA	
	I_{OML4}	$V_{OML4} = V_{SS2} + 0.2\text{ V}$ (V_{SS2} level)	4.0	—	—	μA	
	I_{OML4S}	$V_{OML4S} = V_{SS2} - 0.2\text{ V}$ (V_{SS2} level)	—	—	-4.0	μA	
	I_{OL4}	$V_{OL4} = V_{SS3} + 0.2\text{ V}$ (V_{SS3} level)	4.0	—	—	μA	
Output Leakage Current (P1.0 to P1.3) (P2.0 to P2.3)	I_{OOH}	$V_{OH} = V_{DD}$	—	—	0.3	μA	
	I_{OOL}	$V_{OL} = V_{SS}$	-0.3	—	—	μA	

DC Characteristics (continued)

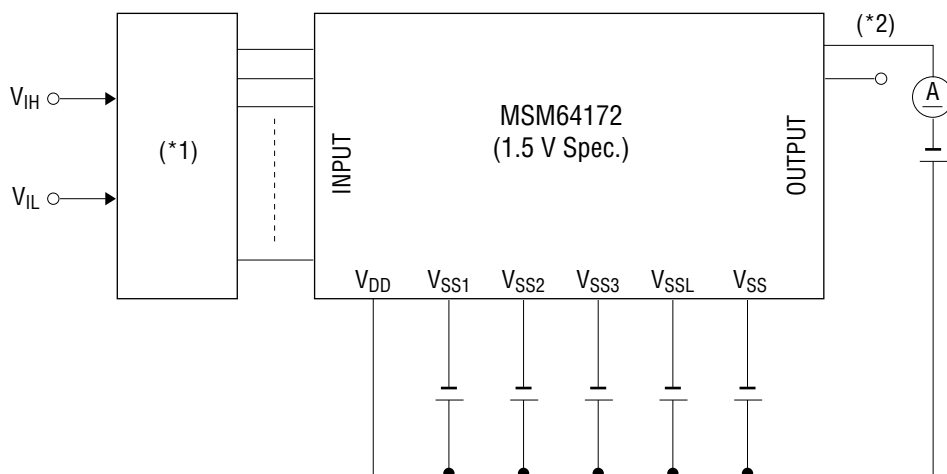
($V_{DD} = 0\text{ V}$, $V_{SS1} = V_{SSL} = V_{SS} = -1.5\text{ V}$, $V_{SS2} = -3.0\text{ V}$, $V_{SS3} = -4.5\text{ V}$,
 $T_a = -10\text{ to }+65^\circ\text{C}$ unless otherwise specified)

Parameter (Pin Name)	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Input Current 1 (P0.0 to P0.3) (P1.0 to P1.3) (P2.0 to P2.3)	I_{IH1}	$V_{IH1} = V_{DD}$ (when pulled down)	5.0	18	60	μA	3
	I_{IL1}	$V_{IL1} = V_{SS}$ (when pulled up)	-60	-18	-5.0	μA	
	I_{IH1S}	$V_{IH1} = V_{DD}$, $V_{SS} = -5\text{ V}$ (when pulled down)	70	250	660	μA	
	I_{IL1S}	$V_{IL1} = V_{SS} = -5\text{ V}$ (when pulled up)	-660	-250	-70	μA	
	I_{IH1Z}	$V_{IH1} = V_{DD}$ (in a high impedance state)	0	—	1.0	μA	
	I_{IL1Z}	$V_{IL1} = V_{SS}$ (in a high impedance state)	-1.0	—	0	μA	
Input Current 2 (OSC1)	I_{IH2}	$V_{IH2} = V_{DD}$	0	—	1.0	μA	4
	I_{IL2}	$V_{IL2} = V_{SS1}$	-60	-22	-6.0	μA	
Input Current 3 (RESET, TST1, TST2)	I_{IH3}	$V_{IH3} = V_{DD}$	0	—	1.0	μA	
	I_{IL3}	$V_{IL3} = V_{SS1}$	-1.5	-0.75	-0.3	mA	
Input Voltage 1 (P0.0 to P0.3) (P1.0 to P1.3) (P2.0 to P2.3)	V_{IH1}	—	-0.3	—	0	V	
	V_{IL1}	—	-1.5	—	-1.2	V	
	V_{IH1S}	$V_{SS} = -5\text{ V}$	-1.0	—	0	V	
	V_{IL1S}	$V_{SS} = -5\text{ V}$	-5.0	—	-4.0	V	
Input Voltage 2 (RESET, TST1, TST2)	V_{IH2}	—	-0.3	—	0	V	4
	V_{IL2}	—	-1.5	—	-1.2	V	
Hysteresis Width (P0.0 to P0.3) (P1.0 to P1.3) (P2.0 to P2.3)	ΔV_{T1}	—	0.05	0.1	0.3	V	
	ΔV_{T1S}	$V_{SS} = -5\text{ V}$	0.25	1.0	1.5	V	
Hysteresis Width (RESET, TST1, TST2)	ΔV_{T2}	—	0.05	0.1	0.3	V	
Input Pin Capacitance (P0.0 to P0.3) (P1.0 to P1.3) (P2.0 to P2.3)	C_{IN}	—	—	—	5.0	pF	1

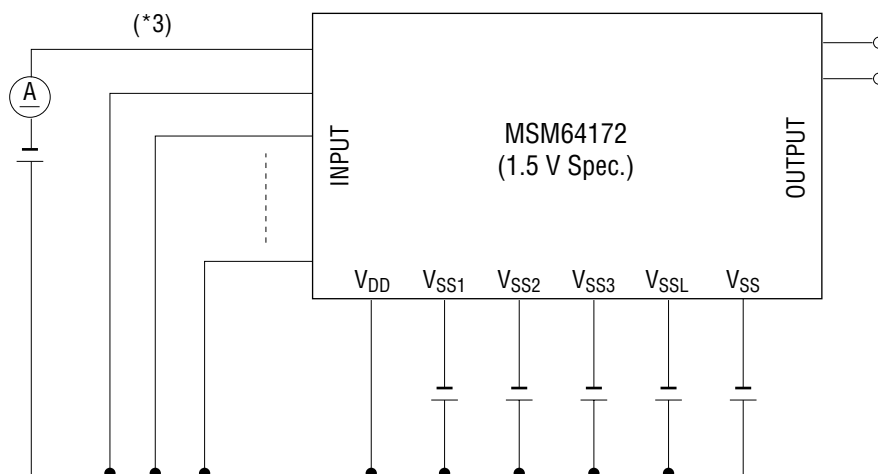
Measuring circuit 1



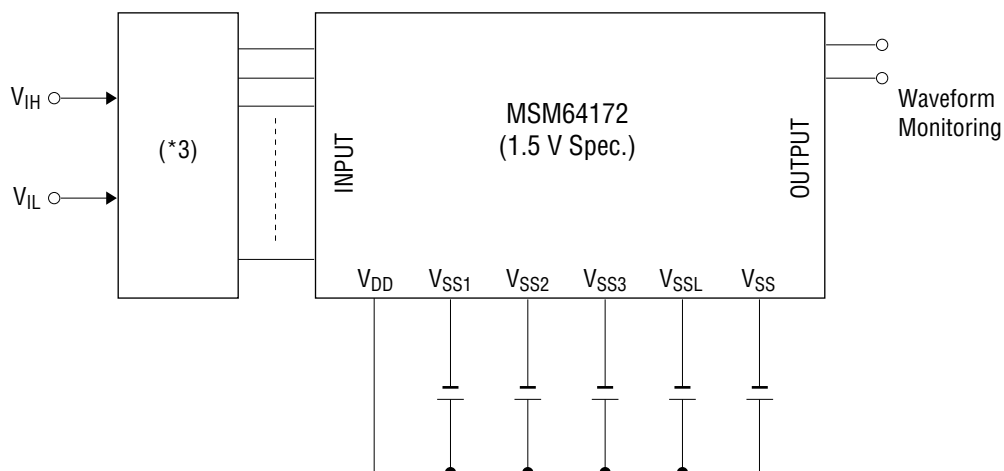
Measuring circuit 2



Measuring circuit 3



Measuring circuit 4



*1 Input logic circuit to determine the specified measuring conditions.

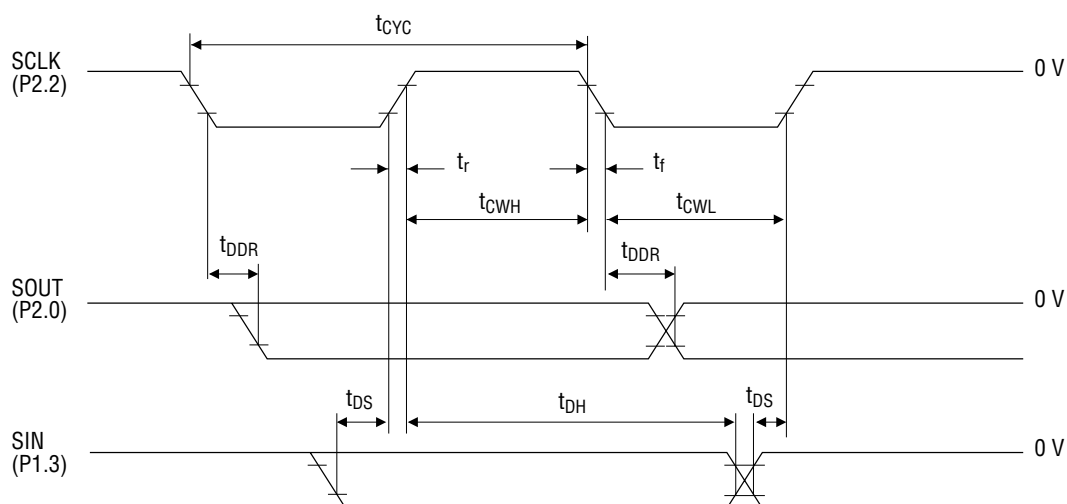
*2 Measured at the specified output pins.

*3 Measured at the specified input pins.

AC Characteristics (Serial Interface)(V_{DD} = 0 V, V_{SS1} = -1.5 V, V_{SS} = -5 V, Ta = -10 to +65°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCLK Input Fall Time	t _f	—	—	—	1.0	μs
SCLK Input Rise Time	t _r	—	—	—	1.0	μs
SCLK Input "L" Level Pulse Width	t _{CWL}	—	0.8	—	—	μs
SCLK Input "H" Level Pulse Width	t _{CWH}	—	0.8	—	—	μs
SCLK Input Cycle Time	t _{CYC}	V _{SS} = -5.25 V to V _{SS1}	1.8	—	—	μs
SCLK Output Cycle Time	t _{CYC1(0)}	CPU operating at 32.768 kHz	—	30.5	—	μs
SOUT Output Delay Time	t _{DDR}	C _I = 10 pF	—	—	0.4	μs
SIN Input Setup Time	t _{DS}	—	0.5	—	—	μs
SIN Input Hold Time	t _{DH}	—	0.8	—	—	μs

AC characteristics timing

("H" level = 0.2 · V_{SS}, "L" level = 0.8 · V_{SS})

ABSOLUTE MAXIMUM RATINGS (3.0 V Spec.)(V_{DD} = 0 V)

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage 1	V _{SS1}	Ta = 25°C	–2.0 to +0.3	V
Power Supply Voltage 2	V _{SS2}	Ta = 25°C	–4.0 to +0.3	V
Power Supply Voltage 3	V _{SS3}	Ta = 25°C	–5.5 to +0.3	V
Power Supply Voltage 4	V _{SSL}	Ta = 25°C	–4.0 to +0.3	V
Power Supply Voltage 5	V _{SS}	Ta = 25°C	–5.5 to +0.3	V
Input Voltage 1	V _{IN1}	V _{SS2} Input, Ta = 25°C	V _{SS2} – 0.3 to +0.3	V
Input Voltage 2	V _{IN2}	V _{SS} Input, Ta = 25°C	V _{SS} – 0.3 to +0.3	V
Input Voltage 3	V _{IN3}	V _{SSL} Input, Ta = 25°C	V _{SSL} – 0.3 to +0.3	V
Output Voltage 1	V _{OUT1}	V _{SS2} Output, Ta = 25°C	V _{SS2} – 0.3 to +0.3	V
Output Voltage 2	V _{OUT2}	V _{SS3} Output, Ta = 25°C	V _{SS3} – 0.3 to +0.3	V
Output Voltage 3	V _{OUT3}	V _{SS} Output, Ta = 25°C	V _{SS} – 0.3 to +0.3	V
Output Voltage 4	V _{OUT4}	V _{SSL} Output, Ta = 25°C	V _{SSL} – 0.3 to +0.3	V
Storage Temperature	T _{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS (3.0 V Spec.)(V_{DD} = 0 V)

Parameter	Symbol	Condition	Range	Unit
Operating Temperature	T _{op}	—	–10 to +65	°C
Operating Voltage	V _{SS2}	—	–3.6 to –1.8	V
	V _{SS}	—	–5.25 to –1.8	V
External RC Oscillator Resistance	R _{OS}	—	90 to 500	kΩ
Crystal Oscillation Frequency	f _{XT}	—	30 to 66	kHz
Ceramic Resonator Oscillation Frequency	f _{CM}	V _{SS2} = –3.6 V to –2.2 V	200 to 600	kHz

ELECTRICAL CHARACTERISTICS (3.0 V Spec.)

DC Characteristics

($V_{DD} = 0\text{ V}$, $V_{SS2} = V_{SS} = -3.0\text{ V}$, $T_a = -10\text{ to }+65^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
V_{SS1} Voltage	V_{SS1}	$C_a, C_b, C_{12} = 0.1\text{ }\mu\text{F}$ +100% -50%	-1.7	-1.5	-1.3	V	1
V_{SS3} Voltage	V_{SS3}	$C_a, C_b, C_{12} = 0.1\text{ }\mu\text{F}$ +100% -50%	-4.7	-4.5	-4.3	V	
V_{SSL} Voltage	V_{SSL}	—	-1.9	-1.3	-0.6	V	
Crystal Oscillation Start Voltage	V_{STA}	Oscillation start time: within 5 seconds	—	—	-1.8	V	
Crystal Oscillation Hold Voltage	V_{HOLD}	—	—	—	-1.8	V	
Crystal Oscillation Stop Detection Time	T_{STOP}	—	0.1	—	1000	ms	
Internal Crystal Oscillator Capacitance	C_G	—	12	15	20	pF	
External Crystal Oscillator Capacitance	C_{GEX}	When external C_G used	12	—	30	pF	
Internal Crystal Oscillator Capacitance	C_D	—	12	15	20	pF	
Internal RC Oscillator Capacitance	C_{OS}	—	8.0	12	16	pF	
RC Oscillation Frequency	f_{OSC}	External resistor $R_{OS} = 100\text{ k}\Omega$ $V_{SS2} = -1.8\text{ to }-3.6\text{ V}$	280	560	800	kHz	
POR Generation Voltage	V_{POR1}	When V_{SS2} is between V_{POR1} and -3.0 V	-0.7	—	0	V	
POR Non-generation Voltage	V_{POR2}	No POR when V_{SS2} is between V_{POR2} and -3.0 V	-3.0	—	-2.0	V	

Notes: 1. "POR" denotes Power On Reset.

2. " T_{STOP} " indicates that if the crystal oscillator stops over the value of T_{STOP} , the system reset occurs.

DC Characteristics (continued)

($V_{DD} = 0\text{ V}$, $V_{SS2} = V_{SS} = -3.0\text{ V}$, $T_a = -10\text{ to }+65^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Supply Current 1	I_{DD1}	CPU in halt state (High-speed clock oscillation stop)	$T_a = -10\text{ to }+30^\circ\text{C}$	—	1.5	3	μA
			$T_a = +30\text{ to }+65^\circ\text{C}$	—	1.5	15	μA
Supply Current 2	I_{DD2}	CPU in operating state (High-speed clock oscillation stop)	$T_a = -10\text{ to }+30^\circ\text{C}$	—	5.0	13	μA
			$T_a = +30\text{ to }+65^\circ\text{C}$	—	5.0	25	μA
Supply Current 3	I_{DD3}	CPU operating at 400 kHz (RC oscillation)	—	220	500	μA	1
Supply Current 4	I_{DD4}	CPU operating at 500 kHz (ceramic oscillation)	—	170	400	μA	
Supply Current 5	I_{DD5}	Serial transfer, $f_{SCK} = 300\text{ kHz}$, CPU in operating state	$T_a = -10\text{ to }+30^\circ\text{C}$	—	7.0	25	μA
		(High-speed clock oscillation stop)	$T_a = +30\text{ to }+65^\circ\text{C}$	—	7.0	40	μA

DC Characteristics (continued)

($V_{DD} = 0\text{ V}$, $V_{SS1} = V_{SSL} = -1.5\text{ V}$, $V_{SS2} = V_{SS} = -3.0\text{ V}$, $V_{SS3} = -4.5\text{ V}$,
 $T_a = -10\text{ to }+65^\circ\text{C}$ unless otherwise specified)

Parameter (Pin Name)	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Output Current 1 (P1.0 to P1.3) (P2.0 to P2.3)	I_{OH1}	$V_{OH1} = -0.5\text{ V}$	-6.0	-2.0	-0.7	mA	2
	I_{OL1}	$V_{OL1} = V_{SS} + 0.5\text{ V}$	0.7	2.0	6.0	mA	
	I_{OH1S}	$V_{SS} = -5\text{ V}$, $V_{OH1S} = -0.5\text{ V}$	-9.0	-3.0	-1.0	mA	
	I_{OL1S}	$V_{SS} = -5\text{ V}$, $V_{OL1} = V_{SS} + 0.5\text{ V}$	1.0	3.0	9.0	mA	
Output Current 2 (BD)	I_{OH2}	$V_{OH2} = -0.7\text{ V}$	-6.0	-2.0	-0.7	mA	
	I_{OL2}	$V_{OL2} = V_{SS2} + 0.7\text{ V}$	0.7	2.0	6.0	mA	
Output Current 3 (When S0 to S15 are configured as output ports) (P3.0 to P3.3) (P4.0 to P4.3) (P5.0 to P5.3) (P6.0 to P6.3)	I_{OH3}	$V_{OH3} = -0.5\text{ V}$	-1.5	-0.6	-0.15	mA	
	I_{OL3}	$V_{OL3} = V_{SS} + 0.5\text{ V}$	0.15	0.6	1.5	mA	
	I_{OH3S}	$V_{SS} = -5\text{ V}$, $V_{OH3S} = -0.5\text{ V}$	-2.0	-0.7	-0.2	mA	
	I_{OL3S}	$V_{SS} = -5\text{ V}$, $V_{OL3S} = V_{SS} + 0.5\text{ V}$	0.2	0.7	2.0	mA	
Output Current 4 (S0 to S22) (COM0 to COM3)	I_{OH4}	$V_{OH4} = -0.2\text{ V}$ (V_{DD} level)	—	—	-4.0	μA	
	I_{OMH4}	$V_{OMH4} = V_{SS1} + 0.2\text{ V}$ (V_{SS1} level)	4.0	—	—	μA	
	I_{OMH4S}	$V_{OMH4S} = V_{SS1} - 0.2\text{ V}$ (V_{SS1} level)	—	—	-4.0	μA	
	I_{OML4}	$V_{OML4} = V_{SS2} + 0.2\text{ V}$ (V_{SS2} level)	4.0	—	—	μA	
	I_{OML4S}	$V_{OML4S} = V_{SS2} - 0.2\text{ V}$ (V_{SS2} level)	—	—	-4.0	μA	
	I_{OL4}	$V_{OL4} = V_{SS3} + 0.2\text{ V}$ (V_{SS3} level)	4.0	—	—	μA	
Output Current 5 (OSC2)	I_{OH5R}	$V_{OH5R} = -0.5\text{ V}$ (RC oscillation mode)	-6.0	-2.0	-0.7	mA	
	I_{OL5R}	$V_{OL5R} = V_{SS} + 0.5\text{ V}$ (RC oscillation mode)	0.7	2.0	6.0	mA	
	I_{OH5C}	$V_{OH5C} = -0.5\text{ V}$ (ceramic oscillation mode)	-100	-35	-10	μA	
	I_{OL5C}	$V_{OL5C} = V_{SS2} + 0.5\text{ V}$ (ceramic oscillation mode)	10	35	100	μA	
Output Leakage Current (P1.0 to P1.3) (P2.0 to P2.3)	I_{OOH}	$V_{OH} = V_{DD}$	—	—	0.3	μA	
	I_{OOL}	$V_{OL} = V_{SS}$	-0.3	—	—	μA	

DC Characteristics (continued)

($V_{DD} = 0\text{ V}$, $V_{SS1} = V_{SSL} = -1.5\text{ V}$, $V_{SS2} = V_{SS} = -3.0\text{ V}$, $V_{SS3} = -4.5\text{ V}$,
 $T_a = -10\text{ to }+65^\circ\text{C}$ unless otherwise specified)

Parameter (Pin Name)	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Input Current 1 (P0.0 to P0.3) (P1.0 to P1.3) (P2.0 to P2.3)	I_{IH1}	$V_{IH1} = V_{DD}$ (when pulled down)	30	90	300	μA	3
	I_{IL1}	$V_{IL1} = V_{SS}$ (when pulled up)	-300	-90	-30	μA	
	I_{IH1S}	$V_{IH1} = V_{DD}$, $V_{SS} = -5\text{ V}$ (when pulled down)	80	250	800	μA	
	I_{IL1S}	$V_{IL1} = V_{SS} = -5\text{ V}$ (when pulled up)	-800	-250	-80	μA	
	I_{IH1Z}	$V_{IH1} = V_{DD}$ (in a high impedance state)	0	—	1.0	μA	
	I_{IL1Z}	$V_{IL1} = V_{SS}$ (in a high impedance state)	-1.0	—	0	μA	
Input Current 2 (OSC1)	I_{IL2}	$V_{IL2} = V_{SS2}$ (when pulled up)	-300	-110	-30	μA	
	I_{IH2Z}	$V_{IH2} = V_{DD}$ (RC oscillation mode)	0	—	1	μA	
	I_{IL2Z}	$V_{IL2} = V_{SS2}$ (RC oscillation mode)	-1	—	0	μA	
	I_{IH2C}	$V_{IH2} = V_{DD}$ (ceramic oscillation mode)	0.75	1.5	3	μA	
	I_{IL2C}	$V_{IL2} = V_{SS2}$ (ceramic oscillation mode)	-3	-1.5	-0.75	μA	
Input Current 3 (RESET, TST1, TST2)	I_{IH3}	$V_{IH3} = V_{DD}$	0	—	1.0	μA	
	I_{IL3}	$V_{IL3} = V_{SS2}$	-3.0	-1.5	-0.75	mA	
Input Voltage 1 (P0.0 to P0.3) (P1.0 to P1.3) (P2.0 to P2.3)	V_{IH1}	—	-0.6	—	0	V	4
	V_{IL1}	—	-3.0	—	-2.4	V	
	V_{IH1S}	$V_{SS} = -5\text{ V}$	-1.0	—	0	V	
	V_{IL1S}	$V_{SS} = -5\text{ V}$	-5.0	—	-4.0	V	
Input Voltage 2 (OSC1)	V_{IH2}	—	-0.6	—	0	V	
	V_{IL2}	—	-3.0	—	-2.4	V	
Input Voltage 3 (RESET, TST1, TST2)	V_{IH3}	—	-0.6	—	0	V	
	V_{IL3}	—	-3.0	—	-2.4	V	

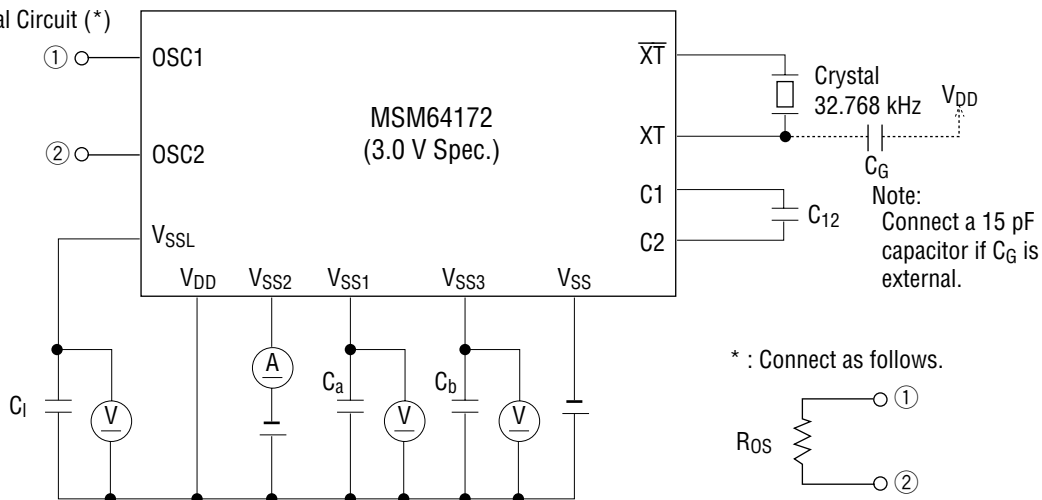
DC Characteristics (continued)

($V_{DD} = 0\text{ V}$, $V_{SS1} = V_{SSL} = -1.5\text{ V}$, $V_{SS2} = V_{SS} = -3.0\text{ V}$, $V_{SS3} = -4.5\text{ V}$,
 $T_a = -10\text{ to }+65^\circ\text{C}$ unless otherwise specified)

Parameter (Pin Name)	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Hysteresis Width (P0.0 to P0.3) (P1.0 to P1.3) (P2.0 to P2.3)	ΔV_{T1}	—	0.2	0.5	1.0	V	4
	ΔV_{T1S}	$V_{SS} = -5\text{ V}$	0.25	1.0	1.5	V	
Hysteresis Width (RESET, TST1, TST2)	ΔV_{T2}	—	0.2	0.5	1.0	V	
Input Pin Capacitance (P0.0 to P0.3) (P1.0 to P1.3) (P2.0 to P2.3)	C_{IN}	—	—	—	5.0	pF	1

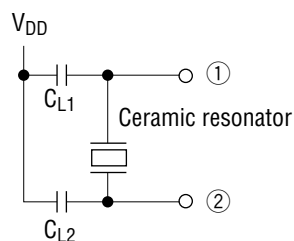
Measuring circuit 1

External Circuit (*)

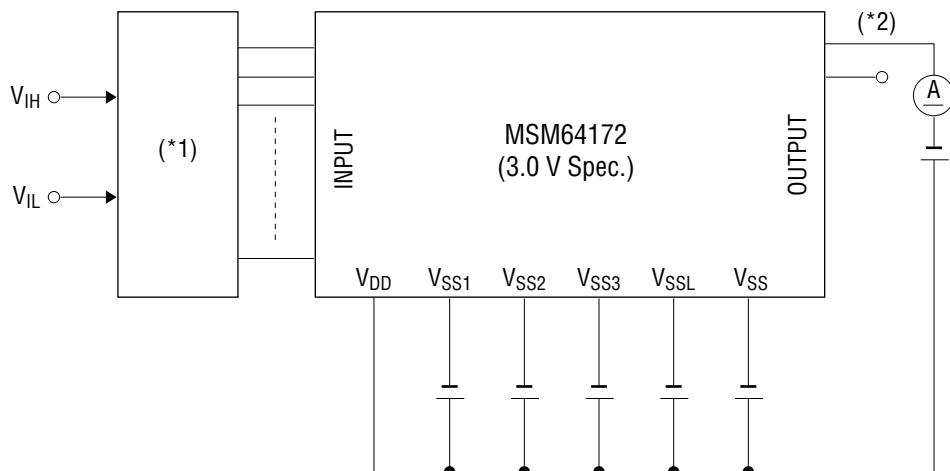


C_a, C_b, C_{12} : 0.1 μ F
 C_I : 0.47 μ F
 R_{0S} : 100 k Ω
 C_{L1} : 100 pF
 C_{L2} : 100 pF
 Ceramic resonator : CSB500E (500 kHz)
 (Murata MFG.-make)

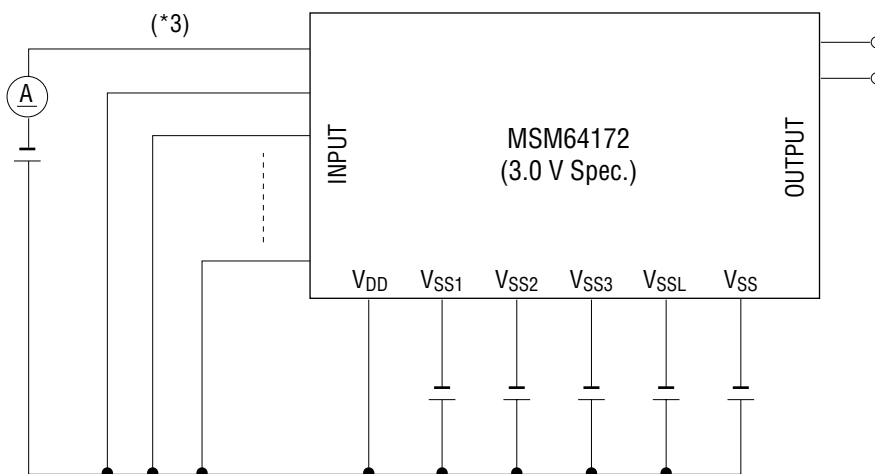
In ceramic resonator oscillation mode



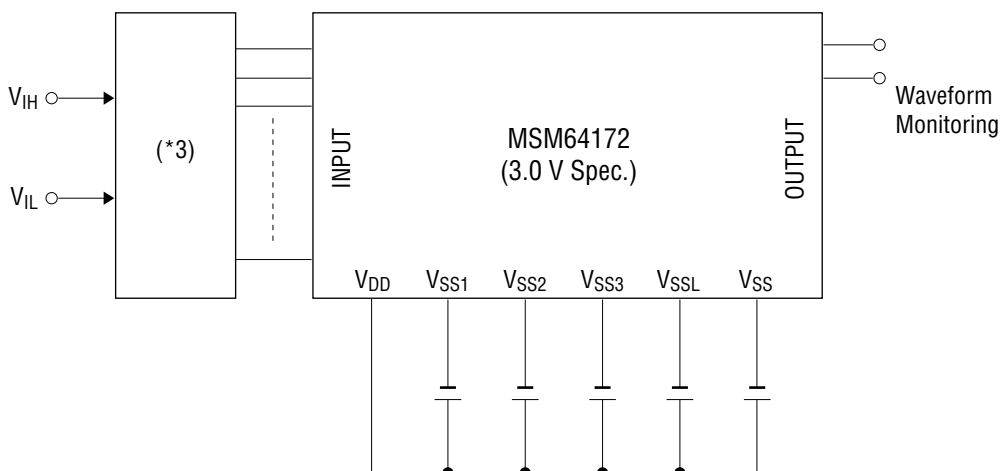
Measuring circuit 2



Measuring circuit 3



Measuring circuit 4



*1 Input logic circuit to determine the specified measuring conditions.

*2 Measured at the specified output pins.

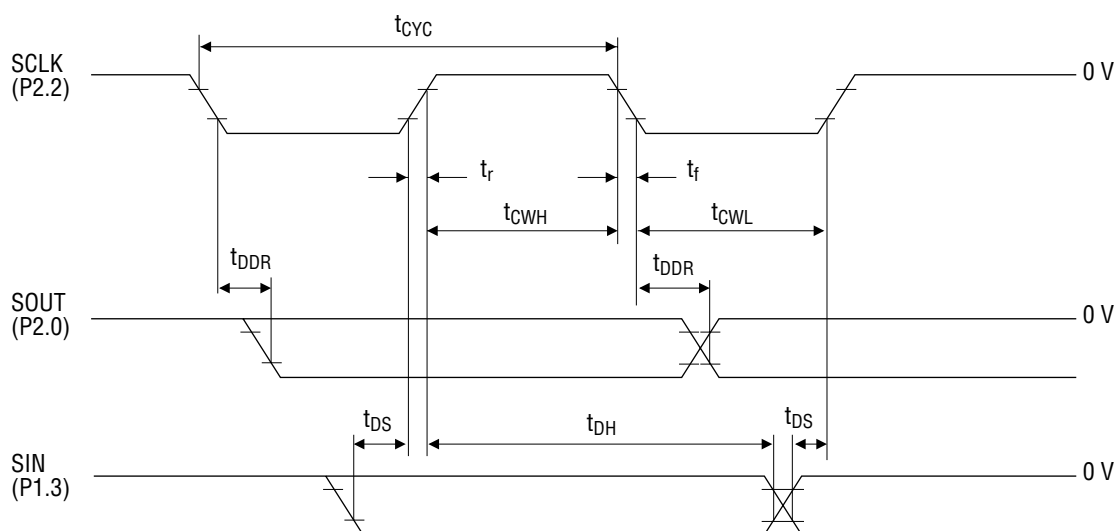
*3 Measured at the specified input pins.

AC Characteristics (Serial Interface)

(V_{DD} = 0 V, V_{SS2} = -3 V, V_{SS} = -5 V, Ta = -10 to +65°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCLK Input Fall Time	t _f	—	—	—	1.0	μs
SCLK Input Rise Time	t _r	—	—	—	1.0	μs
SCLK Input "L" Level Pulse Width	t _{CWL}	—	0.8	—	—	μs
SCLK Input "H" Level Pulse Width	t _{CWH}	—	0.8	—	—	μs
SCLK Input Cycle Time	t _{CYC}	V _{SS} = -5.25 V to -2.4 V	1.8	—	—	μs
SCLK Output Cycle Time	t _{CYC1(0)}	CPU operating at 32.768 kHz	—	30.5	—	μs
SCLK Output Cycle Time	t _{CYC2(0)}	CPU operating at 500 kHz	—	2.0	—	μs
SOUT Output Delay Time	t _{DDR}	C _I = 10 pF	—	—	0.4	μs
SIN Input Setup Time	t _{DS}	—	0.5	—	—	μs
SIN Input Hold Time	t _{DH}	—	0.8	—	—	μs

AC characteristics timing

("H" level = 0.2 · V_{SS}, "L" level = 0.8 · V_{SS})

FUNCTIONAL DESCRIPTION

CPU Peripheral Functions

• Serial port (SIOP)

The MSM64172 has an 8-bit synchronous serial port. Receive/transmit operation of the serial port is performed simultaneously and the serial transfer clock can select either internal or external mode. Direction of transfer data can be big endian or little endian. Each pin of the serial port is assigned as secondary functions of P1.3 and P2.0 to P2.2. Setting each bit of SIN, SOUT, SPR, and SCLK of P13CON and P20CON to P22CON to "1" makes each pin valid.

• LCD driver (LCD)

The MSM64172 has a built-in LCD driver for 27 outputs.

The LCD driver consists of display registers (DSPR0-30), the Display Control Register (DSPCON), a 27-output LCD driver circuit, and a bias generation circuit (BIAS).

There are three types of driving methods: 1/4 duty, 1/3 duty, and 1/2 duty. Software selects the duty mode.

S0 to S15 of the LCD driver can be configured to be output ports by a mask option.

The relationship between the duty, the bias method, and the maximum segment number follows:

1/4 duty 1/3 bias method	-----	92 segments (COM0-3, S0-22)
1/3 duty 1/3 bias method	-----	72 segments (COM0-2, S0-23)
1/2 duty 1/2 bias method	-----	50 segments (COM0, 1, S0-24)

• Buzzer driver (BD)

The MSM64172 has a built-in buzzer driver with 2 buzzer output frequencies and 4 buzzer output modes. Each buzzer output is selected by the Buzzer Control Register (BDCON) and the Buzzer Frequency Control Register (BFCON).

• Watchdog timer (WDT)

The MSM64172 has a built-in watchdog timer to detect CPU malfunction. The watchdog timer is composed of a 6-bit watchdog timer counter (WDTC) to count a 16 Hz output and a watchdog timer control register (WDTCN) to reset WDTC.

• Clock generation circuit (2CLK)

The Clock Generation Circuit (2CLK) consists of a 32.768 kHz crystal oscillation circuit, a high-speed clock generation circuit, and clock control logic. 2CLK generates the system clock (CLK) and the time-base clock (32.768 kHz).

The high-speed clock generation circuit is available only for use in 3 V operation, and offers two modes, the RC Oscillation Mode and the Ceramic Resonator Oscillation Mode.

The system clock is the source clock for the CPU. The time-base clock is the source clock for the TBC and BD.

The system clock frequency is 32.768 kHz, which is output from the crystal oscillation circuit in 1.5 V operation. In 3.0 V operation, the system clock can be switched to 32.768 kHz, which is output from the crystal oscillation circuit, or to the frequency that is output from the high-speed clock oscillation circuit by controlling the contents of Frequency Control Register (FCON). The desired high-speed clock oscillation circuit mode also can be selected by using FCON.

- **Time base counter (TBC)**

The MSM64172 has a built-in time base counter (TBC) that generates clocks to be supplied to internal peripheral circuits. The time base counter is composed of 15 binary counters. The count clock of the time base is driven by the oscillation clock (32.768 kHz) of the crystal oscillation circuit. The output of the time base counter is used for the buzzer driver, the system reset circuit, the watchdog timer, the time base interrupt, and the sampling clocks of each port.

- **I/O port**

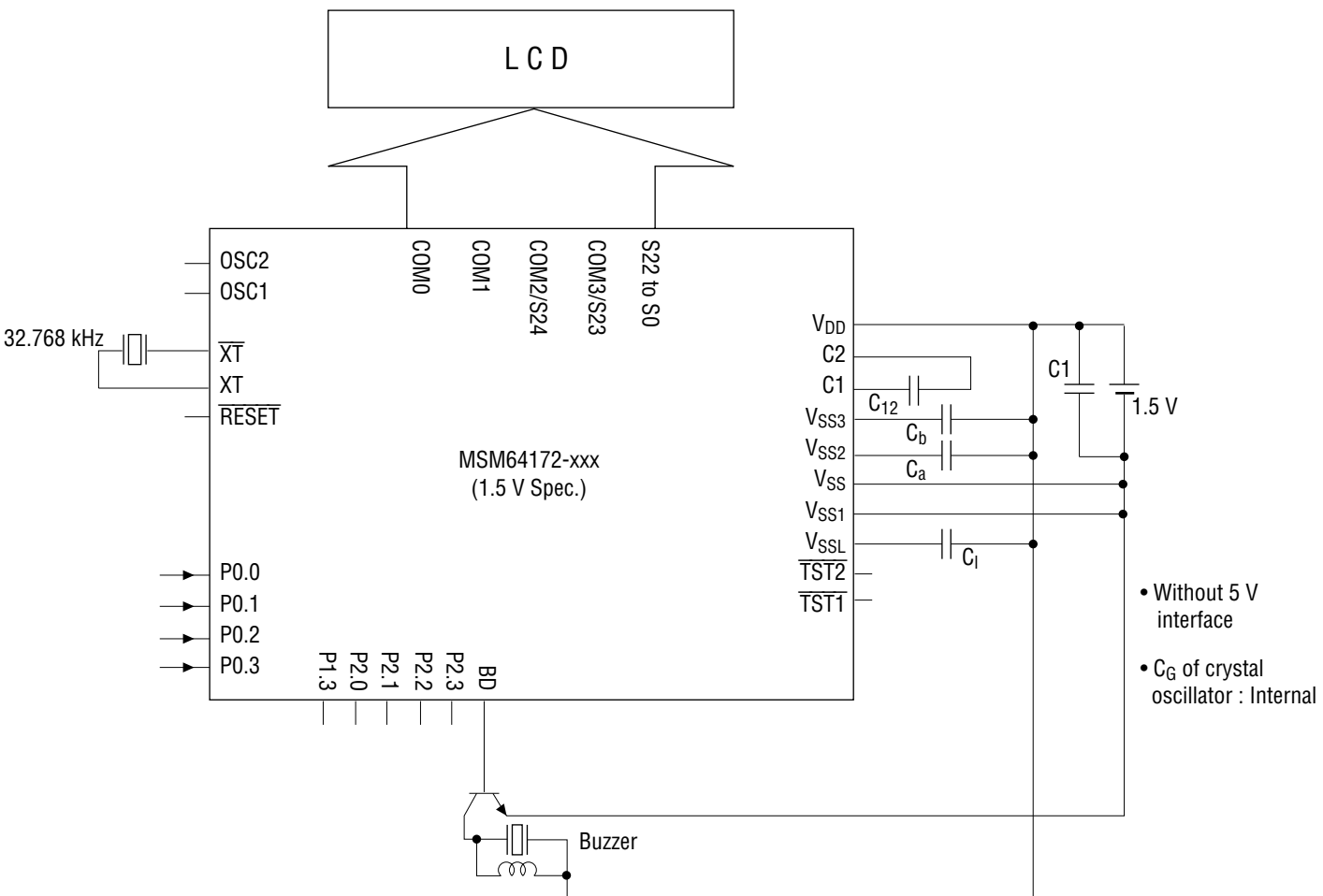
Input-output ports (P1, P2) (8 bits)	: Pull-up (pull-down) resistor input or high-impedance input, CMOS output or NMOS open drain output: these can be specified for each bit; external 0 interrupt
Input port (P0) (4 bits)	: Pull-up (pull-down) resistor input or high-impedance input; external 1 interrupt

- **Interrupt (INTC)**

The MSM64172 has seven interrupt sources (seven vector addresses), of which two are external interrupts from ports and five are internal interrupts.

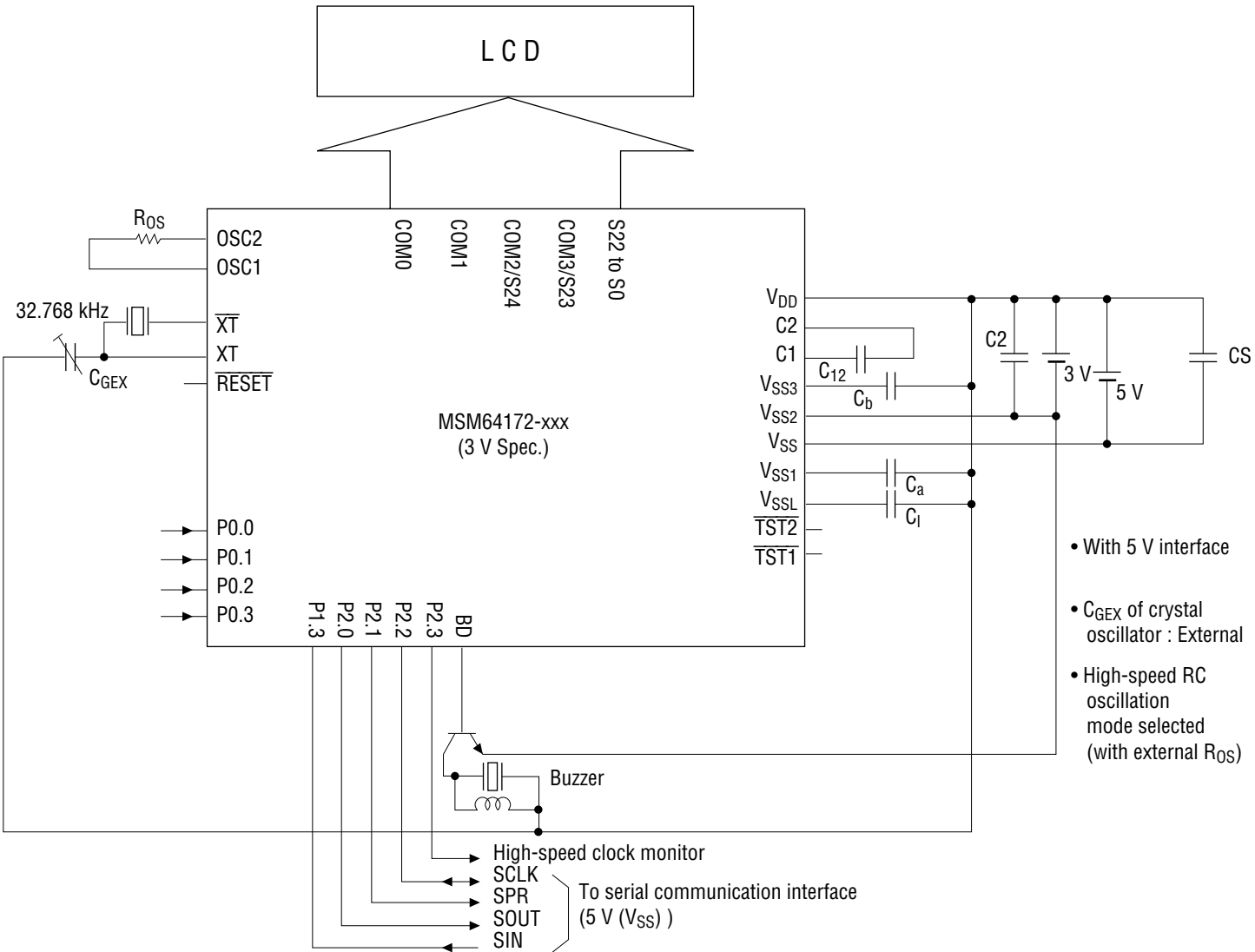
Of the seven interrupt sources, only the watchdog interrupt cannot be disabled (non-maskable interrupt). The other six interrupts are controlled by the master interrupt enable flag (MI) and the interrupt enable registers (IE0 and IE1). When an interrupt condition is met, the CPU branches to a vector address corresponding to the interrupt source.

APPLICATION CIRCUITS



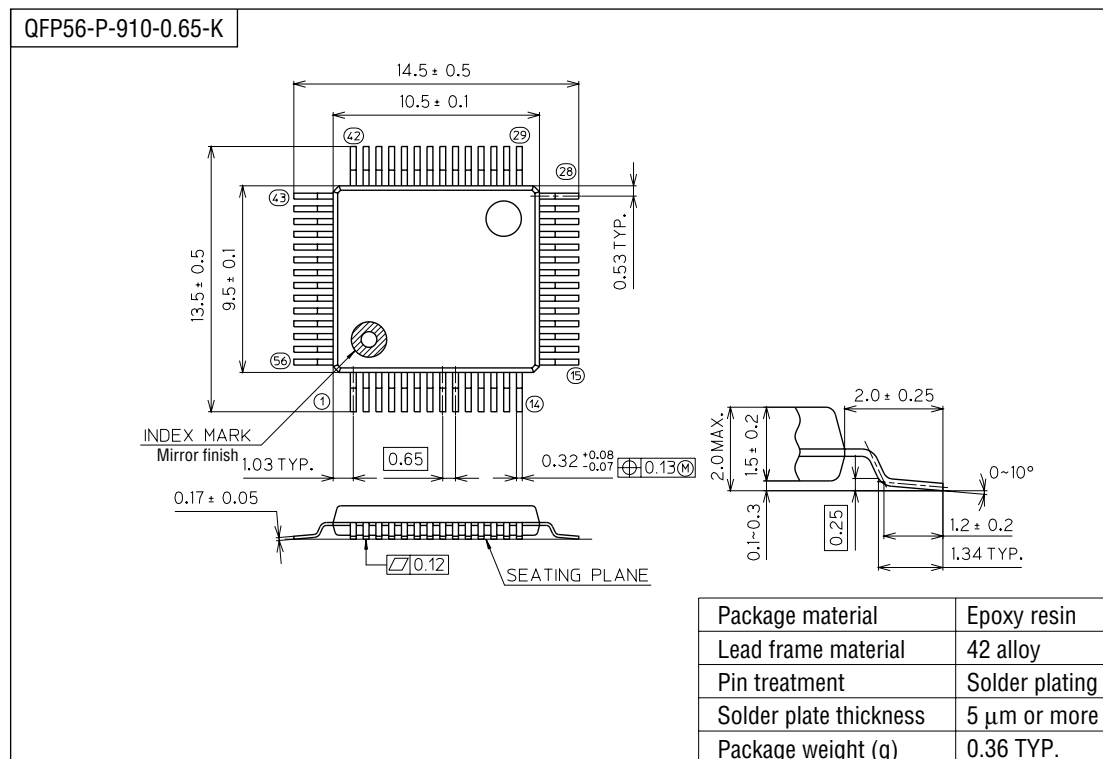
1.5 V Spec. Application Circuit

APPLICATION CIRCUITS (continued)



PACKAGE DIMENSIONS

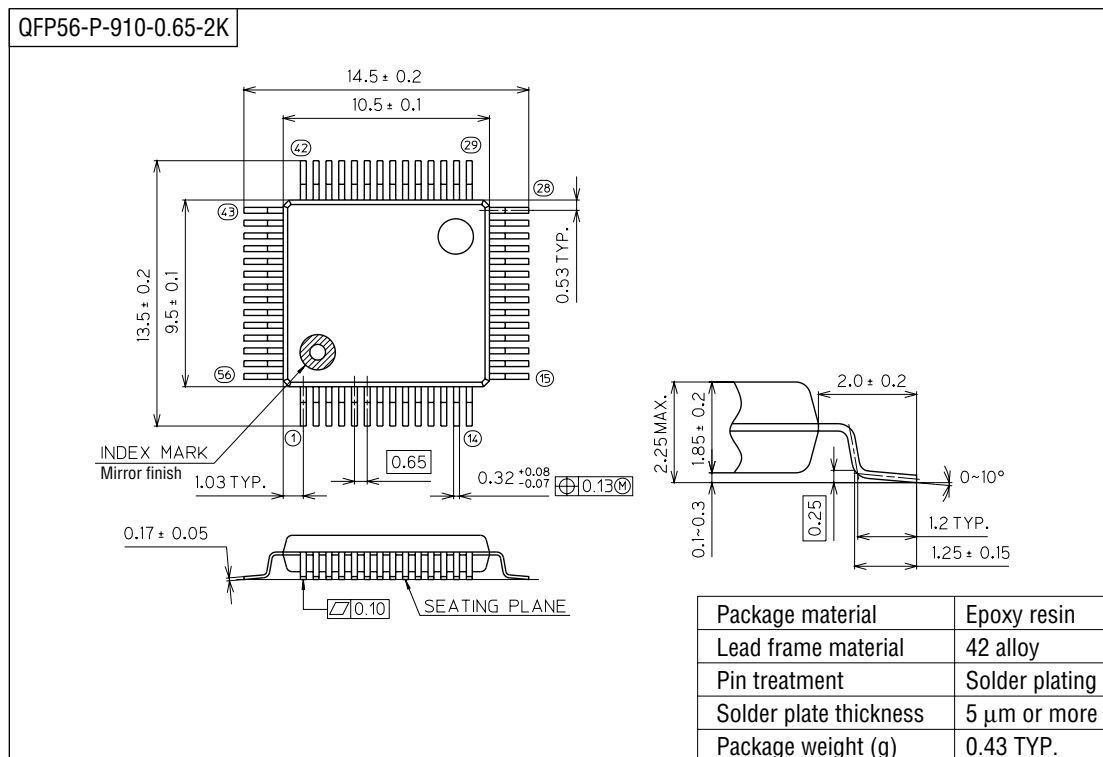
(Unit : mm)



Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)



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