MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

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Rev 2.0, 10/2004

Preliminary Information

High-Frequency, High-Current, Self-Protected High-Side Switch (4.0 mΩ up to 60 kHz)

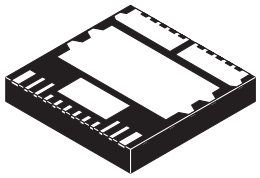
33981

HIGH-SIDE SWITCH
4.0 mΩ

The 33981 is a high-frequency, self-protected 4.0 mΩ $R_{DS(ON)}$ high-side switch used to replace electromechanical relays, fuses, and discrete devices in power management applications.

The 33981 can be controlled by pulse-width modulation (PWM) with a frequency up to 60 kHz. It is designed for harsh environments, and it includes self-recovery features. The 33981 is suitable for loads with high inrush current, as well as motors and all types of resistive and inductive loads.

The 33981 is packaged in a 12 x 12 nonleaded power-enhanced Power QFN package with exposed tabs.



Bottom View

PNA SUFFIX
CASE 1402-02
16-TERMINAL PQFN (12 X 12)

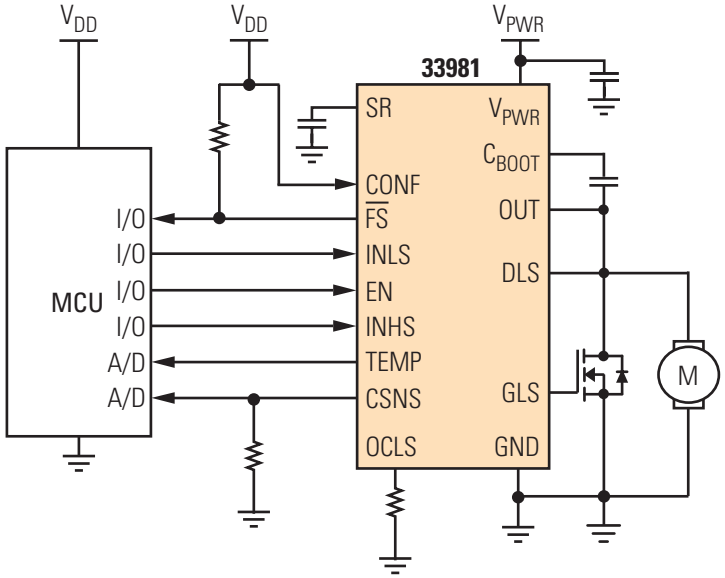
Features

- Single 4.0 mΩ $R_{DS(ON)}$ Maximum High-Side Switch
- PWM Capability up to 60 kHz with Duty Cycle from 5% to 100%
- Very Low Standby Current
- Slew Rate Control with External Capacitor
- Overcurrent and Overtemperature Protection, Undervoltage Shutdown and Fault Reporting
- Reverse Battery Protection
- Gate Drive Signal for External Low-Side N-Channel MOSFET with Protection Features
- Output Current Monitoring
- Temperature Feedback

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
PC33981PNA/R2	-40°C to 125°C	16 PQFN

33981 Simplified Application Diagram



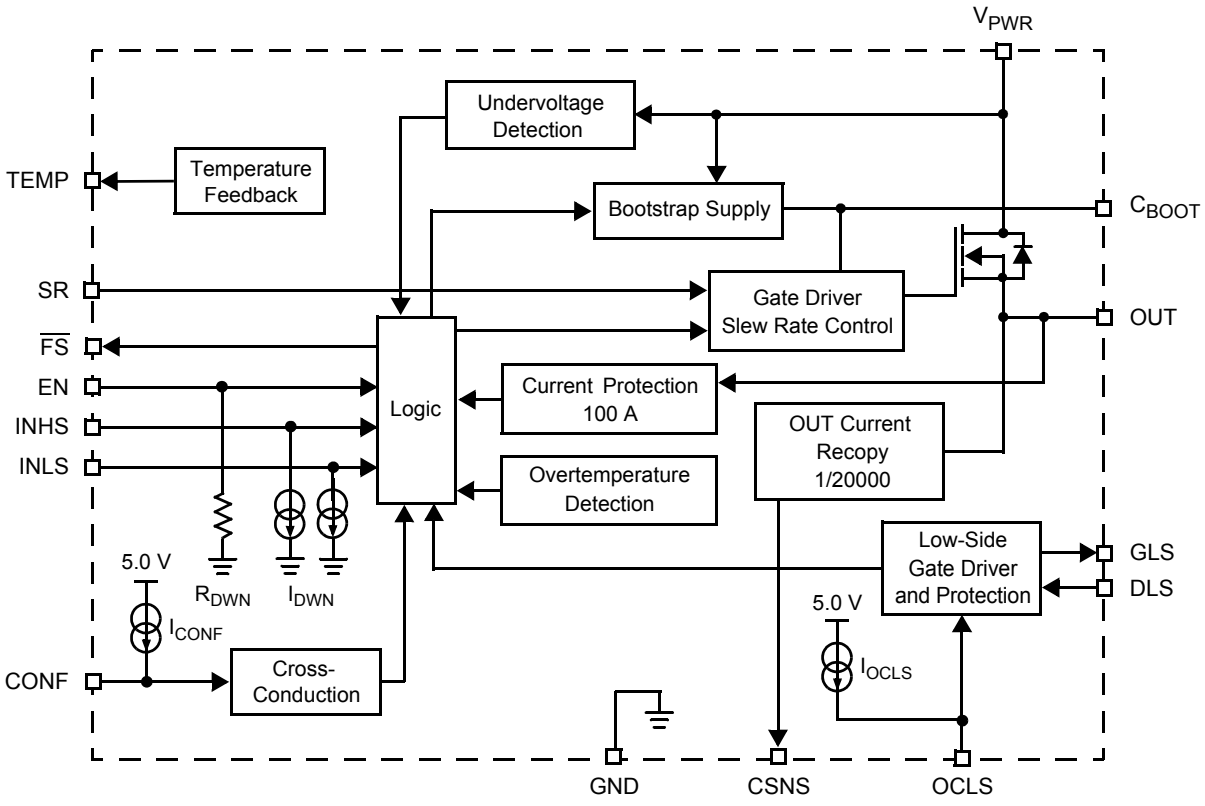
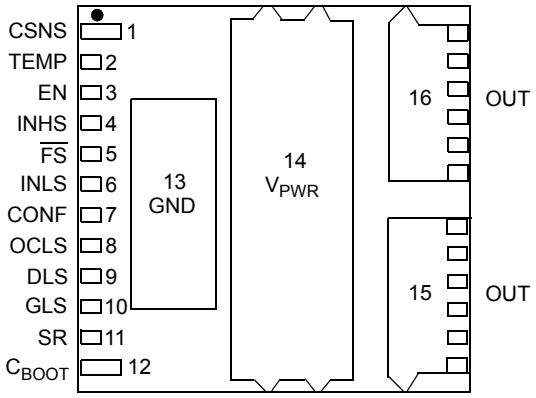


Figure 1. 33981 Simplified Internal Block Diagram

Transparent Top View of Package



TERMINAL DEFINITIONS

Functional descriptions of some of these terminals can be found in the System/Application Information section beginning on page 19.

Terminal	Terminal Name	Formal Name	Definition
1	CSNS	Output Current Monitoring	This terminal is used to output a current proportional to the high-side OUT current and is used externally to generate a ground-referenced voltage for the microcontroller (MCU) to monitor OUT current.
2	TEMP	Temperature Feedback	This terminal reports an analog value proportional to the temperature of the GND flag (terminal 13). It is used by the MCU to monitor board temperature.
3	EN	Enable (Active High)	This is an input used to place the device in a low current sleep mode. This terminal has an passive internal pulldown.
4	INHS	Serial Input High Side	The input terminal is used to directly control the OUT. This input has an active internal pulldown current source and requires CMOS logic levels.
5	$\overline{FS}$	Fault Status (Active Low)	This is an open drain-configured output requiring an external pull-up resistor to V_{DD} (5.0 V) for fault reporting. When a device fault condition is detected, this terminal is active LOW.
6	INLS	Serial Input Low Side	The input terminal is used to directly control an external low-side N-channel MOSFET and has an active internal pulldown current source and requires CMOS logic levels. It can be controlled independently of the INHS depending of CONF terminal.
7	CONF	Configuration Input	This input terminal is used to manage the cross-conduction between the internal high-side N-channel MOSFET and the external low-side N-channel MOSFET. The terminal has an active internal pullup current source. When CONF is at 0 V, the two MOSFETs are controlled independently. When CONF is at 5.0 V, the two MOSFETs cannot be on at the same time.
8	OCLS	Low-Side Overload	This terminal sets the V_{DS} protection level of the external low-side MOSFET. This terminal has an active internal pullup current source. It must be connected to an external resistor.
9	DLS	Drain Low Side	This terminal is the drain of the external low-side N-channel MOSFET. Its monitoring allows for protection features.
10	GLS	Low-Side Gate	This terminal is an output used to drive the gate of the external low-side N-channel MOSFET.
11	SR	Slew Rate Control	A capacitor connected between this terminal and the ground is used to control the output slew rate.

TERMINAL DEFINITIONS (continued)

Functional descriptions of some of these terminals can be found in the System/Application Information section beginning on page 19.

Terminal	Terminal Name	Formal Name	Definition
14	V_{PWR}	Positive Power Supply	This terminal connects to the positive power supply and is the source input of operational power for the device. The V_{PWR} terminal is a backside surface mount tab of the package.
15, 16	OUT	Output	Protected high-side power output to the load. Output terminals must be connected in parallel for operation.

MAXIMUM RATINGS

All voltages are with respect to ground unless otherwise noted.

Rating	Symbol	Value	Unit
ELECTRICAL RATINGS			
Power Supply Voltage Steady-State	V_{PWR}	 -16 to 41	V
Input/Output Terminals Voltage (Note 1)	V_{IN}	-0.3 to 7.0	V
Output Voltage	V_{OUT}	-5.0 to 41	V
Continuous Output Current (Note 2)	I_{OUT}	40	A
CSNS Input Clamp Current	I_{CSNS}	10	mA
SR Voltage	V_{SR}	-0.3 to 54	V
Temperature Feedback Voltage	V_{TEMP}	-0.3 to 5.0	V
C_{BOOT} Voltage	C_{BOOT}	-0.3 to 54	V
OCLS Voltage	V_{OCLS}	-0.3 to 7.0	V
Low-Side Gate Voltage	V_{GLS}	-0.3 to 15	V
Low-Side Drain Voltage	V_{DLS}	-5.0 to 41	V
ESD Voltage Human Body Model (Note 3) Machine Model (Note 4)	 V_{ESD1} V_{ESD2}	 ±2000 ±200	V
Output Clamp Energy (Note 5)	E_{CL}	TBD	J
THERMAL RATINGS			
Operating Temperature Ambient Junction	 T_A T_J	 -40 to 125 -40 to 150	°C
Storage Temperature	T_{STG}	-55 to 150	°C
Thermal Resistance (Note 6) Junction to Power Die Case Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 1.0 20	°C/W
Peak Terminal Reflow Temperature During Solder Mounting (Note 7)	T_{SOLDER}	240	°C
Power Dissipation (TA = 25°C) (Note 8)	P_D	TBD	W

Notes

1. Exceeding voltage limits on INHS, INLS, CONF, CSNS, $\overline{FS}$, TEMP, and EN terminals may cause a malfunction or permanent damage to the device.
2. Continuous high-side output rating as long as maximum junction temperature is not exceeded. Calculation of maximum output current using package thermal resistance is required.
3. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω).
4. ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω) and in accordance with the system module specification with a capacitor > 0.01 μF connected from OUT to GND.
5. Active clamp energy using single-pulse method (L = 16 mH, R_L = 0, V_{PWR} = 12 V, T_J = 150°C).
6. Device mounted on a 2s2p test board per JEDEC JESD51-2.
7. Terminal soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
8. Maximum power dissipation at indicated ambient temperature in free air with no heatsink used.

STATIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions 4.5 V ≤ V_{DD} ≤ 5.5 V, 6.0 V ≤ V_{PWR} ≤ 27 V, -40°C ≤ T_J ≤ 150°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT					
Battery Supply Voltage Range	V_{PWR}				V
Fully Operational		6.0	–	27	
Extended		4.5	–	27	
V_{PWR} Supply Current	$I_{PWR(ON)}$				mA
Output ON, I_{OUT} = 0 A		–	–	10	
V_{PWR} Supply Current	$I_{PWR(SBY)}$				mA
Output OFF, EN = 5.0 V, OUT Connected to GND		–	–	10	
Sleep State Supply Current (V_{PWR} < 14 V, EN = 0 V)	$I_{PWR(SLEEP)}$				μA
T_J = 25°C		–	–	5.0	
T_J = 125°C		–	–	50	
Undervoltage Shutdown	$V_{PWR(UV)}$	2.0	–	4.0	V
Undervoltage Hysteresis	$V_{PWR(UVHYS)}$	–	0.3	–	V
POWER OUTPUT					
Output Drain-to-Source ON Resistance (I_{OUT} = 20 A, T_J = 25°C)	$R_{DS(ON)}$				mΩ
V_{PWR} = 6.0 V		–	–	6.0	
V_{PWR} = 10.0 V		–	–	5.0	
V_{PWR} = 13 V		–	–	4.0	
Output Drain-to-Source ON Resistance (I_{OUT} = 20 A, T_J = 150°C)	$R_{DS(ON)}$				mΩ
V_{PWR} = 6.0 V		–	–	10.2	
V_{PWR} = 9.0 V		–	–	8.5	
V_{PWR} = 13 V		–	–	6.8	
Output Drain-to-Source ON Resistance (I_{OUT} = 20 A, T_J = 25°C)	$R_{DS(ON)}$				mΩ
V_{PWR} = - 13 V		–	–	8.0	
Output Overcurrent Detection Level	I_{OCH}	–	–	100	A
Current Sense Ratio	C_{SR}				–
9.0 V ≤ V_{PWR} ≤ 16 V, CNS ≤ 4.5V		–	1/20000	–	
Current Sense Ratio (C_{SR}) Accuracy	C_{SR_ACC}				%
Output Current					
5.0 A		-20	–	20	
10 A		-14	–	14	
30 A		-12	–	12	
Current Sense Voltage Clamp	$V_{CL(CSNS)}$				V
I_{CCNS} = 15 mA		4.5	6.0	7.0	

STATIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions 4.5 V ≤ V_{DD} ≤ 5.5 V, 6.0 V ≤ V_{PWR} ≤ 27 V, -40°C ≤ T_J ≤ 150°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT (continued)					
Overtemperature Shutdown	T_{SD}	160	175	190	°C
Overtemperature Shutdown Hysteresis (Note 9)	$T_{SD(HYS)}$	5.0	–	20	°C
Low-Side Gate	V_{GSLS}				V
V_{PWR} = 6.0 V		–	6.0	–	
V_{PWR} = 9.0 V		–	9.0	–	
V_{PWR} = 13 V		–	12	–	
V_{PWR} = 27 V		–	12	–	
Low-Side Gate Current C = 4.7 nF	I_{GSLS}	–	100	–	mA
Low-Side Overload Detection Level versus Low-Side Drain Voltage V_{OCLS} - V_{DLS}	V_{DS_LS}	–	–	50	mV
Temperature Feedback T_J = 25°C	T_{Feed}	TBD	4.75	TBD	V
Temperature Feedback Derating	DT_{Feed}	–	-12	–	mV/°C
CONTROL INTERFACE					
Input Logic High Voltage (Note 10)	V_{IH}	0.7	–	–	V_{DD}
Input Logic Low Voltage (Note 10)	V_{IL}	–	–	0.2	V_{DD}
Input Logic Voltage Hysteresis (Note 10)	$V_{IN(HYS)}$	100	350	750	mV
Input Logic Active Pulldown Current (INHS, INLS)	I_{DWN}	5.0	–	20	µA
Input Logic Pulldown Resistor (EN)	R_{DWN}	100	200	400	kΩ
Input Active Pullup Current (OCLS)	I_{OCLSp}	–	100	–	µA
Input Active Pullup Current (CONF)	I_{CONF}	–	10	–	µA
$\overline{FS}$ Tri-State Capacitance (Note 9)	C_{SO}	–	–	20	pF
$\overline{FS}$ Low-State Output Voltage	V_{SOL}	–	0.2	0.4	V

Notes

9. Parameter is guaranteed by process monitoring but is not production tested.
10. Upper and lower logic threshold voltage range applies to EN, CONF, INHS, and INLS input signals.

DYNAMIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions 4.5 V ≤ V_{DD} ≤ 5.5 V, 6.0 V ≤ V_{PWR} ≤ 27 V, -40°C ≤ T_J ≤ 150°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CONTROL INTERFACE AND POWER OUTPUT TIMING					
C_{BOOT} Charge Blanking Time (Note 11)	t_{ON}	–	20	–	µs
Output Rising Slew Rate (Note 12) V_{PWR} = 14 V C_{GATE} = 6.8 nF, from 10% to 90% of V_{OUT}, SR Capacitor = 4.7 nF	SR_R	 – –	 25 –	 – –	V/µs
Output Falling Slew Rate (Note 12) V_{PWR} = 14 V C_{GATE} = 6.8 nF, from 90% to 10% of V_{OUT}, SR Capacitor = 4.7 nF	SR_F	 – –	 25 –	 – –	V/µs
Output Turn-ON Delay Time (Note 13)	$t_{DLY(ON)}$	–	200	–	ns
Output Turn-OFF Delay Time	$t_{DLY(OFF)}$	–	400	–	ns
Input Switching Frequency (Note 14)	f_{PWM}	–	–	60	kHz

Notes

11. Refer to the paragraph entitled Sleep Mode on page 19.
12. Parameter is guaranteed by process monitoring but is not production tested.
13. Turn-ON delay time measured from rising edge of INHS that turns the output ON to V_{OUT} = 0.5 V with R_L= 5.0 Ω resistive load.
14. Turn-OFF delay time measured from falling edge of INHS that turns the output OFF to V_{OUT} = V_{PWR} -0.5 V with R_L= 5.0 Ω resistive load.

Table 1. Functional Truth Table in Normal Mode

Condition	CONF	INHS	INLS	OUT	GLS	$\overline{FS}$	EN	Comments
Sleep	x	x	x	x	x	H	L	Device is in Sleep mode. The OUT and low-side gate are OFF.
Normal	L	H	H	H	H	H	H	Normal mode. High side and low side are controlled independently. The high side and the low side are both on.
Normal	L	L	L	L	L	H	H	Normal mode. High side and low side are controlled independently. The high side and the low side are both off.
Normal	H	L	H	L	H	H	H	Normal mode. No cross-conduction. Half-bridge configuration. The high side is off and the low side is on.
Normal	H	H	L	H	L	H	H	Normal mode. No cross-conduction. Half-bridge configuration. The high side is on and the low side is off.
Normal	H	PWM	H	PWM	PWM OR H (Logical OR)	H	H	Normal mode. Cross-conduction management is activated. Half-bridge configuration.

H = High level
L = Low level
x = Don't care
PWM = Pulse-width modulation

Table 2. Functional Truth Table in Fault Mode

Conditions	CONF	INHS	INLS	OUT	GLS	$\overline{FS}$	EN	TEMP	CSNS	OCLS	Comments
Overtemperature on OUT	x	x	x	L	x	L	H	L	x	x	The 33981 is currently in fault mode. The OUT is OFF. TEMP at 0 V indicates this fault. Once the fault is removed 33981 recovers its normal mode.
Overtemperature on C_{BOOT} or GLS	x	x	x	L	L	L	H	L	x	x	The 33981 is currently in fault mode. The OUT is OFF and GLS is at 0 V. TEMP at 0 V indicates this fault. Once the fault is removed 33981 recovers its normal mode.
Overcurrent on OUT	x	H	x	L	x	L	H	x	L	x	The 33981 is currently in fault mode. The OUT is OFF. It is reset by a logic [0] at INHS for at least 200 μs. When INHS goes to 0 V, CSNS goes to 5.0 V.
Overload on External Low-Side MOSFET	L	x	H	x	L	L	H	x	x	L	The 33981 is currently in fault mode. GLS is at 0 V and OCLS internal current source is off. The external resistance connected between OCLS and GND terminal will pull OCLS terminal to 0 V. The fault is reset by a logic [0] at INLS for at least 200 μs.

H = High level
L = Low level
x = Don't care

Timing Diagram

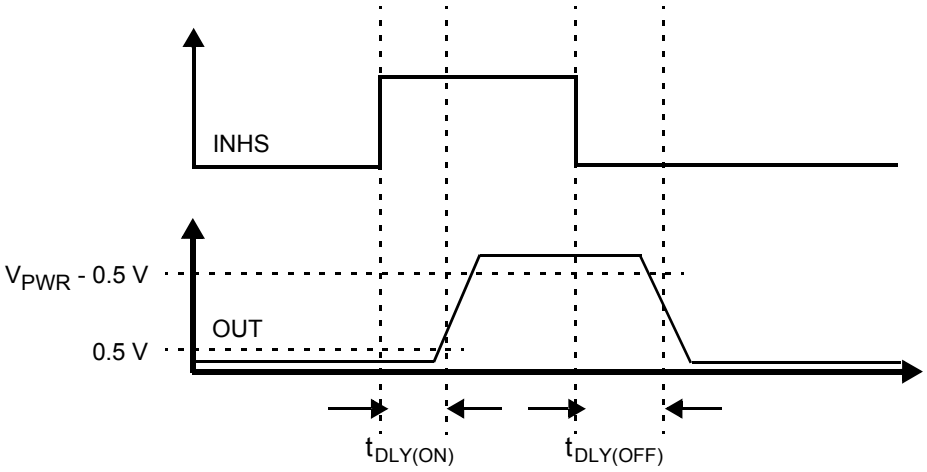


Figure 2. Time Delays

Functional Diagrams

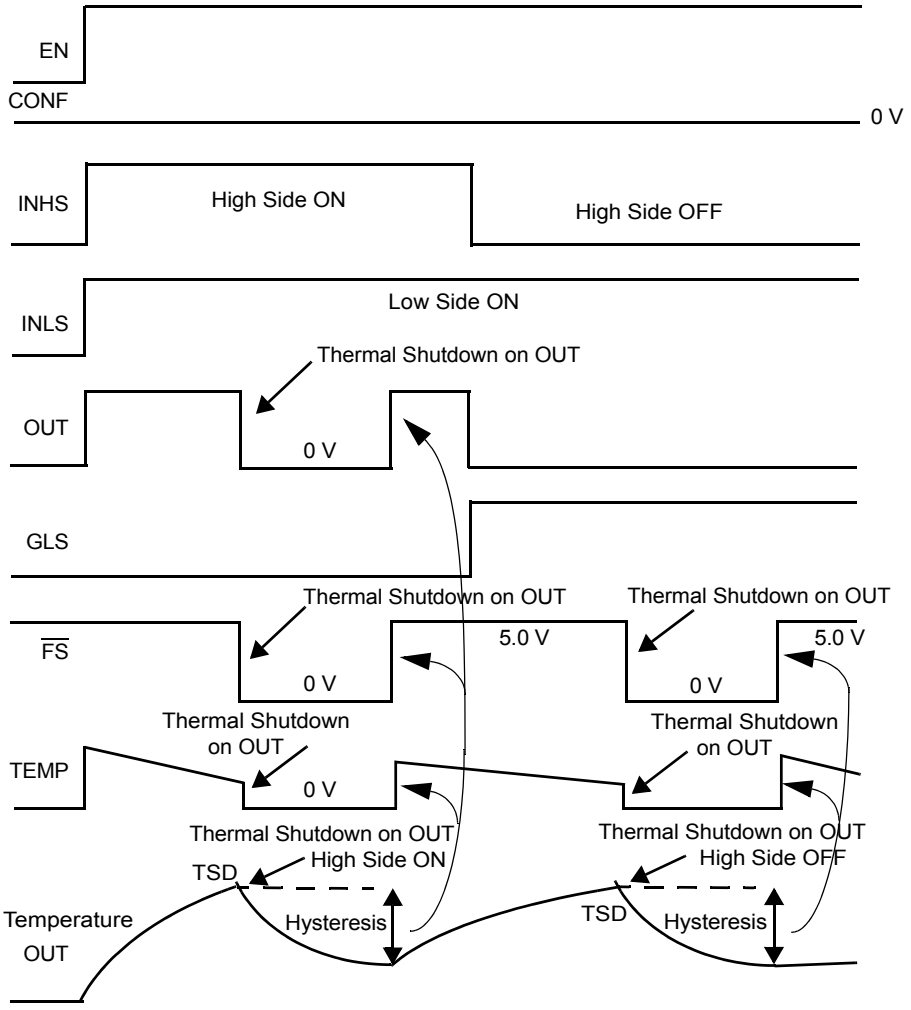


Figure 3. Overtemperature on Output

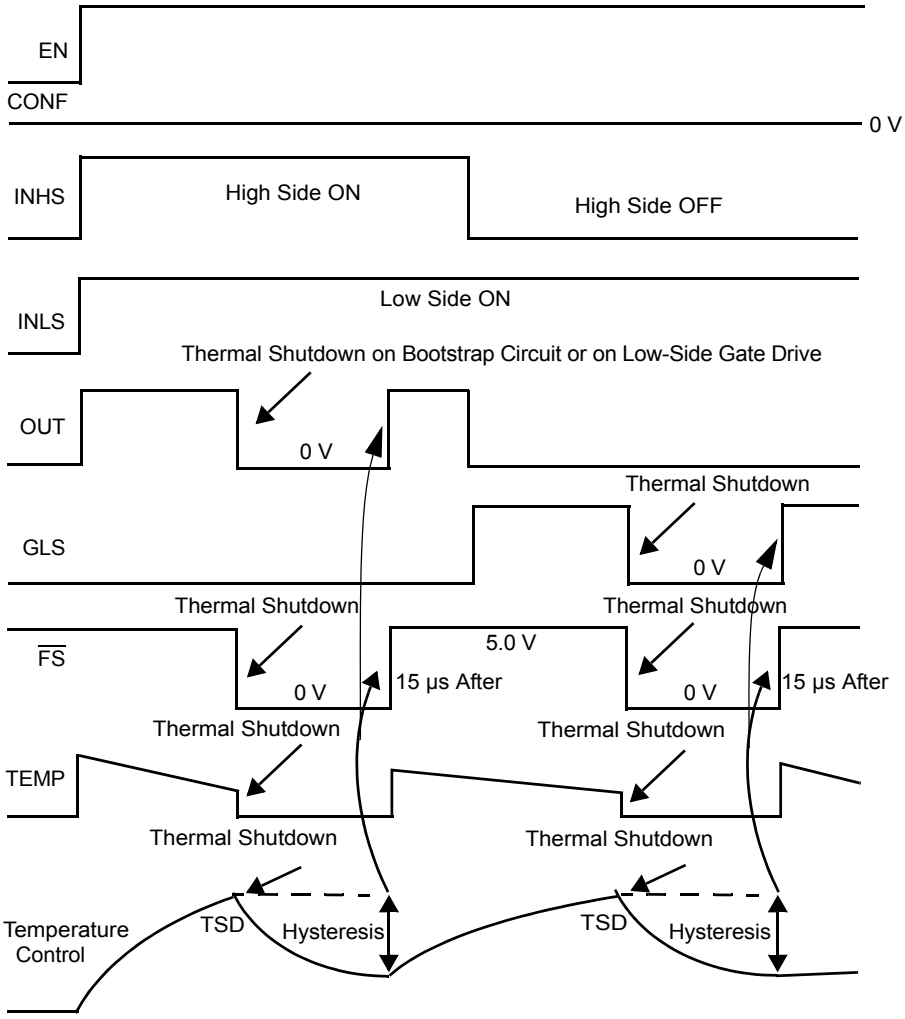


Figure 4. Overtemperature on Bootstrap Circuit or on Low-Side Gate Drive

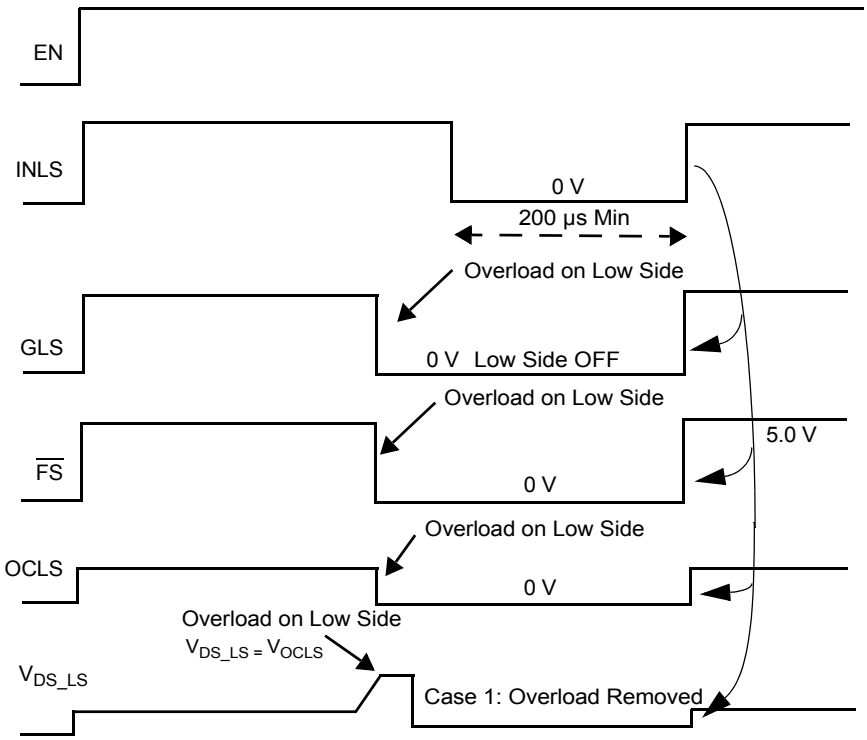


Figure 5. Overload on Low-Side Gate Drive, Case 1

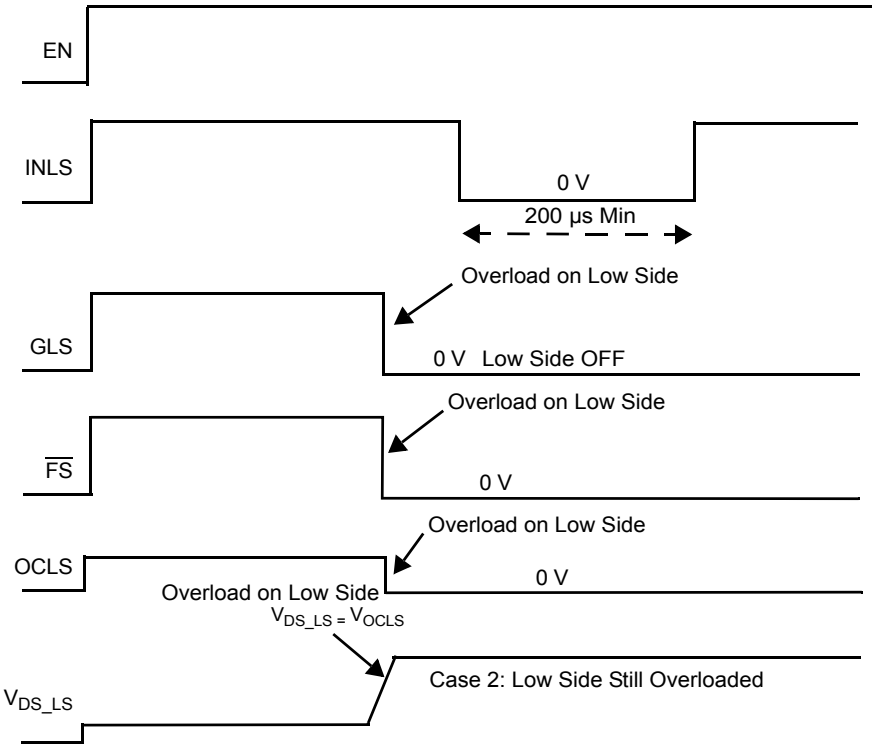


Figure 6. Overload on Low-Side Gate Drive, Case 2

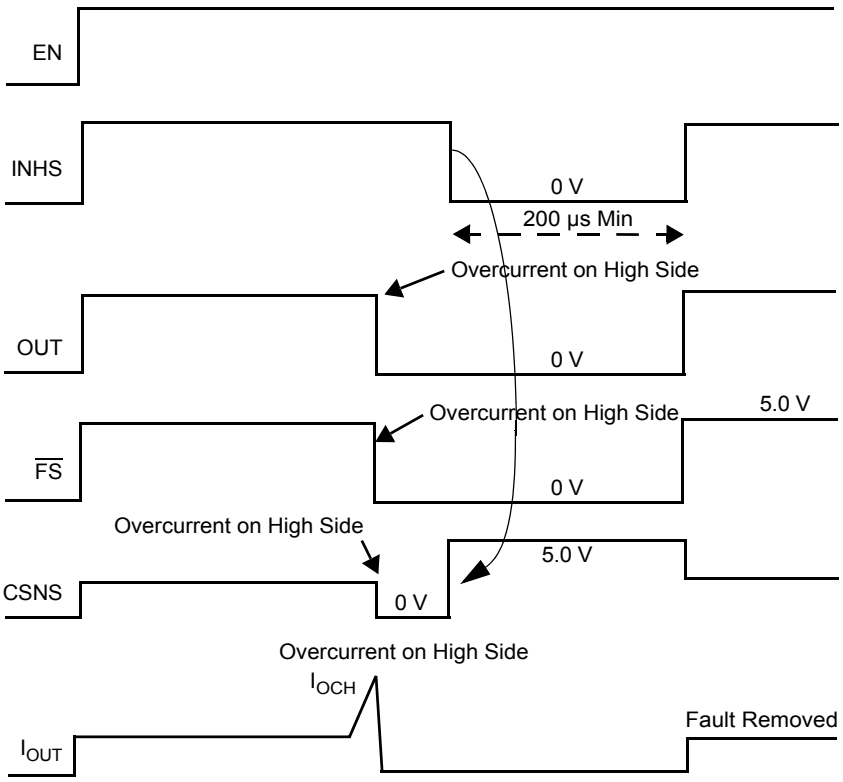


Figure 7. Overcurrent on Output

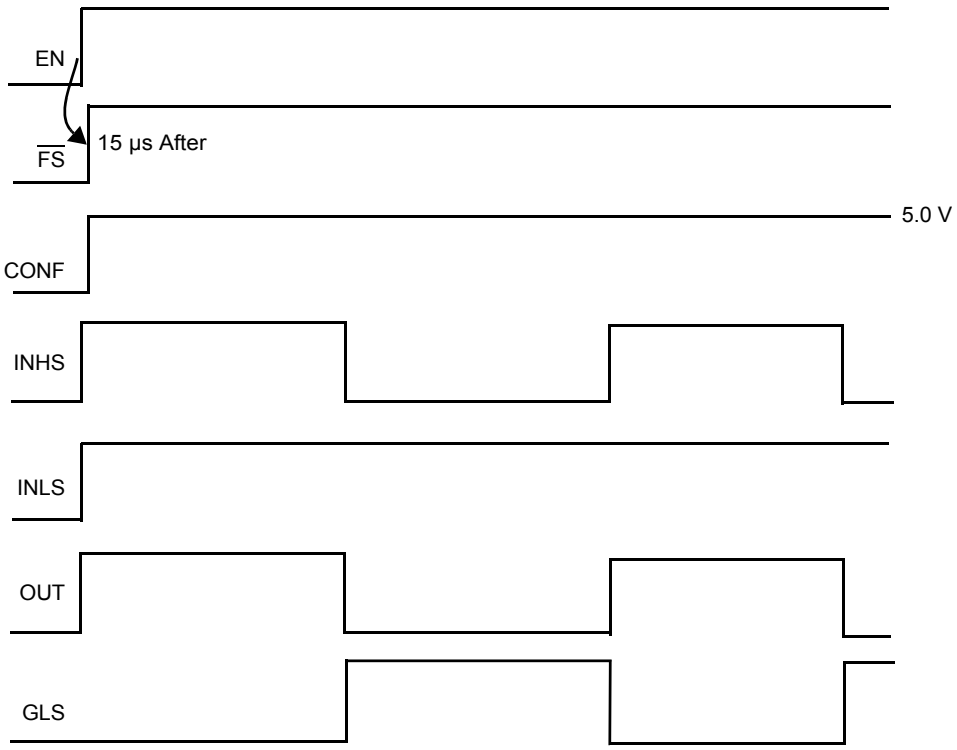


Figure 8. Normal Mode. Cross-Conduction Management

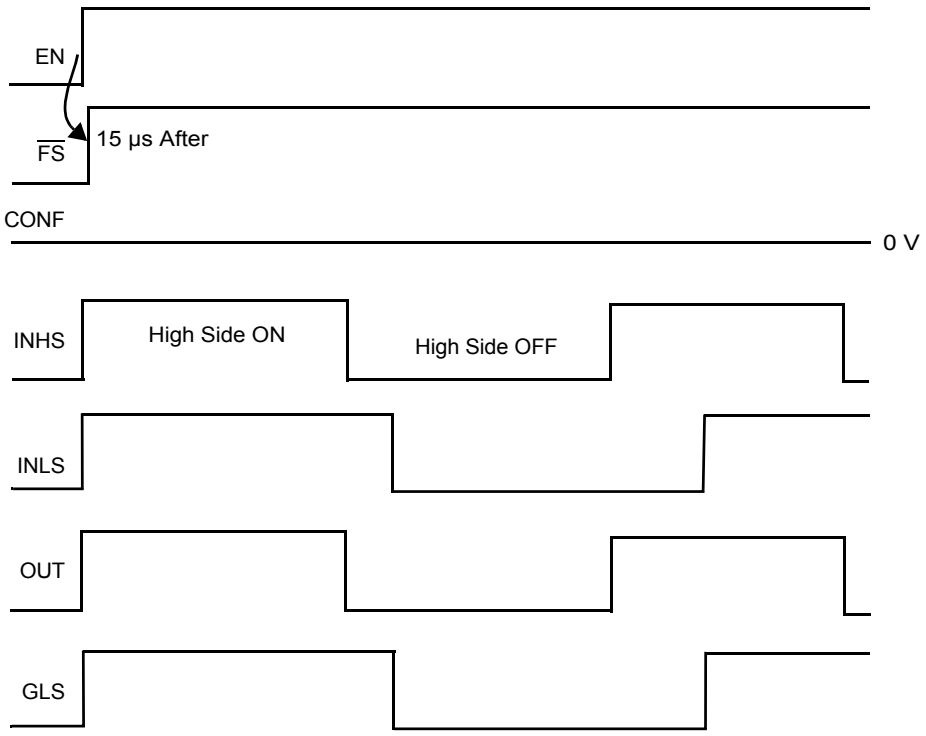


Figure 9. Normal Mode. Independent High Side and Low Side

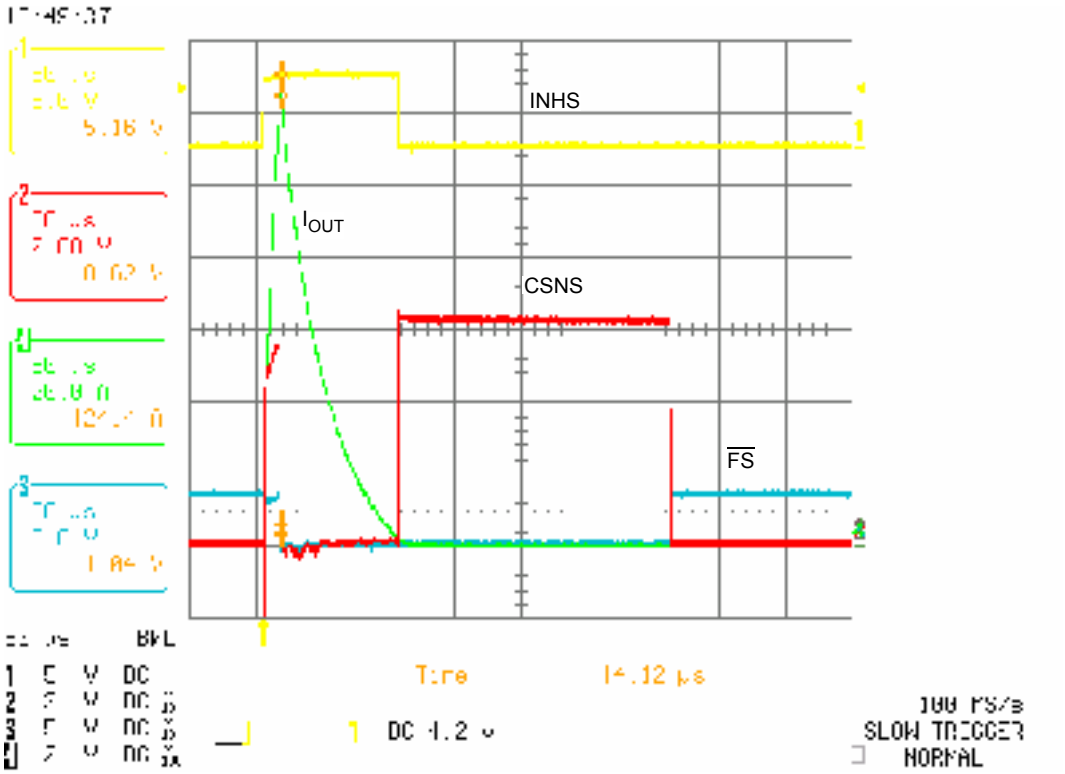


Figure 10. High-Side Overcurrent

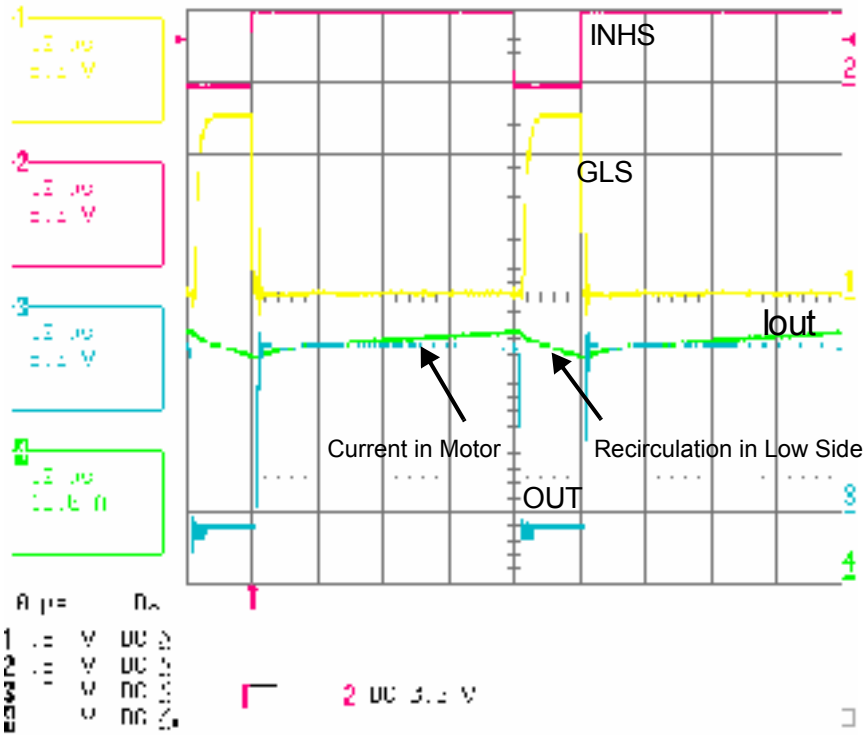


Figure 11. Cross-Conduction with Low Side

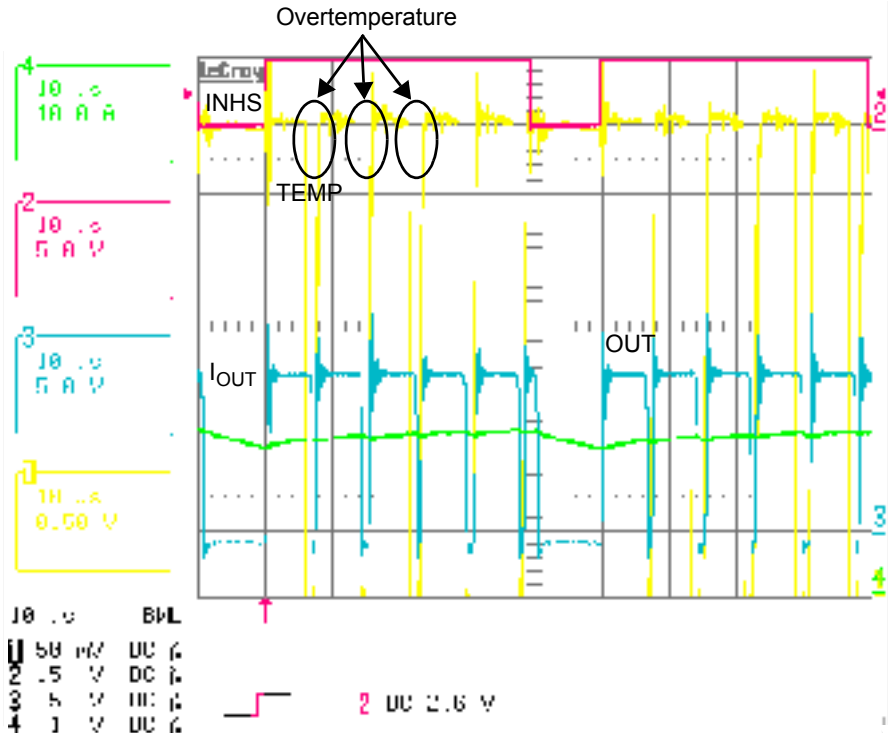


Figure 12. Overtemperature on OUT

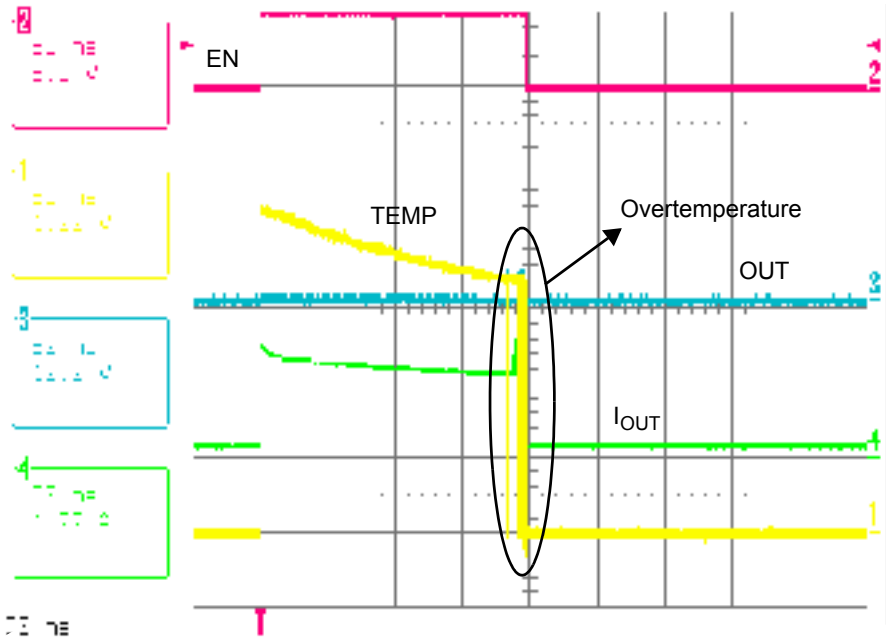


Figure 13. Overtemperature on Bootstrap Circuit or on Low-Side Gate Drive

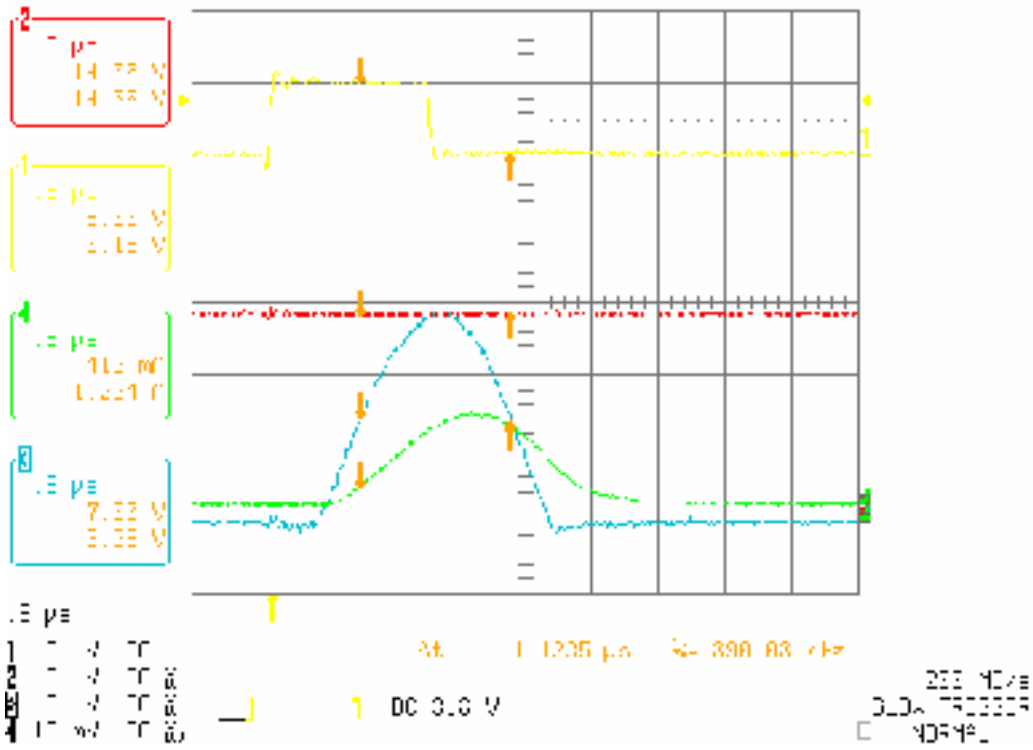


Figure 14. Maximum Operating Frequency for SR Capacitor of 4.7 nF

Electrical Performance Curves

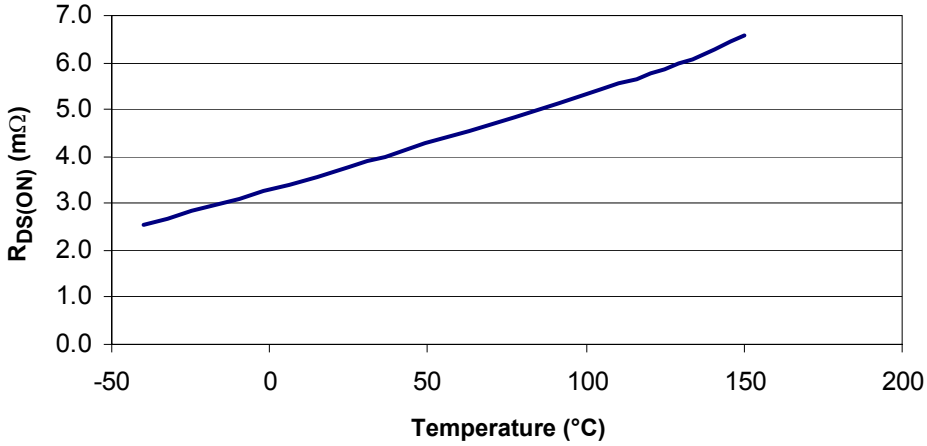


Figure 15. $R_{DS(ON)}$ versus Temperature

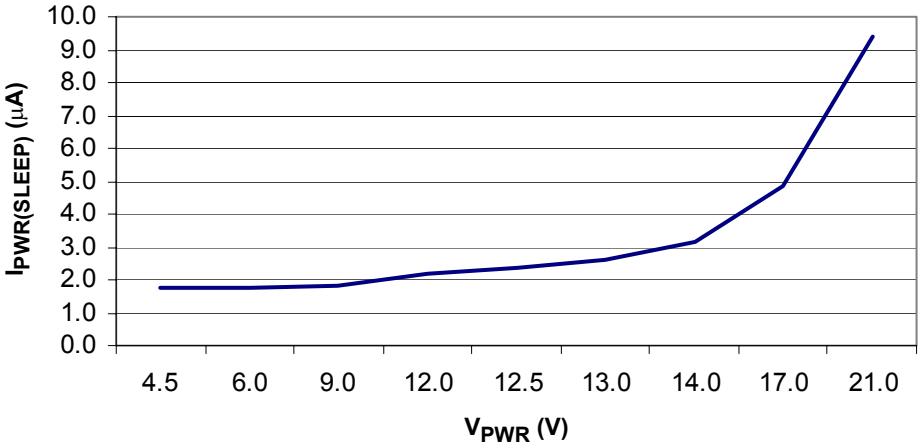


Figure 16. Sleep State Supply Current versus V_{PWR} at 150°C

SYSTEM/APPLICATION INFORMATION

INTRODUCTION

The 33981 is a high-frequency self-protected silicon 4.0 mΩ $R_{DS(ON)}$ high-side switch used to replace electromechanical relays, fuses, and discrete devices in power management applications. The 33981 can be controlled by pulse-width modulation (PWM) with a frequency up to 60 kHz. It is designed for harsh environments, and it includes self-recovery features.

The 33981 is suitable for loads with high inrush current, as well as motors and all types of resistive and inductive loads. A dedicated parallel input is available for an external low-side control with protection features and cross-conduction management.

FUNCTIONAL DESCRIPTION

Sleep Mode

Sleep mode is the state of the 33981 when the EN is logic [0]. In this mode, OUT, the gate driver for the external MOSFET, and all unused internal circuitry are off to minimize current draw.

The 33981 will go to the normal operating mode when the EN terminal is logic [1]. The INHS and INLS commands will be disabled typically 20 μs after the EN transitions to logic [1] to enable the charge of the bootstrap capacitor.

Fault Logic

This 33981 indicates the faults below as they occur by driving the $\overline{FS}$ terminal to logic [0]:

- Overtemperature
- Overcurrent fault on OUT
- Overload fault on the external low-side MOSFET

The $\overline{FS}$ terminal will return to logic [1] when the overtemperature fault condition is removed. The two other faults are latched.

Undervoltage

The latched faults are reset when the V_{PWR} voltage is below $V_{PWR(UV)}$.

Overtemperature Fault

The 33981 incorporates overtemperature detection and shutdown circuitry on OUT. Overtemperature detection also protects the bootstrap circuit (C_{BOOT} terminal) and the low-side gate driver (GLS terminal). Overtemperature detection occurs when OUT is in the ON or OFF state and GLS is at high or low level.

For OUT, an overtemperature fault condition results in OUT turning OFF until the temperature falls below T_{SD}. This cycle will continue indefinitely until the offending load is removed.

Figure 12, page 16, shows an overtemperature on OUT.

An overtemperature fault on the bootstrap circuit or on the low-side gate drive results in OUT turning OFF and the GLS going to 0 V until the temperature falls below T_{SD}. This cycle will continue indefinitely until the offending load is removed. $\overline{FS}$ terminal transition to logic [1] will be disabled typically 15 μs after to enable the charge of the bootstrap capacitor.

Figure 13, page 17, shows an overtemperature on the bootstrap circuit or on the low-side gate drive. As the temperature increases, TEMP voltage decreases until thermal shutdown.

Overtemperature faults force the TEMP terminal to 0 V.

Overcurrent Fault on High Side

The OUT terminal has a 100 A overcurrent high-detection level for maximum device protection. If at any time the current reaches this level, OUT will stay OFF and the CSNS terminal will go to 0 V. The OUT terminal is reset by a logic [0] at the INHS terminal for at least 200 μs. When INHS goes to 0 V, CSNS goes to 5.0 V.

In Figure 11, page 16, the OUT terminal is short-circuited to 0 V. When the current reaches I_{OCH}, OUT is turned OFF within 10 μs owing to internal logic circuit.

Overload Fault on Low Side

This fault detection is active when INLS is logic [1]. Low-side overload protection does not measure the current directly but rather its effects on the low-side MOSFET. When $V_{GLS} > V_{GSH}$ and $V_{DLS} > V_{DSH}$ for at least 2.5 μs, the GLS terminal goes to 0 V and the OCLS internal current source is disconnected and OCLS goes to 0 V. The GLS terminal and the OCLS terminal are reset by a logic [0] at the INLS terminal for at least 200 μs.

When connected to an external resistor, the OCLS terminal with its internal current source sets the V_{DSH} level. By changing the external resistance, the protection level can be adjusted depending on low-side characteristics. A 3.3 kΩ resistor gives a V_{DSH} level of 3.3 V typical.

This protection circuitry measures the voltage between the drain of the low side (DLS terminal) and the 33981 ground (GND terminal). It also uses the voltage across the external resistance connected to the OCLS terminal and the GND terminal. For this reason it is key that the low-side source, the 33981 ground, and the external resistance ground connection are connected together in order to prevent false error detection due to ground shifts.

Configuration

The CONF terminal manages the cross-conduction between the internal MOSFET and the external low-side MOSFET. With the CONF terminal at 0 V, the two MOSFETs can be independently controlled. A load can be placed between the high side and the low side.

With the CONF terminal at 5.0 V, the two MOSFETs cannot be on at the same time. They are in half-bridge configuration as shown in the simplified application diagram on page 1. If INHS and INLS are at 5.0 V at the same time, INHS has priority and OUT will be at V_{PWR}. If INHS changes from 5.0 V to 0 V with INLS at 5.0 V, GLS will go to high state as soon as the V_{GS} of the internal MOSFET is lower than TBD typically. A half-bridge application could consist in sending PWM signal to the INHS terminal and 5.0 V to the INLS terminal with the CONF terminal at 5.0 V.

Figure 11, page 16, illustrates the simplified application diagram on page 1 with a DC motor and external low side. The CONF and INLS terminals are at 5.0 V. When INHS is at 5.0 V, current is flowing in the motor. When INHS goes to 0 V, the load current recirculates in the external low side.

Bootstrap Supply

Bootstrap supply provides current to recharge the bootstrap capacitor through the V_{PWR} terminal. A short time is required after the application of power to the device to charge the bootstrap capacitor. A typical value for this capacitor is 100 nF. An internal charge pump allows continuous MOSFET drive. When the device is in the sleep mode, this bootstrap supply is off to minimize current consumption.

High-Side Gate Driver

The high-side gate driver switches the bootstrap capacitor voltage to the gate of the MOSFET. The driver circuit has a low-impedance drive to ensure that the MOSFET remains OFF in the presence of fast falling dV/dt transients on the OUT terminal.

This bootstrap capacitor connected between the power supply and the C_{BOOT} terminal provides the high pulse current to drive the device. The voltage across this capacitor is limited to about 13 V. C_{BOOT} is protected against short by a local overtemperature sensor.

An external capacitor connected between terminals SR and GND is used to control the slew rate at the OUT terminal.

Low-Side Gate Driver

The low-side control circuitry is PWM capable. It can drive a standard MOSFET with an $R_{DS(ON)}$ as low as 4.0 mΩ at a frequency up to 60 kHz. The V_{GS} is internally clamped at 14 V typically to protect the gate of the MOSFET. The GLS terminal is protected against short by a local overtemperature sensor.

Thermal Feedback

The 33981 has an analog feedback output (TEMP terminal) that provides a value proportional to the temperature of the GND flag (terminal 13). The controlling microcontroller can “read” the temperature proportional voltage with its analog-to-digital converter (ADC). This can be used to provide real-time monitoring of the PC board temperature to optimize the motor speed and to protect the whole electronic system. TEMP terminal value is typically 4.2 V at 25°C with a negative temperature coefficient of 10 mV/K.

Reverse Battery

The 33981 survives the application of reverse battery voltage as low as -16 V. Under these conditions, the output’s gate is enhanced to decrease device power dissipation. No additional passive components are required. The 33981 survives these conditions until the maximum junction rating is reached.

In the case of reverse battery in a half-bridge application, a direct current passes through the external freewheeling diode and the internal high-side.

As Figure 17 shows, it is essential to protect this power line. The proposed solution is an external low-side with its gate tied to battery voltage through a resistor. A high-side in the V_{PWR} line could be another solution but with a more complex drive.

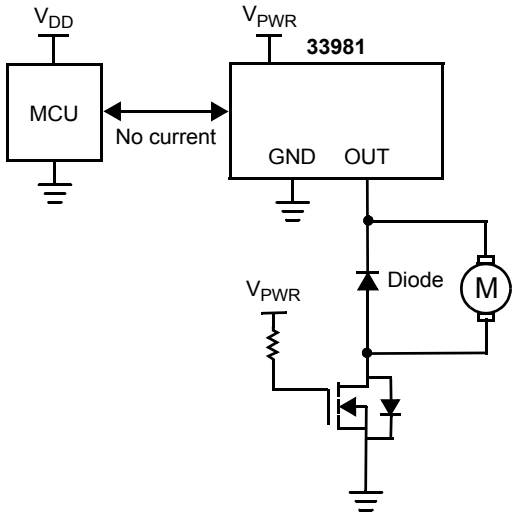


Figure 17. Reverse Battery Protection

APPLICATIONS

Figure 18 shows a typical application for the 33981. A brush DC motor is connected to the output. A low-side gate driver is used for the freewheeling phase. Typical values for the external capacitors and resistances are given.

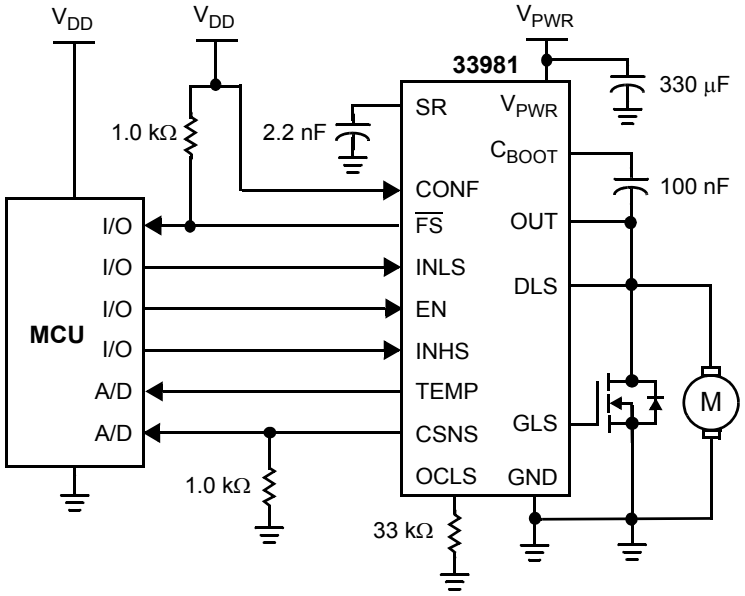
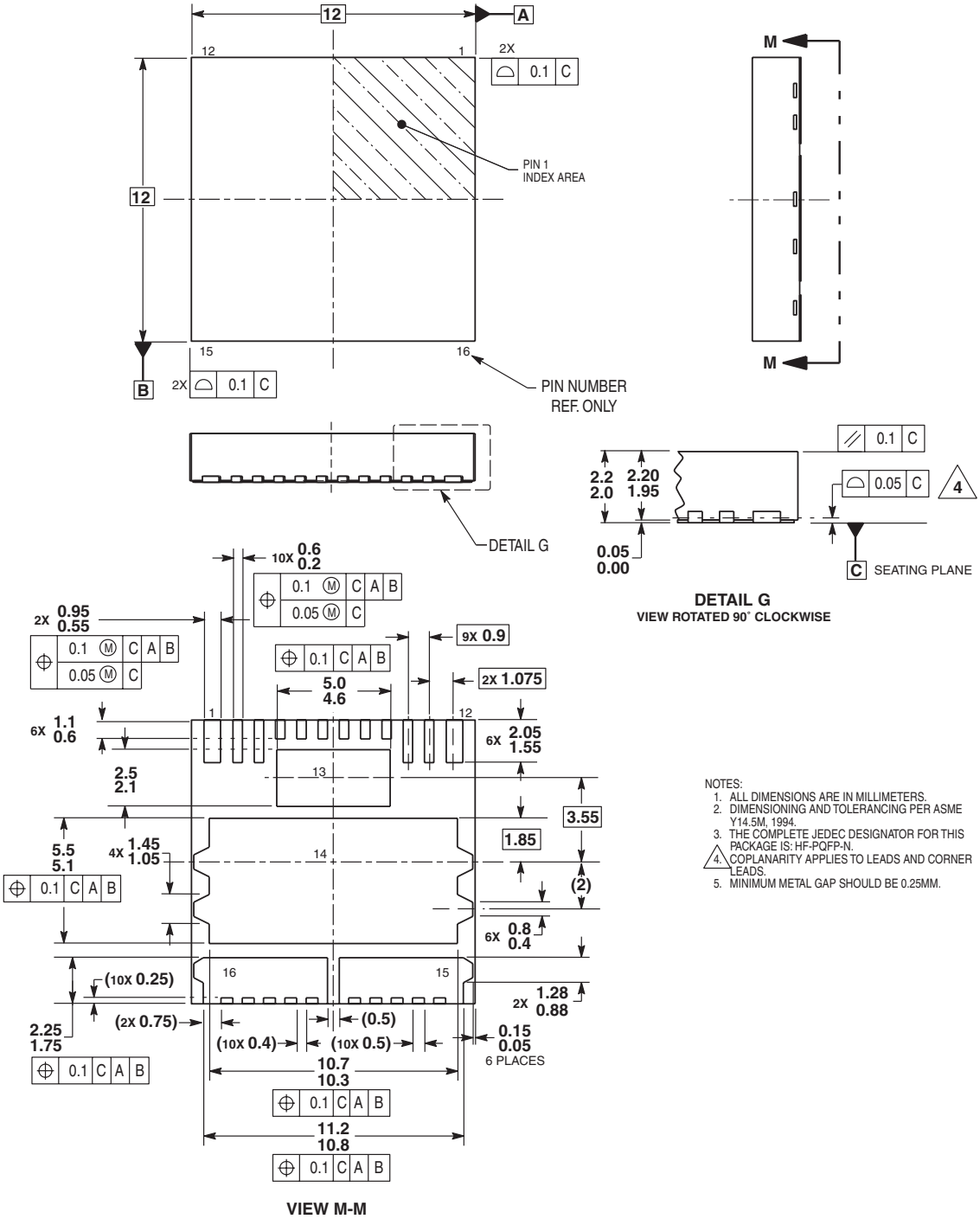


Figure 18. 33981 Typical Application Diagram

PACKAGE DIMENSIONS

PNA SUFFIX
16-TERMINAL PQFN
NONLEADED PACKAGE
CASE 1402-02
ISSUE B



VIEW M-M

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF-PQFP-N.
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5. MINIMUM METAL GAP SHOULD BE 0.25MM.

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