

MSM5188

16,384-WORD × 4-BIT HIGH SPEED STATIC CMOS RAM

GENERAL DESCRIPTION

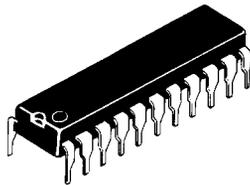
The MSM5188RS is a static CMOS RAM organized as 16384 words by 4 bits. It features 5V single power supply operation and direct TTL input/output compatibility. Since the circuitry is completely static, external clock and refreshing operations are unnecessary which makes this device very easy to use.

The MSM5188RS is offered in a 22-pin slim package.

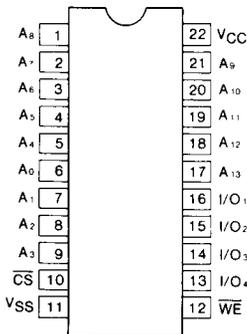
FEATURES

- Single 5V supply ($\pm 10\%$)
- Completely static operation
- Operating temperature range $T_a = 0$ to 70°C
- Low power dissipation
 - Standby 11 mW MAX
 - Operation 605 mW MAX
- Access time
 - 45/55/70 ns MAX
- Direct TTL compatible (Input and output)
- 3-State output
- 22 pin DIP PKG (300 mil width)

5

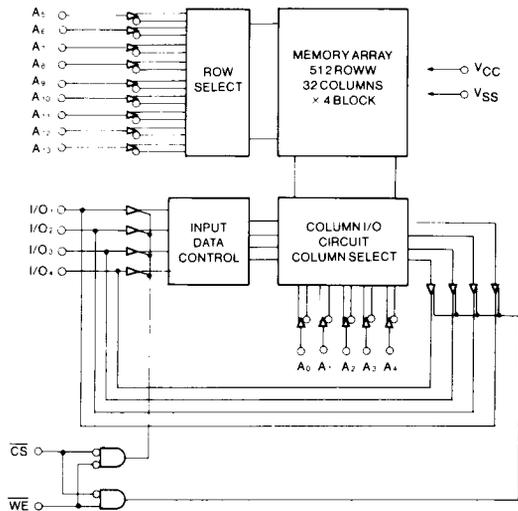


PIN CONFIGURATION



Pin Names	Function
A ₀ to A ₁₃	Address input
I/O ₁ to I/O ₄	Data input/output
CS	Chip Select
WE	Write Enable
V _{CC} , V _{SS}	Supply Voltage

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Condition	Value	Unit
Supply Voltage	V_{CC}	$T_a = 25^\circ\text{C}$ Respect to V_{SS}	-0.3 to 7.0	V
Input Voltage	V_{IN}		-0.3 to 7.0	V
Power Dissipation	PD	$T_a = 25^\circ\text{C}$	1.0	W
Operating Temperature	T_{opr}	-	0 to +70	$^\circ\text{C}$
Storage Temperature	T_{stg}	-	-55 to +150	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	-	4.5	5.0	5.5	V
"H" Input Voltage	V_{IH}	$V_{CC} = 5V \pm 10\%$	2.2	-	$V_{CC} + 0.3$	V
"L" Input Voltage	V_{IL}		-0.3	-	0.8	V
Output Load	CL	-	-	-	30	pF
	N	TTL Load	-	-	1	

5

* When pulse width is equal to or smaller than 20 ns, V_{IH} max = $V_{CC} + 1.0V$, V_{IL} min = $-1.0V$.

DC CHARACTERISTICS

($V_{CC} = 5V \pm 10\%$, $T_a = 0^\circ\text{C}$ to 70°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Leakage Current	I_{LI}	$V_I = 0$ to V_{CC}	-1		1	μA
Output Leakage Current	I_{LO}	$\overline{CS} = V_{IH}$ $V_{I/O} = 0$ to V_{CC}	-1		1	μA
"H" Output Voltage	V_{OH}	$I_{OH} = -4$ mA	2.4			V
"L" Output Voltage	V_{OL}	$I_{OL} = 8$ mA			0.4	V
Standby Supply Current	I_{CCS}	$\overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} \leq 0.2V$ OR $V_{IN} \geq V_{CC} - 0.2V$			2	mA
	I_{CCS1}	$\overline{CS} = V_{IH}$ $T_{CYC} = \text{min cycle}$			30	mA
Operating Supply Current	I_{CCA}	Min cycle, $I_{OUT} = 0$ mA			110	mA

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Condition	Min.	Max.	Unit
Input Capacitance	C _I	V _I = 0V		6	pF
I/O Capacitance	C _{I/O}	V _{I/O} = 0V		8	pF

AC CHARACTERISTICS TEST CONDITIONS

Parameter	Conditions
Input Pulse Level	V _{IH} = 3.0V, V _{IL} = 0V
Input Rise and Fall Times	5 ns
Input/Output Timing Reference Level	1.5V
Output Load	CL = 30 pF, 1 TTL GATE

5

READ CYCLE

(V_{CC} = 5V ± 10%, Ta = 0°C to 70°C)

Parameter	Symbol	5188-45		5188-55		5188-70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	T _{RC}	45		55		70		ns
Address Access Time	T _{AC}		45		55		70	ns
Chip Select Access Time	T _{CO}		45		55		70	ns
Chip Selection to Output Active	T _{CX}	5		5		5		ns
Output Hold Time from Address Change	T _{OHA}	5		5		5		ns
Output 3-state from Deselection	T _{OTD}	0	25	0	25	0	30	ns
Chip Selection to Power up Time	T _{PU}	0		0		0		ns
Chip Deselection to Power Down Time	T _{PD}	0	45	0	55	0	70	ns

- Notes:**
1. Read Condition: During the overlap of a low \overline{CS} and a high \overline{WE} .
 2. T_{CX} and T_{OTD} are measured ±200 mV from steady state voltage with specified loading in Figure 2.

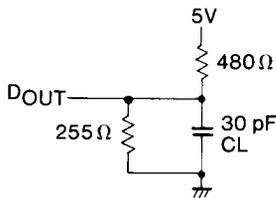


Figure 1 Output Load

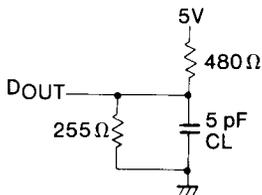


Figure 2 Output Load

Note: CL includes scope and jig.

WRITE CYCLE

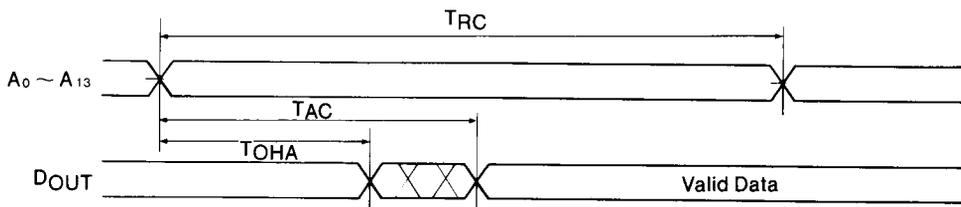
($V_{CC} = 5V \pm 10\%$, $T_a = 0^\circ C$ to $70^\circ C$)

Parameter	Symbol	5188-45		5188-55		5188-70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	T _{WC}	45		55		70		ns
Chip Selection to End of Write	T _{CW}	40		45		55		ns
Address Valid to End of Write	T _{AW}	40		45		55		ns
Address to Write Setup Time	T _{AS}	0		0		0		ns
Write Time	T _W	40		45		55		ns
Write Recovery Time	T _{WR}	5		5		5		ns
Data Setup Time	T _{DS}	25		25		30		ns
Data Hold from Write Time	T _{DH}	0		0		0		ns
Output 3-state from Write	T _{TOW}	0	20	0	25	0	30	ns
Output Active from End of Write	T _{OW}	0		0		0		ns

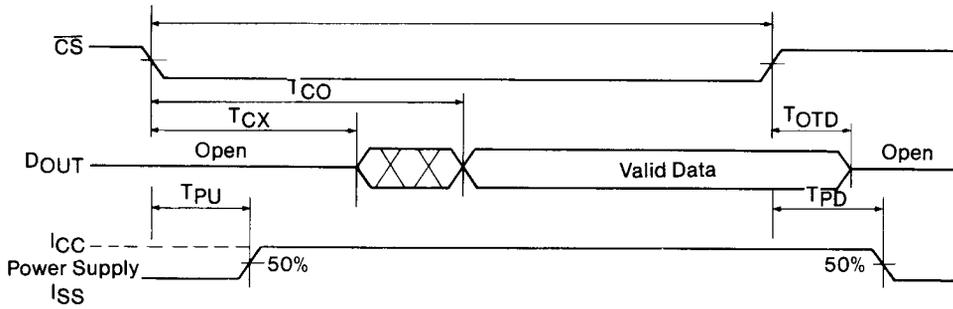
5

- Notes:**
1. Write condition: During the overlap of a low \overline{CS} and a low \overline{WE} .
 2. T_{AS} is specified from a low \overline{CS} or a low \overline{WE} , whichever occurs last after the address is set.
 3. T_W is an overlap time of a low \overline{CS} and a low \overline{WE} .
 4. T_{WR}, T_{DS} and T_{DH} are specified from a high \overline{CS} or a high \overline{WE} , whichever occurs first.
 5. T_{TOW} and T_{OW} are measured ± 200 mV from steady state voltage with specified loading in Figure 2.
 6. When I/O pins are Data output mode, don't force inverse input signals to those pins.

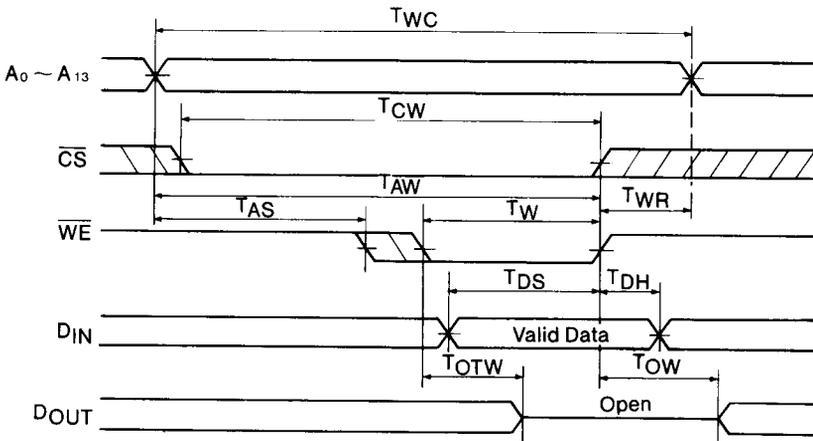
READ CYCLE TIMING 1



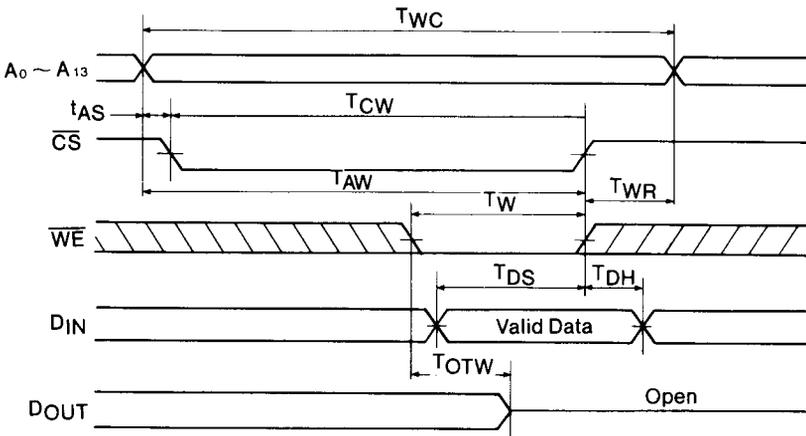
READ CYCLE TIMING 2



WRITE CYCLE TIMING 1
(\overline{WE} Control)



WRITE CYCLE TIMING 2
(\overline{CS} Control)



5