



STS3C2F100

N-CHANNEL 100V - 0.110 Ω - 3A SO-8
 P-CHANNEL 100V - 0.320 Ω - 1.5A SO-8

COMPLEMENTARY PAIR STripFET™ POWER MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STS3C2F100(N-Channel)	100 V	< 0.145Ω	3.0 A
STS3C2F100(P-Channel)	100 V	< 0.380Ω	1.5 A

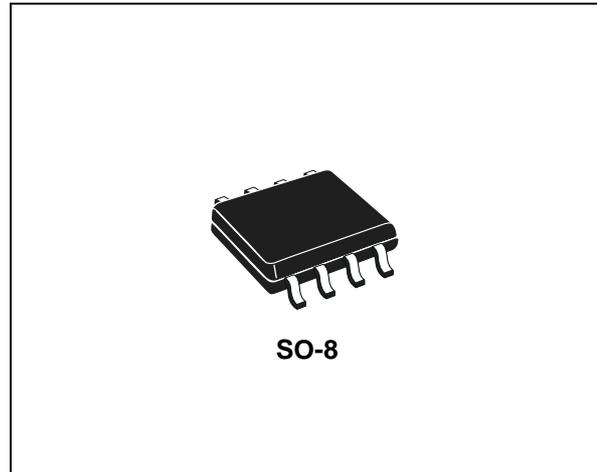
- TYPICAL R_{DS(on)} (N-Channel) = 0.110 Ω
- TYPICAL R_{DS(on)} (P-Channel) = 0.320 Ω
- STANDARD OUTLINE FOR EASY AUTOMATED SURFACE MOUNT ASSEMBLY
- ULTRA LOW GATE CHARGE
- ULTRA LOW ON-RESISTANCE

DESCRIPTION

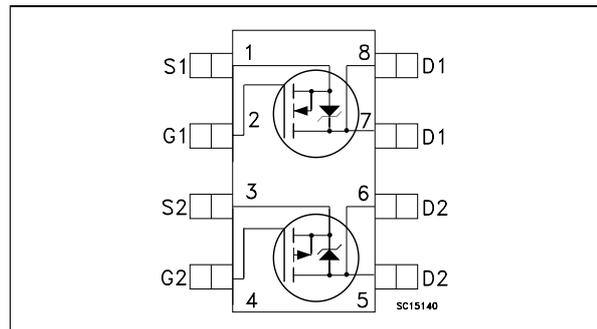
This MOSFET is the second generation of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

APPLICATIONS

- DC MOTOR DRIVES
- AUDIO AMPLIFIER



INTERNAL SCHEMATIC DIAGRAM



Ordering Information

SALES TYPE	MARKING	PACKAGE	PACKAGING
STS3C2F100	S3C2F100	SO-8	TAPE & REEL

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	N-CHANNEL	P-CHANNEL	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	100		V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	100		V
V _{GS}	Gate- source Voltage	± 20		V
I _D	Drain Current (continuous) at T _C = 25°C	3.0	1.5	A
I _D	Drain Current (continuous) at T _C = 100°C	1.9	1.0	A
I _{DM} (●)	Drain Current (pulsed)	12	6	A
P _{tot}	Total Dissipation at T _C = 25°C	2		W
T _{stg}	Storage Temperature	-55 to 150		°C
T _j	Max. Operating Junction Temperature	150		°C

(●) Pulse width limited by safe operating area.

Note: P-CHANNEL MOSFET actual polarity of voltages and current has to be reversed

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TAB.1 THERMAL DATA

Rthj-amb(1)	Thermal Resistance Junction-ambient	62.5	°C/W
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(1) when mounted on 1 in² pad of 2 oz. copper, t ≤ 10sec.

ELECTRICAL CHARACTERISTICS (T_j = 25 °C unless otherwise specified)

TAB.2 OFF

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0	n-ch p-ch	100			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating T _C = 125°C	n-ch p-ch			1 10	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 20 V	n-ch p-ch			±100	nA

TAB.3 ON

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} I _D = 250 μA	n-ch p-ch	2 2			V V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V I _D = 1.5 A V _{GS} = 10 V I _D = 1.0 A	n-ch p-ch		0.110 0.320	0.145 0.380	Ω Ω

TAB.4 DYNAMIC

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
g _{fs} (*)	Forward Transconductance	V _{DS} = 20 V I _D = 1.5 A V _{DS} = 30 V I _D = 1.0 A	n-ch p-ch		3 4		S S
C _{iss}	Input Capacitance		n-ch p-ch		460 705		pF pF
C _{oss}	Output Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0	n-ch p-ch		70 83		pF pF
C _{rss}	Reverse Transfer Capacitance		n-ch p-ch		30 30		pF pF

ELECTRICAL CHARACTERISTICS (continued)

TAB.5 SWITCHING ON

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on Delay Time	N-CHANNEL V _{DD} = 50 V I _D = 1.5 A R _G = 4.7 Ω V _{GS} = 10 V	n-ch		16		ns
			p-ch		14		ns
t _r	Rise Time	P-CHANNEL V _{DD} = 50 V I _D = 1.5 A R _G = 4.7 Ω V _{GS} = 10 V (Resistive Load, Figure 1)	n-ch		25		ns
			p-ch		20		ns
Q _g	Total Gate Charge	N-CHANNEL V _{DD} =80V I _D =3A V _{GS} =10V	n-ch p-ch		15 20	20 27	nC nC
Q _{gs}	Gate-Source Charge	P-CHANNEL V _{DD} = 80V I _D = 1.5A V _{GS} = 10V (see test circuit, Figure 2)	n-ch		3.7		nC
Q _{gd}	Gate-Drain Charge		p-ch		2.0		nC
			n-ch		4.7		nC
		p-ch		6.0		nC	

TAB.6 SWITCHING OFF

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
t _{d(off)}	Turn-off Delay Time	N-CHANNEL V _{DD} = 50 V I _D = 1.5 A R _G = 4.7 Ω V _{GS} = 10 V	n-ch		32		ns
			p-ch		33		ns
t _f	Fall Time	P-CHANNEL V _{DD} = 50 V I _D = 1.5 A R _G = 4.7 Ω V _{GS} = 10 V (Resistive Load, Figure 1)	n-ch		20		ns
			p-ch		7.5		ns

TAB.7 SOURCE DRAIN DIODE

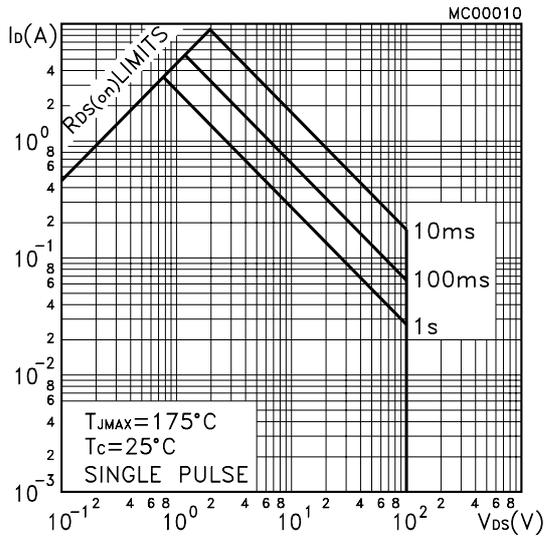
Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
I _{SD}	Source-drain Current		n-ch			3.0	A
I _{SDM} (*)	Source-drain Current (pulsed)		p-ch			1.5	A
			n-ch			12	A
			p-ch			6.0	A
V _{SD} (*)	Forward On Voltage	I _{SD} = 3 A V _{GS} = 0 I _{SD} = 1.5 A V _{GS} = 0	n-ch			1.2	V
			p-ch			1.2	V
t _{rr}	Reverse Recovery Time	N-CHANNEL I _{SD} = 3 A di/dt = 100A/μs V _{DD} = 50 V T _j = 150 °C	n-ch		90		ns
			p-ch		65		ns
Q _{rr}	Reverse Recovery Charge	P-CHANNEL I _{SD} = 1.5 A di/dt = 100A/μs V _{DD} = 50 V T _j = 150 °C (see test circuit, Figure 3)	n-ch		230		nC
I _{RRM}	Reverse Recovery Current		p-ch		175		nC
			n-ch		5.0		A
		p-ch		5.4		A	

(*) Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %.

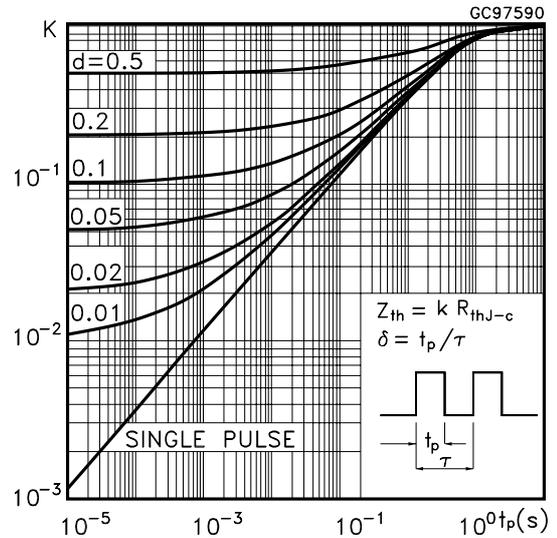
(●) Pulse width limited by safe operating area.

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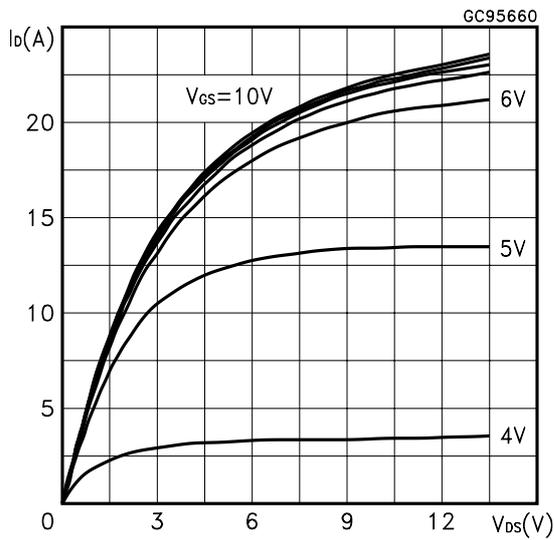
Safe Operating Area **n-ch**



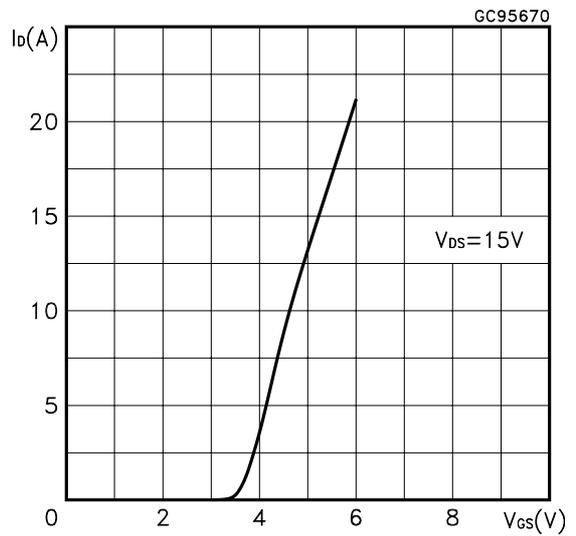
Thermal Impedance **n-ch**



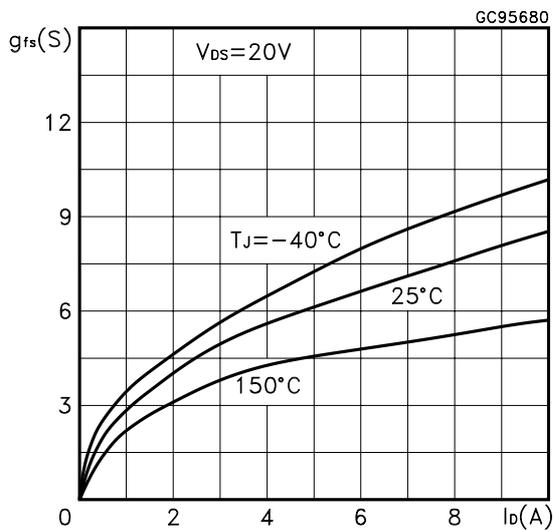
Output Characteristics **n-ch**



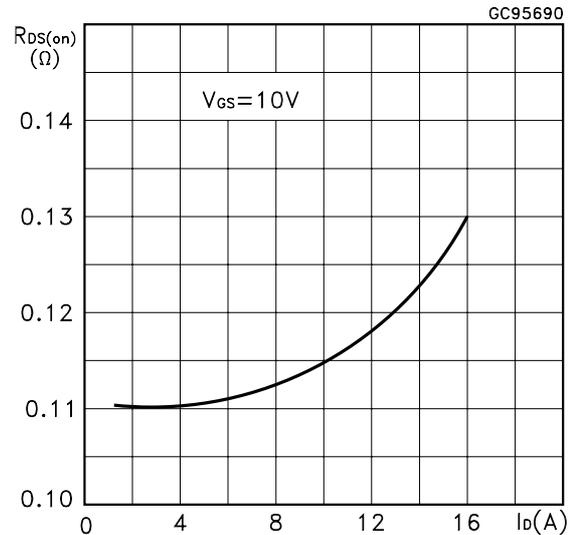
Transfer Characteristics **n-ch**



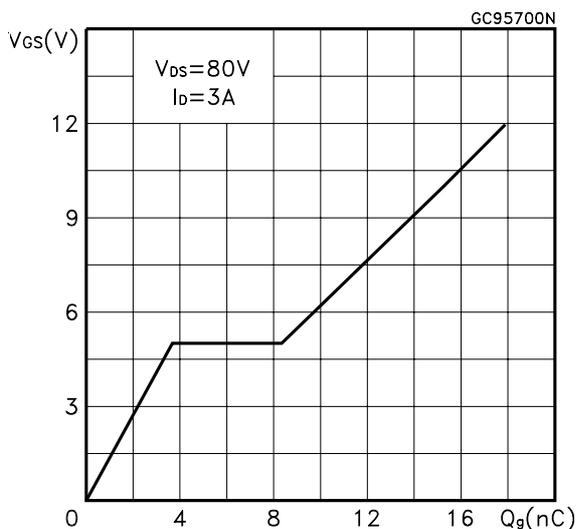
Transconductance **n-ch**



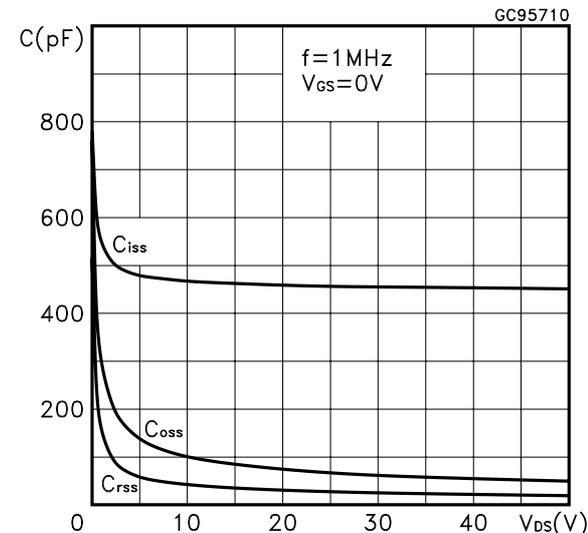
Static Drain-source On Resistance **n-ch**



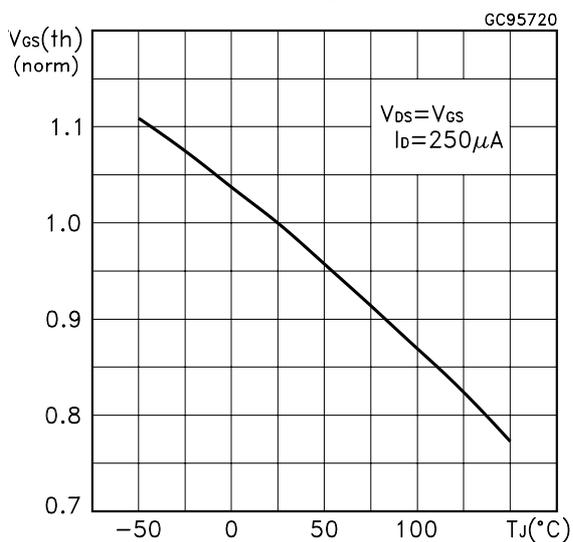
Gate Charge vs Gate-source Voltage **n-ch**



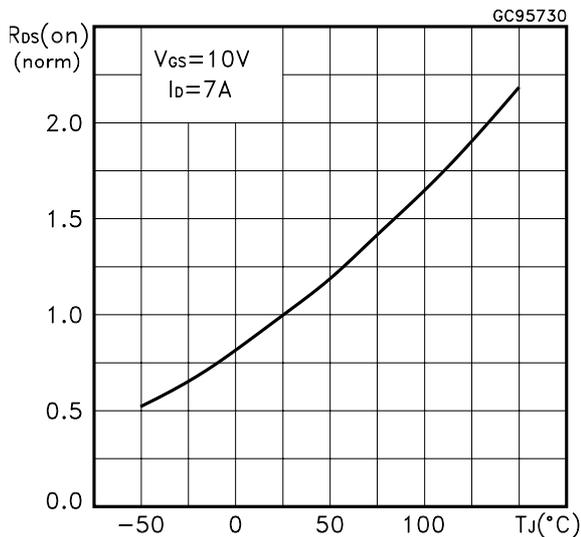
Capacitance Variations **n-ch**



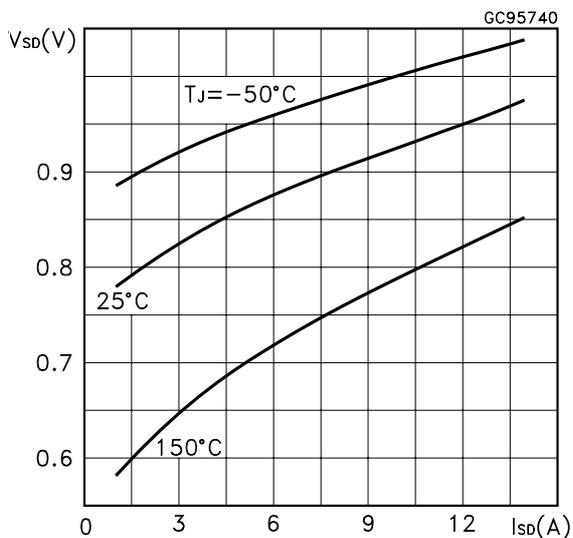
Normalized Gate Threshold Voltage vs Temperature **n-ch**



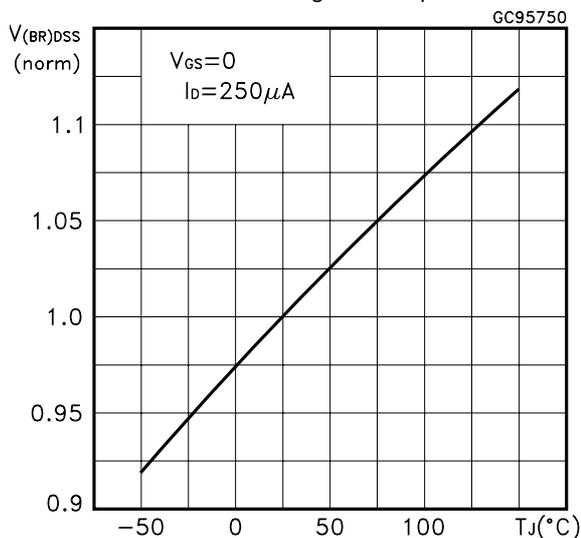
Normalized on Resistance vs Temperature **n-ch**



Source-drain Diode Forward Characteristics **n-ch**

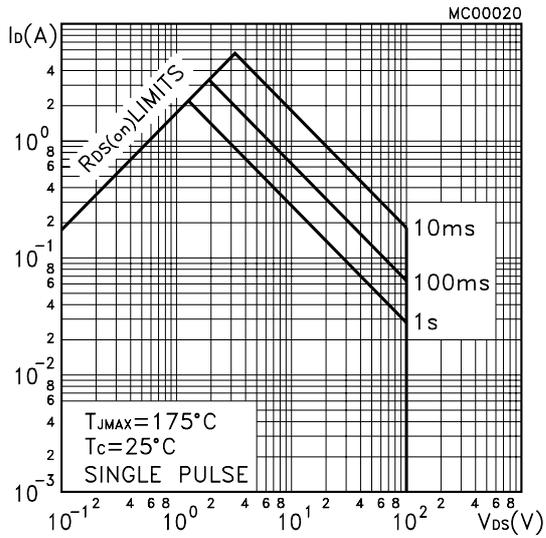


Normalized Breakdown Voltage vs Temperature **n-ch**

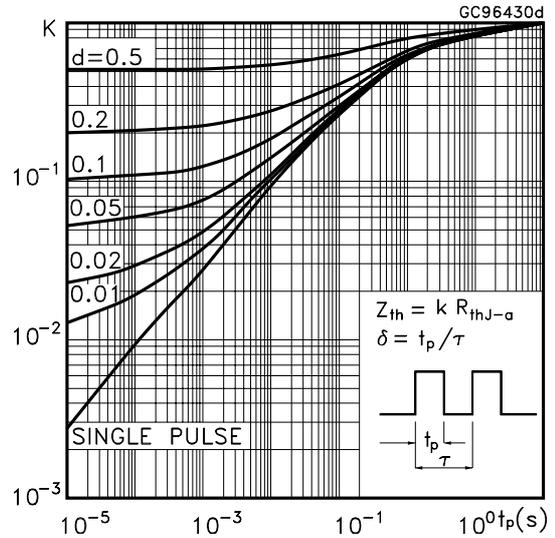


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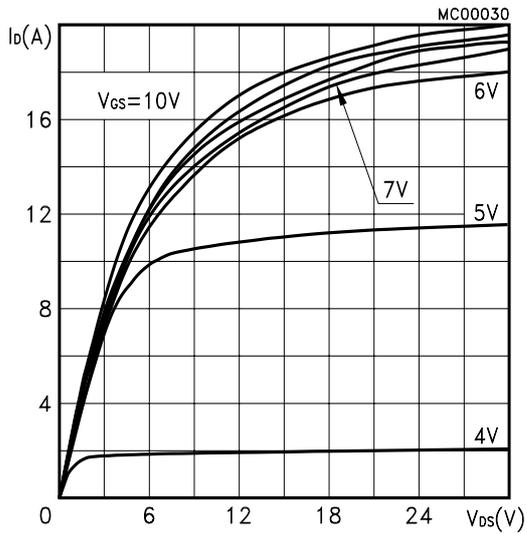
Safe Operating Area **p-ch**



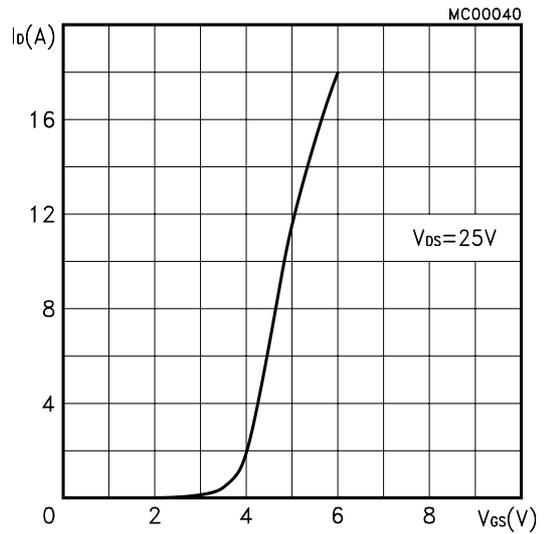
Thermal Impedance **p-ch**



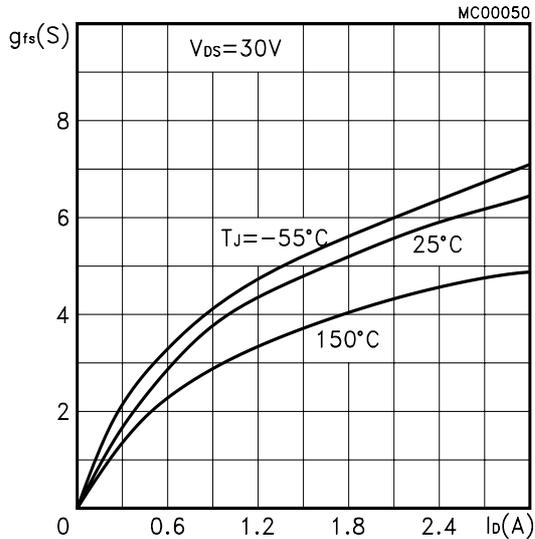
Output Characteristics **p-ch**



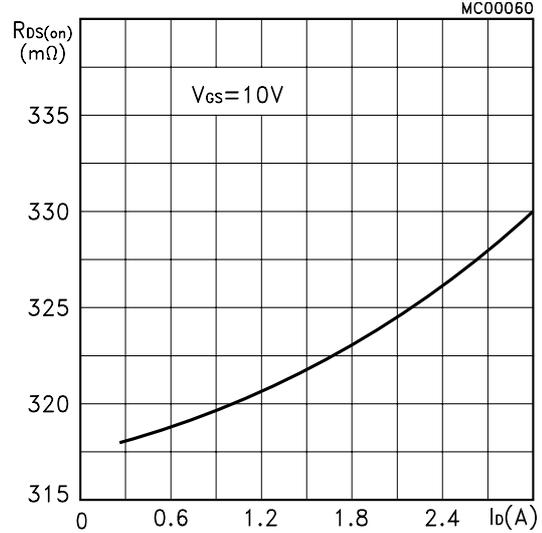
Transfer Characteristics **p-ch**



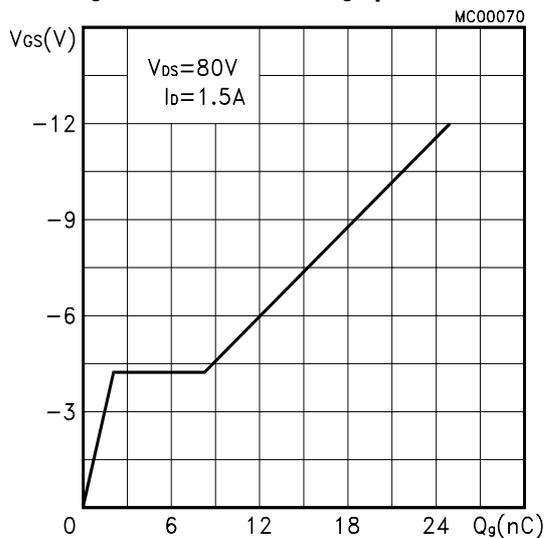
Transconductance **p-ch**



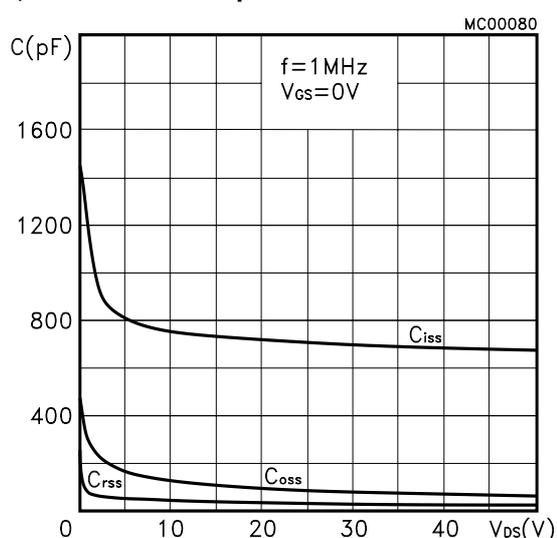
Static Drain-source On Resistance **p-ch**



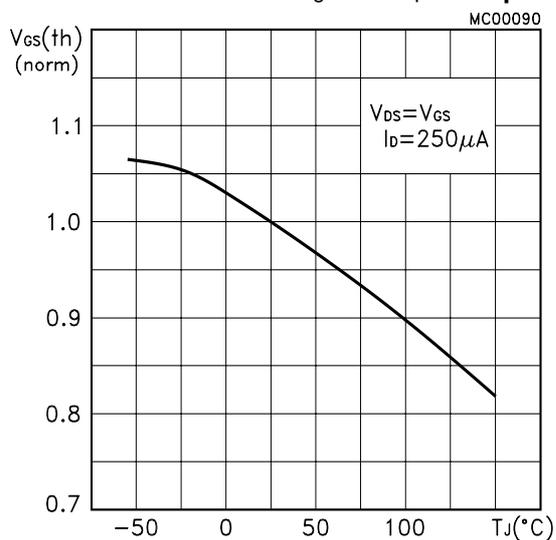
Gate Charge vs Gate-source Voltage **p-ch**



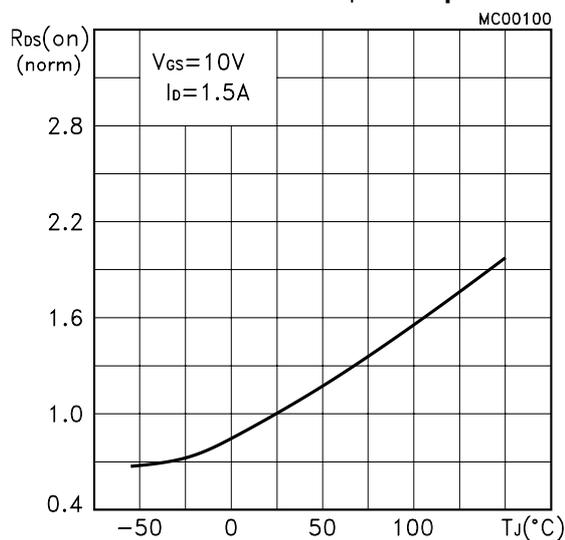
Capacitance Variations **p-ch**



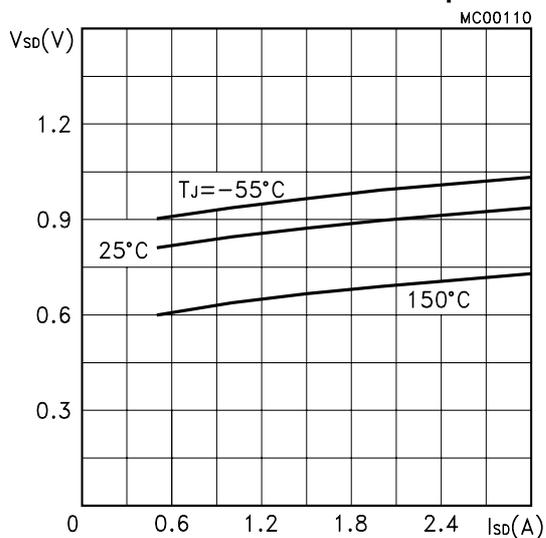
Normalized Gate Threshold Voltage vs Temperature **p-ch**



Normalized on Resistance vs Temperature **p-ch**



Source-drain Diode Forward Characteristics **p-ch**



Normalized Breakdown Voltage vs Temperature **p-ch**

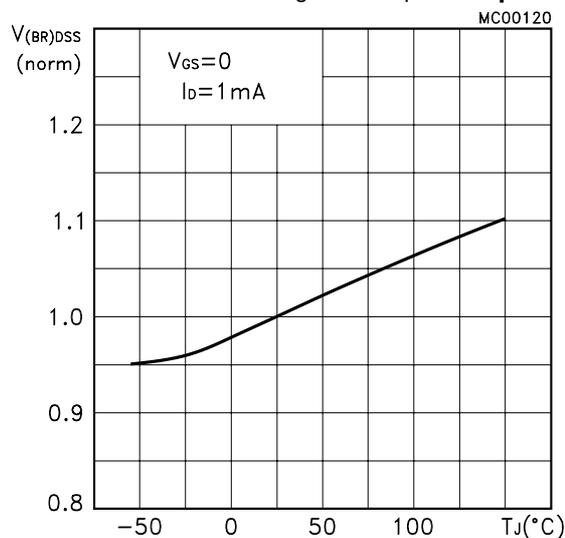


Fig. 1: Switching Times Test Circuits For Resistive Load

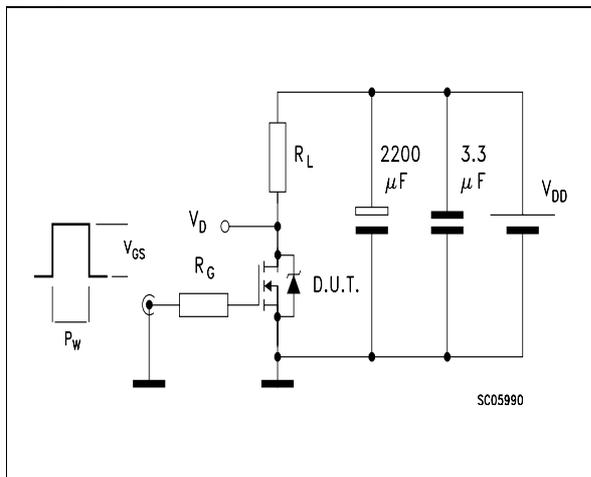


Fig. 2: Gate Charge test Circuit

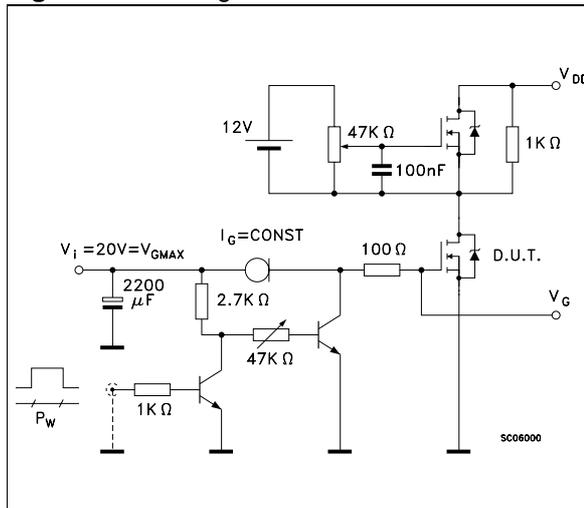
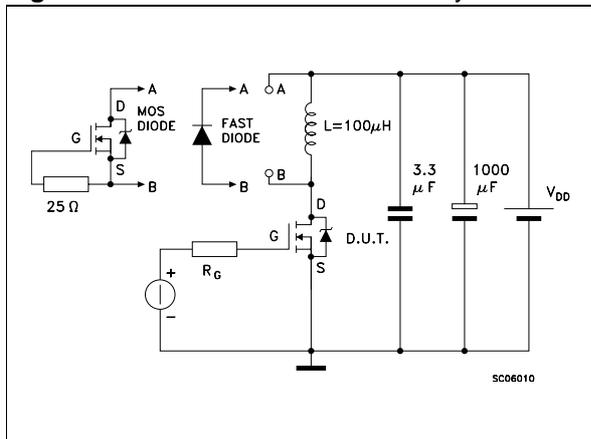
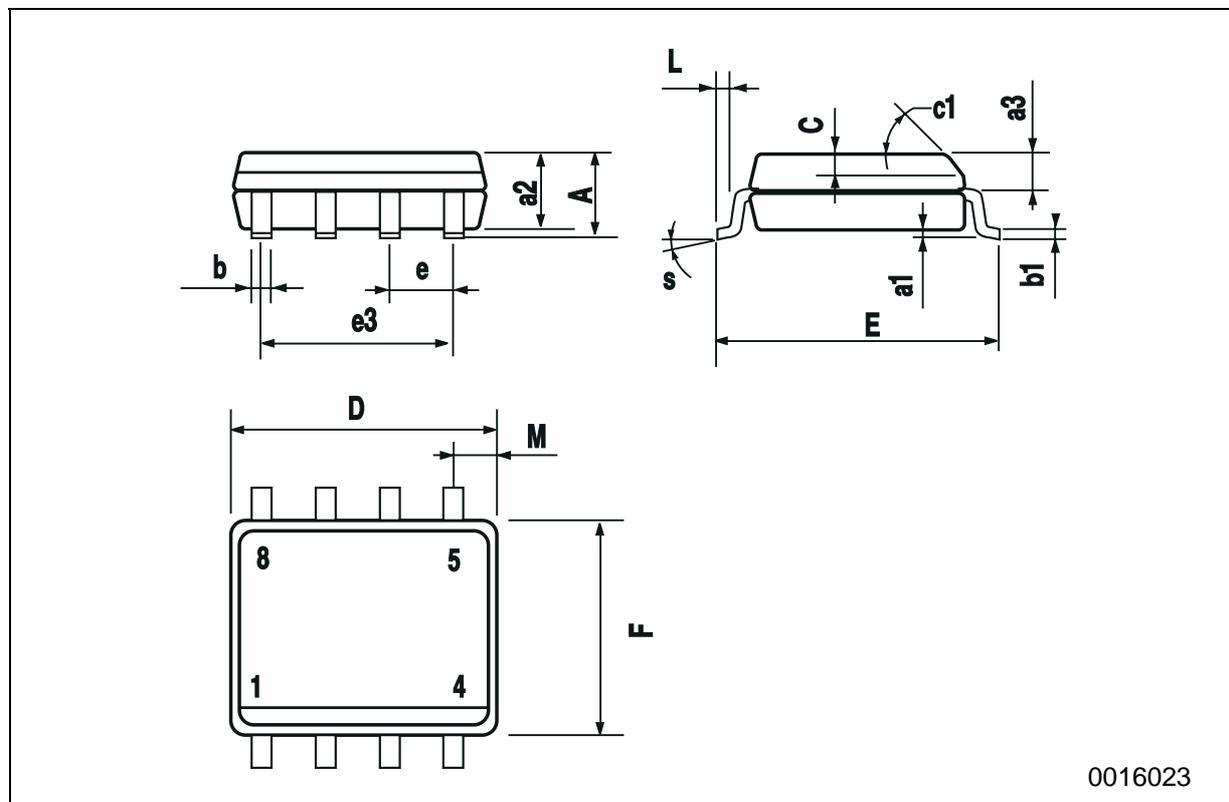


Fig. 3: Test Circuit For Diode Recovery Behaviour



SO-8 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



Revision History

Date	Revision	Description of Changes
Friday 18 June 2004	1.0.1	FIRST ISSUE

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