OKI Semiconductor

MSM6691

DRAM Interface IC

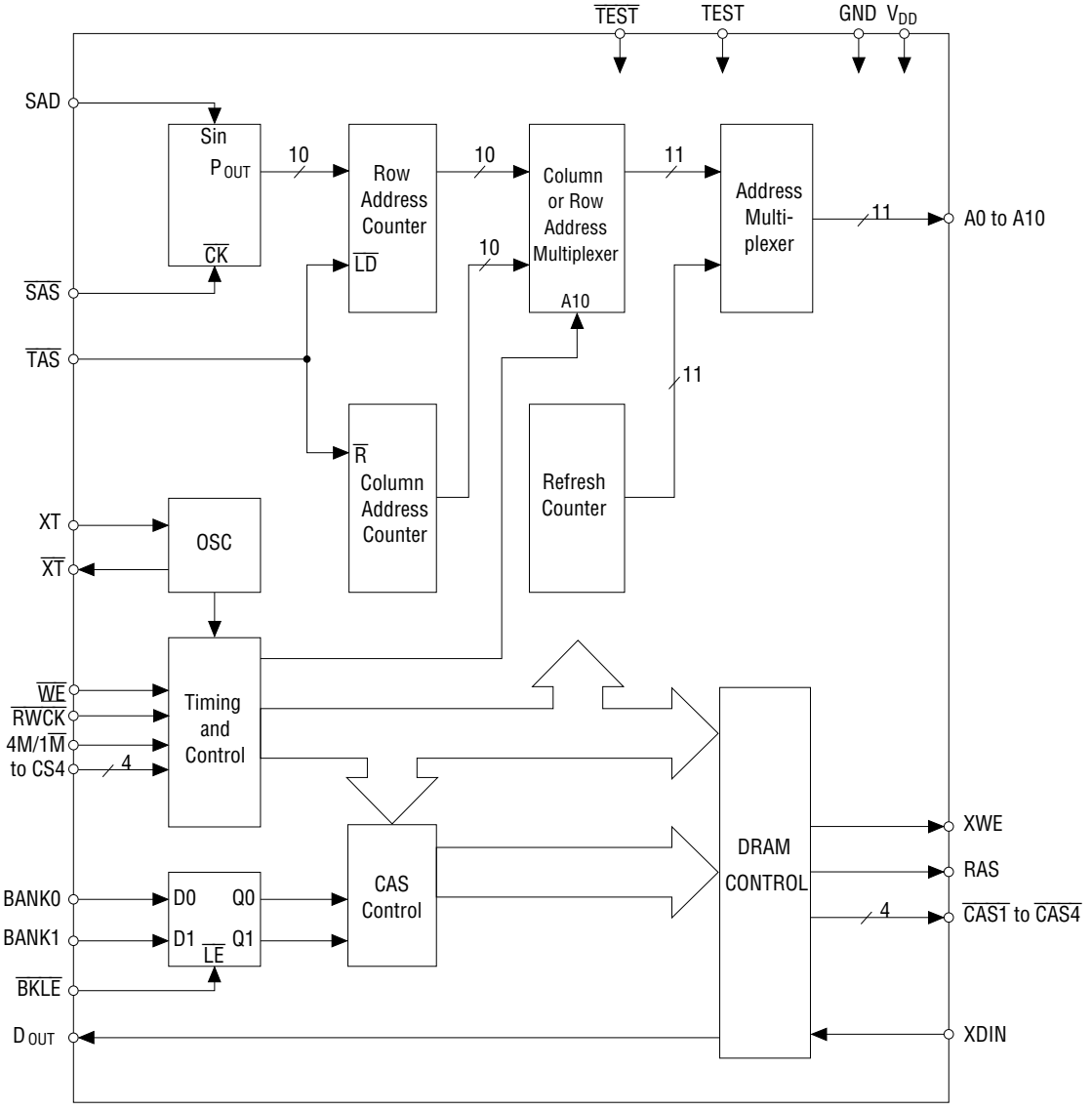
GENERAL DESCRIPTION

DRAMs can be used for voice storage by connecting the MSM6691 with OKI's integrate R/W (Read/Write) ICs, the MSM6388, and the MSM6588. The MSM6691 translates the signals associated with the dedicated serial register interface of the MSM6388 and MSM6588 driver interface when used in a stand-alone mode.

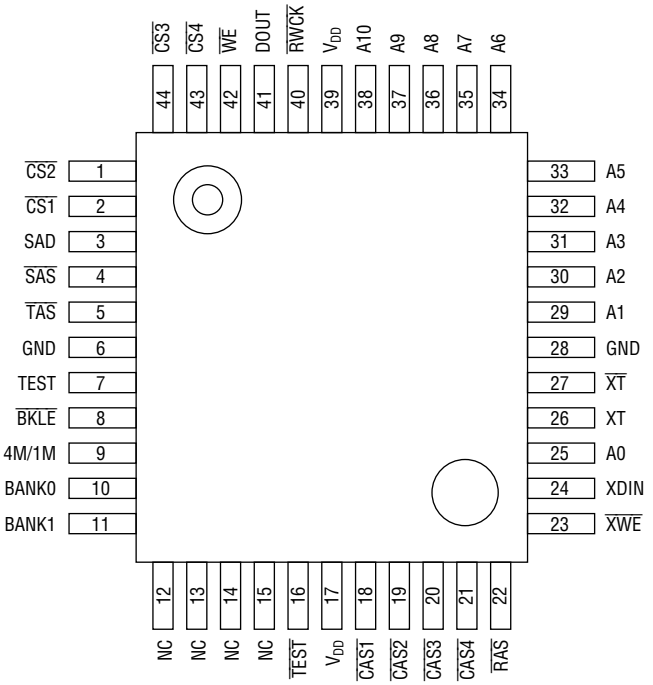
FEATURES

- DRAM (× 1-bit configuration)
- 1-Mbit DRAM (M 51100A, M511001A) : Four units can be used.
- 4-Mbit DRAM (M 514100A, M514101A) : Four units can be used.
- Power voltage : 5V single
- Built-in refresh circuit (RAS only refresh)
- Oscillation frequency : 8MHz (during refresh)
- Sampling frequency
- 4 kHz to 32 kHz when MSM6388 is connected.
- 4 kHz to 16 kHz when MSM6588 is connected.
- Package : 44-pin plastic QFP (QFP44-P-910-2K) (Product name : MSM6691GS-2K)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



44-Pin Plastic QFP

NC: No-connection pin

PIN DESCRIPTIONS

Symbol	Type	Description
V_{DD}	I	Power
GND	I	GND
XT	I	Oscillator
$\overline{XT}$	O	Oscillator
TEST	I	IC test. Set to "L".
$\overline{TEST}$	I	IC test. Set to "H".
SAD	I	Initial address of R/W
$\overline{SAS}$	I	Clock to input serial address data to internal register
$\overline{TAS}$	I	Load serial data, input to address register, and reset to internal address counter.
$\overline{RWCK}$	I	Clock to read and write data register information. At $\overline{RWCK}$ fall, internal operation starts. In read mode data input to XDIN is latched and output the DOUT terminal. In write mode, DIN (D I/O) output data MSM6388 (MSM6588) is input to the DIN pin of DRAM. At $\overline{RWCK}$ the fall internal address counter automatically increments, and address data is output from A_0 to A_{10}.
$\overline{WE}$	I	Select R/W modes
$\overline{XWE}$	O	Control DRAM
A0 to A10	O	Address control DRAM
$\overline{RAS}$	O	Control DRAM
$\overline{CAS1}$ $\overline{CAS2}$ $\overline{CAS3}$ $\overline{CAS4}$	O	Control DRAM
XDIN	I	Write data
DOUT	O	Read data
$\overline{CS1}$ $\overline{CS2}$ $\overline{CS3}$ $\overline{CS4}$	I	Chip select when 1-M DRAM is connected. Because input terminal to select most significant address when 4-M DRAM is connected.
4M/$\overline{1M}$	I	Select 4-M DRAM or 1-M DRAM for connection. "L" 1M DRAM connected; 4-M DRAM connected
BANK0 BANK1	I	Chip select data when 4-M DRAM is connedted. Terminal is used to select desired DRAM from DRAMs connected to select terminals. $\overline{CAS1}$ to $\overline{CAS4}$. Set to "L" when 1-M DRAM is connected.
$\overline{BKLE}$	I	Latch data, input to BANK0, BANK1, when 4-M DRAM is used. "L" indicates a "through" setting. "H" indicates a "latch" setting. Set to "L" when 1-M DRAM is used.

Select Terminal	Bank1	Bank0
$\overline{CAS1}$	L	L
$\overline{CAS2}$	L	H
$\overline{CAS3}$	H	L
$\overline{CAS4}$	H	H

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta=25°C Standard is GND=0V	–0.5 to +7	V
Input Voltage	V_I		–0.5 to V_{DD}+0.5	V
Output Voltage	V_O		–0.5 to V_{DD}+0.5	V
Input Current	I_I		–10 to +10	mA
Output Current	I_O		–20 to +20	mA
Storage Temperature	T_{STG}	—	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(GND=0V)

Parameter	Symbol	Range	Unit
Power Supply Voltage	V_{DD}	4.5 to +5.5	V
Operating Temperature	T_{OP}	–40 to +85	°C
Oscillation Frequency	f_{OSC}	8	MHz

ELECTRICAL CHARACTERISTICS

DC Characteristics

(Ta=–40 to +85°C, V_{DD}=5V±10%, GND=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
H Level Input Voltage	V_{IH}	—	3.5	—	V_{DD}+0.3	V
L Level Input Voltage	V_{IL}	—	–0.3	—	1.5	V
H Level Input Current	I_{IH}	$V_{IH}=V_{DD}$	—	0.01	10	µA
L Level Input Current	I_{IL}	V_{IL}=GND	–10	–0.01	—	µA
Tri-state Output Leak Current (Including open drain output)	I_{OZH}	$V_{OH}=V_{DD}$	—	0.01	10	µA
	I_{OZL}	V_{OL}=GND	–10	–0.01	—	
H Level Output Voltage	V_{OH}	I_{OH}=–5.0mA	2.4	4.20	V_{DD}	V
L Level Output Voltage	V_{OL}	I_{OL}=+5.0mA	GND	0.24	0.5	V
Operating Current Consumption	I_{DD}	Output Open $V_{IH}=V_{DD}$ f_{OSC}=8MHz V_{IL}=GND	—	—	3	mA

*1 Standard when V_{DD}=5.0V, Ta=25°C

APPLICATION CIRCUITS

Figure 2 indicates an example of the circuits used when the MSM6388 (M6588) is used with four 1-Mbit DRAMs.

Figure 3 indicates an example of the circuits used when MSM6388 (M6588) is used with four 4-Mbit DRAMs.

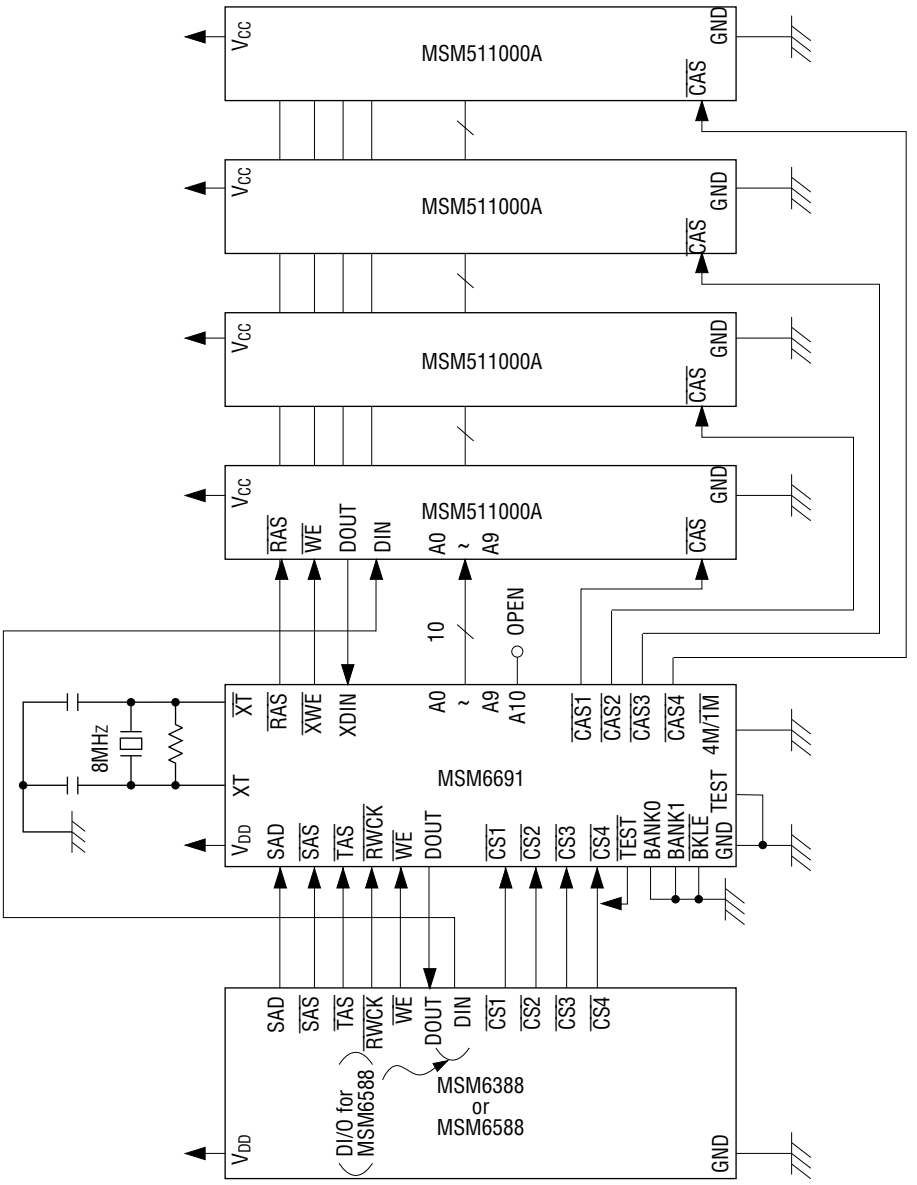


Figure 2. Example of Interfacing with Four 1-Mbit DRAMs

One of four DRAMs can be selected by BANK0 and BANK1.

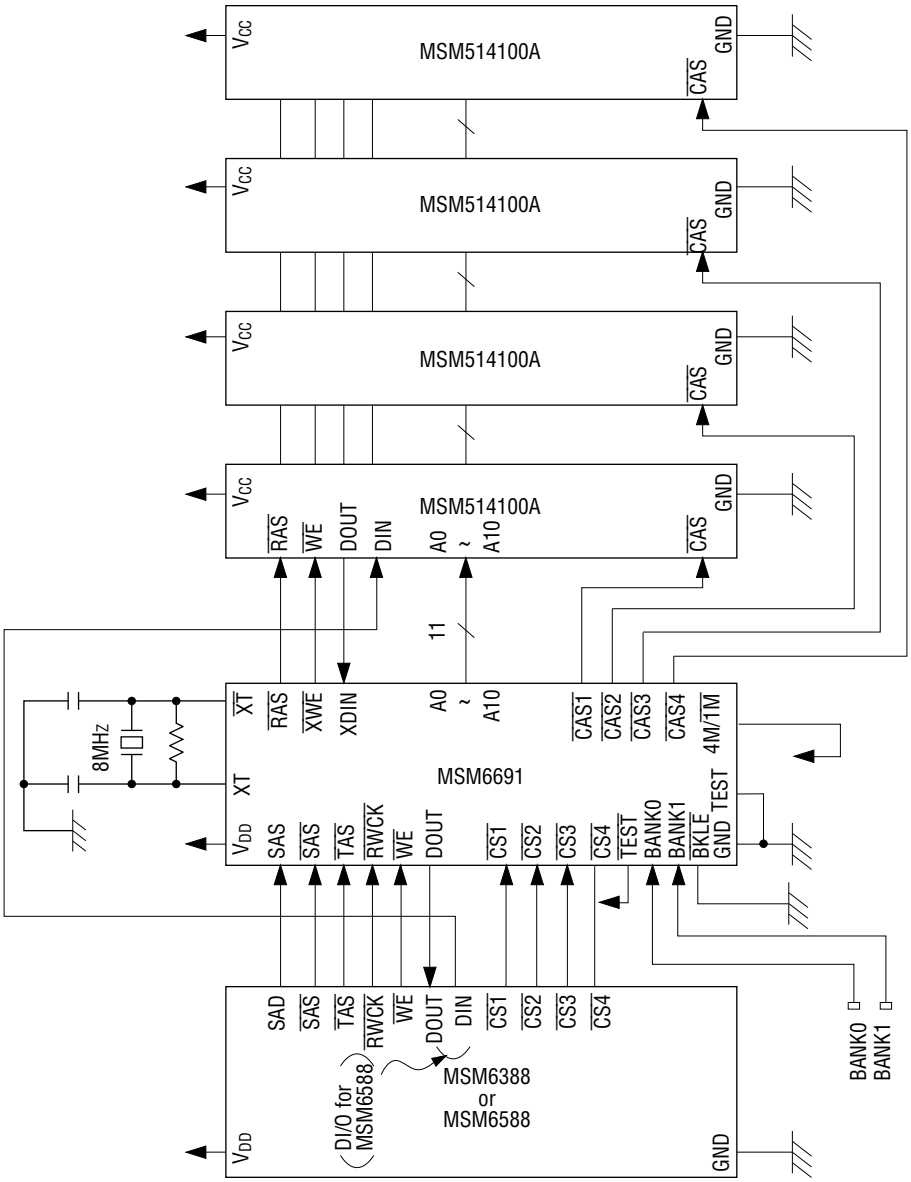


Figure 3. Example of Interfacing with Four 4-Mbit DRAMs