54/7476
54H/74H76
54LS/74LS76

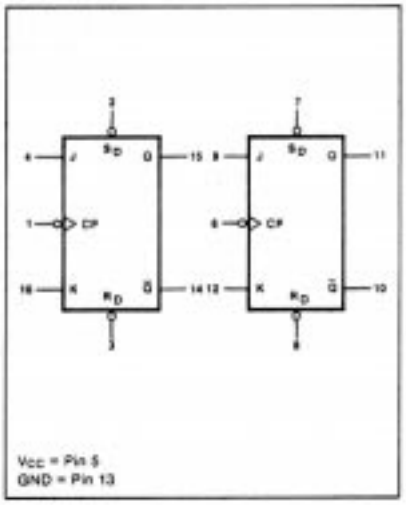
DESCRIPTION

The "76" is a Dual JK Flip-Flop with individual J, K, Clock, Set and Reset inputs. The 7476 and 74H76 are positive pulse triggered flip-flops. JK information is loaded into the master while the Clock is HIGH and transferred to the slave on the HIGH-to-LOW Clock transition. The J and K inputs must be stable while the Clock is HIGH for conventional operation.

The 74LS76 is a negative edge triggered flip-flop. The J and K inputs must be stable only one setup time prior to the HIGH-to-LOW Clock transition.

The Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) are asynchronous active LOW inputs. When LOW, they override the Clock and data inputs forcing the outputs to the steady state levels as shown in the Truth Table.

LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to +125°C
Plastic DIP	Fig A Fig A	N7476N • N74H76N N74LS76N	
Ceramic DIP	Fig A Fig A	N7476F • N74H76F N74LS76F	S5476F • S54H76F S54LS76F
Flatpak	Fig A Fig A		S5476W • S54H76W S54LS76W

PIN CONFIGURATION

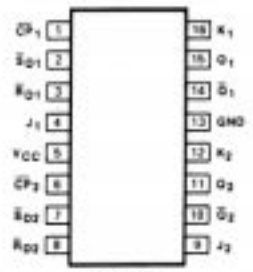


Figure A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE [a]

PINS			54/74	54H/74H	54S/74S	54LS/74LS
$\overline{CP}$	Clock input	I_{IH} (μA) I_{IL} (mA)	80 -3.2	50 -2.0		80 -0.8
$\overline{R}_D$	Reset input	I_{IH} (μA) I_{IL} (mA)	80 -3.2	100 -4.0		60 -0.8
$\overline{S}_D$	Set input	I_{IH} (μA) I_{IL} (mA)	80 -3.2	100 -4.0		60 -0.8
JK	Data inputs	I_{IH} (μA) I_{IL} (mA)	40 -1.6	50 -2.0		20 -0.4
Q & $\overline{Q}$	Outputs	I_{OH} (μA) I_{OL} (mA)	-400 16	-500 20		-400 4/8[a]

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE [b]

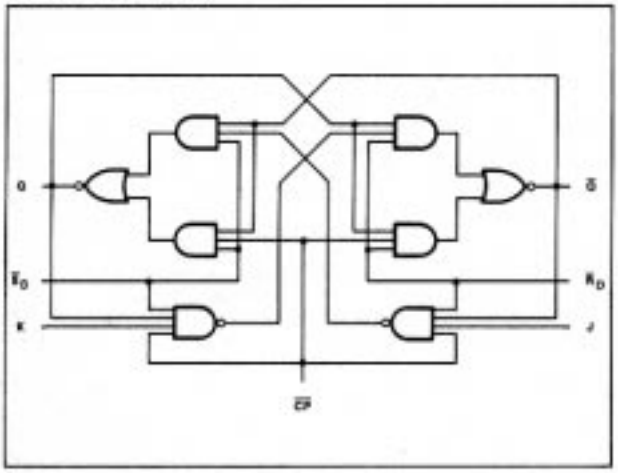
PARAMETER		TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
			Min	Max	Min	Max	Min	Max	Min	Max	
I_{CC}	Supply current	V_{CC} = Max, V_{CP} = 0V		40		50				8.0	mA

NOTES

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H and see inside back cover for 54S/74S and 54LS/74LS specification.

LOGIC DIAGRAM



MODE SELECT—TRUTH TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	$\bar{S}_D$	$\bar{R}_D$	$\overline{CP}$ (d)	J	K	Q	$\bar{Q}$
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	X	L	H
Undetermined (c)	L	L	X	X	X	H	H
Toggle	H	H	⎍	h	h	$\bar{q}$	q
Load "0" (Reset)	H	H	⎍	l	h	L	H
Load "1" (Set)	H	H	⎍	h	l	H	L
Hold "no change"	H	H	⎍	l	l	q	$\bar{q}$

H = HIGH voltage level steady state.
L = LOW voltage level steady state.
h = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition. (e)
l = LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition. (e)
X = Don't care.
q = Lower case letters indicate the state of the referenced output prior to the HIGH to LOW Clock transition.
⎍ = Positive Clock pulse.

AC CHARACTERISTICS T_A = 25°C (See Section 4 for Waveforms and Conditions)

PARAMETER		TEST CONDITIONS	54/74 C_L = 15 pF, R_L = 400Ω		54H/74H C_L = 25 pF, R_L = 280Ω		54S/74S		54LS/74LS C_L = 15pF, R_L = 2kΩ		UNIT
			Min	Max	Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Clock frequency	Waveform 4	15		25				30		MHz
t_{PLH}	Propagation delay Clock to Output	Waveform 4		25		21				20	ns
t_{PHL}				40		27				30	ns
t_{PLH}	Propagation delay $\bar{S}_D$ or $\bar{R}_D$ to Output	Waveform 5		25		13				20	ns
t_{PHL}				40		24				30	ns

AC SETUP REQUIREMENTS T_A = 25°C (See Section 4 for Waveforms and Conditions)

PARAMETER		TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{w(H)}$	Clock pulse width (HIGH)	Waveform 4	20		12				20		ns
$t_{w(L)}$	Clock pulse width (LOW)	Waveform 4	47		28				13		ns
$t_{w(L)}$	Set or Reset pulse width (LOW)	Waveform 5	25		16				25		ns
t_s	Setup time J or K to Clock	Waveform 4	(e)		(e)				20		ns
t_h	Hold time J or K to Clock	Waveform 4	0		0				0		ns

NOTES

c. Both outputs will be HIGH while both $\bar{S}_D$ and $\bar{R}_D$ are LOW, but the output states are unpredictable if $\bar{S}_D$ and $\bar{R}_D$ go HIGH simultaneously.
d. The 74LS76 is edge triggered. Data must be stable one setup time prior to the negative edge of the Clock for predictable operation.
e. The J and K inputs of the 7476 and 74H76 must be stable while the Clock is HIGH for conventional operation.