CL-GD7541/GD7543

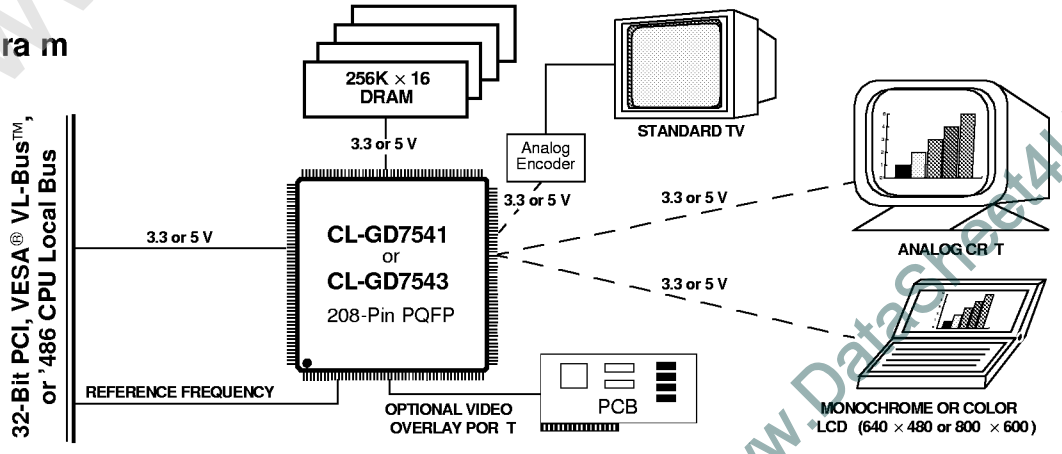
Preliminary Data Book

GUI-Accelerated SVGA LCD Controller for Portable Computers

FEATURES

- **Single-chip Super VGA LCD controller**
  - Pin compatible with CL-GD7542
  - IBM® VGA hardware-compatible
- **GUI acceleration**
  - BitBLT (bit block transfer) engine
  - Color expansion for 8- or 16-bit pixels
  - True packed-pixel addressing for 8 and 16 bpp
  - Programmable linear memory addressing
  - 32 × 32 or 64 × 64 hardware cursor
- **Multimedia acceleration and enhancement**
  - 8-bit feature connector port for video overlay
  - Interface to analog encoders for NTSC/PAL-out
  - MVA™ (MotionVideo™ Acceleration) *CL-GD7543 only*
    - True-color, full-motion video playback
    - Multi-format frame buffer
    - Integrated YCrCb: RGB color space converter
    - 2× horizontal/vertical hardware scaling
- **32-bit direct-connect CPU host bus interfaces**
  - '486 CPU local bus (up to 50 MHz @ 5 V)
  - VESA® VL-Bus™
  - PCI system bus with burst support: big-endian byte-order hardware support for PowerPC™
- **Scalable 1- and 2-Mbyte display memory**
  - Two or four 256K × 16 DRAMs, or four 512K × 8 DRAMs
  - Extended-Data-Out/Hyper-Page-Mode DRAM support
- **Integrated programmable frequency synthesizer**
  - Core VCLK up to 80 MHz @ 5 V; 77 MHz @ 3.3 V
  - Core MCLK up to 60 MHz @ 5 V; 50 MHz @ 3.3 V
  - Vertical refresh rates up to 75 Hz (depending on the graphics mode, MCLK, and voltage level of core VCC)
- **64 × 64 pixel size hardware pop-up icons**
  - Displays up to four independently controlled, 4-color icons
- **Integrated 24-bit true-color RAMDAC**
  - 640 × 480 non-interlaced, 16M colors (CL-GD7543 only)
  - 800 × 600 non-interlaced, 64K colors
  - 1024 × 768 non-interlaced, 256 colors
  - 1280 × 1024 interlaced, 256 colors
- **Support for 640 × 480 and 800 × 600 LCDs**
  - Dual-scan color and monochrome STN LCDs
  - Color TFT LCDs (9-, 12-, 18-, and 24-bit interfaces)
  - Dithering algorithm automatically adds up to 6 bits per primary color without decreasing spatial resolution
  - Enhanced frame-rate modulation algorithm improves display quality with fast-response STN LCDs (~100 ms)
  - SimulSCAN™ (simultaneous CRT and LCD)
  - Full-screen VGA support on 800 × 600 LCDs
- **Power-management capabilities**
  - 3.3-V, 5.0-V, and mixed-voltage operation
  - Hardware-suspend input pin or software-suspend option
  - Self-refresh DRAMs or DRAM refresh via 32-kHz clock
  - Internal timers for Standby mode and backlight control
  - LCD power sequencing
  - VESA® DPMS (Display Power Management Signaling)
  - DDC-1 (Display Data Channel) support
- **EIAJ standard 208-pin quad flat package**

System Block Diagram



OVERVIEW

The GUI-accelerated SVGA LCD controllers — CL-GD7541 and CL-GD7543 — are the latest members of the pin compatible CL-GD754X family. They provide the performance and integration required for the next generation of mid-range to premium portable computers.

The CL-GD7541/GD7543 uses Cirrus Logic's advanced 0.6-µm CMOS process to provide improved 3.3-V operation and support for 1024 × 768 CRT refresh rates of 70 Hz. In addition, increased performance can be achieved through the use of high-speed Extended-Data-Out (EDO) / Hyper-Page-Mode DRAMs. A complete graphics subsystem can be built using only three active components: the CL-GD7541/GD7543 and two DRAMs.

Both the CL-GD7541 and CL-GD7543 provide the following CL-GD7542 features: BitBLT GUI acceleration, true-color capability, support for 800 × 600 LCDs, and mixed-voltage operation for low power consumption.

The CL-GD7543 fully supports all features of the CL-GD7542, including MotionVideo™ Acceleration (MVA™) for playback of Video for Windows .AVI (audio-video interleaved) files.

For the cost-sensitive value market, the CL-GD7541 provides most of the performance and features of the CL-GD7543, including TV-out, Feature Connector, 3D game acceleration, and 2-Mbyte display memory. However, the CL-GD7541 does not support the MVA hardware playback enhancements, relying instead upon standard primary surface DCI support.

UNIQUE FEATURES

Design Flexibility

- Pin-compatible with CL-GD7542
- Big-endian byte ordering in display memory with PCI host interface

High Performance

- BitBLT engine, color expansion, hardware cursor, linear addressing, and 32-bit memory interface
- 32-bit local bus interface, operating at up to 33 MHz, includes support for PCI with burst mode
- Hardware 'pop-up' icons

Multimedia

- 8-bit dynamic Feature Connector port
- Interface to NTSC/PAL analog encoders
- Drivers supplied for 3D-graphics libraries and emerging APIs (advanced programming interface) for games

MVA™ (CL-GD7543 only)

- MVA™ (MotionVideo™ Acceleration)
- Multi-format frame buffer and YCrCb-to-RGB color space conversion
- 2× hardware scaling for playback

Enhanced LCD Support

- 800 × 600 LCD support (both TFT and dual-scan STN) with comprehensive resolution-compensation support
- Enhanced frame-rate modulation
- Intelligent dithering algorithm expands the number of bits per primary color (RGB) on TFT or STN LCDs

Power Management

- 3.3-V, 5.0-V, or mixed-voltage support
- Hardware-initiated Standby and Suspend modes and VESA® DPMS support for CRTs

BENEFITS

- ❒ CL-GD754X family offers products for a wide range of market segments. Design knowledge gained with any CL-GD754X device can be leveraged over entire CL-GD754X family.
- ❒ Supports 'X86 designs with little-endian data; supports PowerPC™ designs with big-endian data.
- ❒ Accelerates GUIs such as Microsoft® Windows®; provides high resolution and color-depth capabilities.
- ❒ Increases system throughput; PCI interface allows use in 'X86, PowerPC™, or other platforms.
- ❒ Provides hot-key display for on-screen symbols such as battery 'fuel gauge' and contrast/brightness controls.
- ❒ Allows overlay capability for live 'TV in a window'.
- ❒ Integrated design can be developed to display computer-generated data on a TV or to record to a VCR.
- ❒ Supports emerging standards for DOS and Windows®-based 3D applications.
- ❒ Hardware enhancement for playback of Video for Windows .AVI files.
- ❒ Displays separate graphics and video windows at independent color depths.
- ❒ Enlarges video clips with little or no frame-rate reduction.
- ❒ Supports latest LCD technology and enables full use of the display area whether in graphics or text mode.
- ❒ Improves display quality; increases stability of shades.
- ❒ Displays high- and true-color modes with smooth shading (no contouring) on all supported LCD types.
- ❒ Minimizes operating power consumption; provides manufacturing flexibility.
- ❒ Reduces power consumption; supports Energy Star monitors for 'green PC' compliance.

SOFTWARE SUPPORT

Operating System and Application Software Drivers

Software Drivers[a]	Resolution Supported	Number of Colors
Microsoft®/Intel® DCI™ (Display Control Interface)	640 × 480, 800 × 600, 1024 × 768, 1280 × 1024 640 × 480, 800 × 600	256 65,536
Microsoft® Windows® v3.1	640 × 480, 800 × 600, 1024 × 768, 1280 × 1024 640 × 480, 800 × 600 640 × 480	256 65,536 16.8 million (CL-GD7543 only)
Microsoft® Windows NT™ v3.1	640 × 480, 800 × 600, 1024 × 768	16 and 256
OS/2® v2.0, v2.1	640 × 480, 800 × 600, 1024 × 768 640 × 480, 800 × 600 640 × 480	16 and 256 65,536 16.8 million (CL-GD7543 only)
AutoCAD® v11, v12	640 × 480, 800 × 600, 1024 × 768 640 × 480, 800 × 600 640 × 480	16 and 256 65,536 16.8 million (CL-GD7543 only)
Autoshade® v2.0 3D Studio® v1, v2	640 × 480, 800 × 600, 1024 × 768 640 × 480, 800 × 600 640 × 480	256 65,536 16.8 million (CL-GD7543 only)

[a] Driver support for additional applications is provided by independent software vendors, either with specific drivers or through VESA mode support. In many instances, existing drivers for the CL-GD542X can be used with the CL-GD7541/GD7543. For more information concerning driver support, contact the software manufacturer.

BIOS

Feature	*Benefit*
■ Available as 48-Kbyte BIOS to provide optimum performance with VGA and VESA® extended mode support, or as a 32-Kbyte subset with a 16-Kbyte-relocatable module or loaded as TSRs (terminate and stay resident)	❒ Provides system design options for the best combination of performance and functionality.
■ Fully IBM® VGA-compatible BIOS	❒ Ensures compatibility with the existing base of PC applications.
■ VESA® VBE (VGA BIOS extensions) 1.2 and PM (power management) support	❒ Compatible with industry standard for extended mode support beyond VGA and power-management control.

Software Utilities

Utility	Function
AutoResolution Switching	Windows® application for automatically switching display resolutions (for example, from a 1024 × 768 CRT to lower-resolution 640 × 480 or 800 × 600 LCDs) without relaunching Windows
CLDemo	Demonstration program to test various capabilities of the CL-GD7541/GD7543
CLMode	Video mode and video display configuration utility suitable for end-use distribution (includes foreign language translations)
OEMSI	BIOS-customization utility for OEM development use
PCLRegs	VGA controller register viewer/editor for OEM development use
Switcher	Video configuration TSR (terminate and stay resident)
WinMode	Windows® application for graphics mode and display type configuration (includes foreign language translations, selectable from within the utility)

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1. PIN INFORM ATION

1.1 Pin Diagram

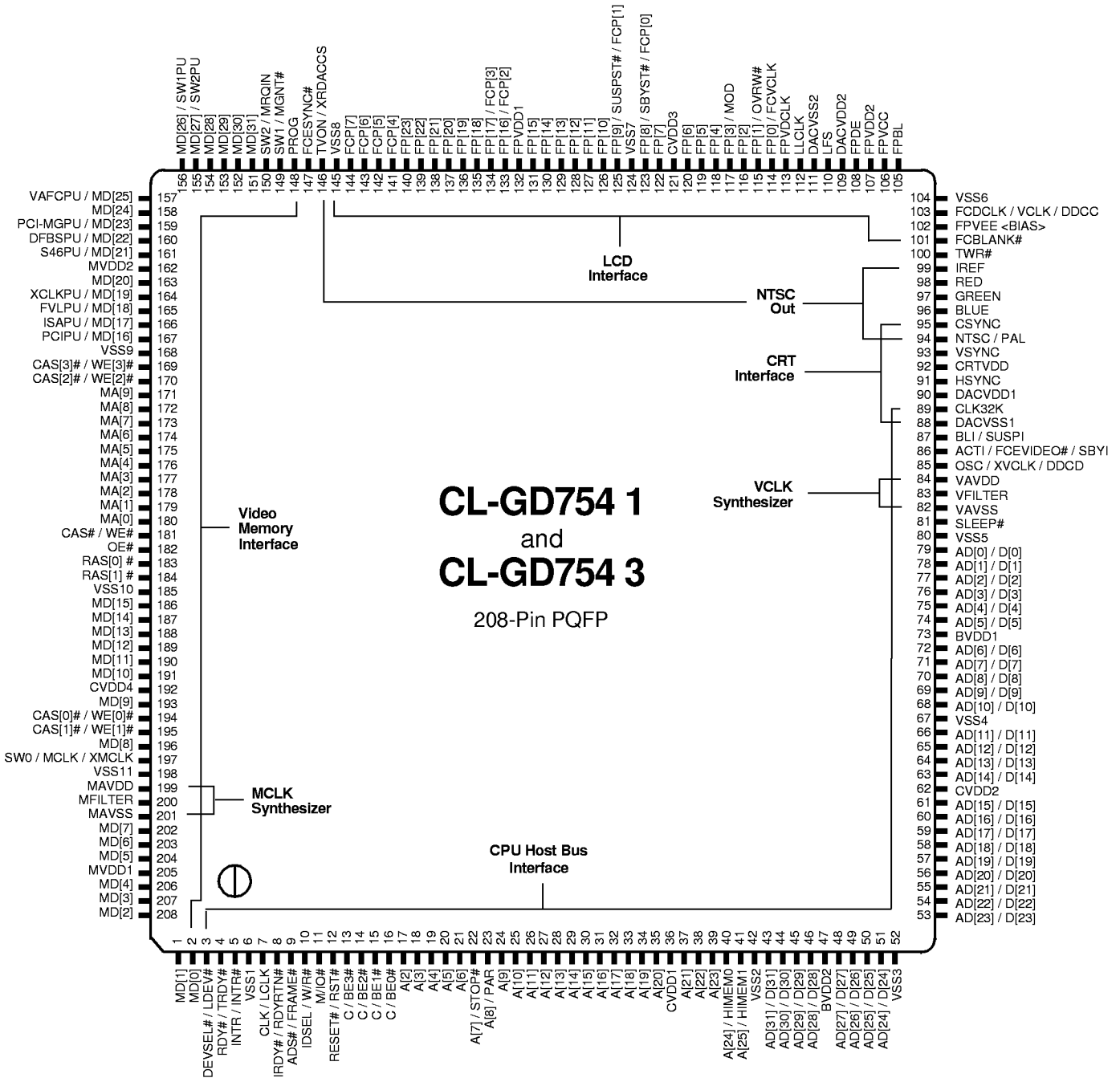


Figure 1-1. Pin Diagram

1.2 Pin Tables

Table 1-1. CL-GD7541/GD7543 Pins in Numerical Order

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	MD [1]	37	A [21]	73	BVDD1
2	MD [0]	38	A [22]	74	AD [5] / D [5]
3	DEVSEL# / LDEV#	39	A [23]	75	AD [4] / D [4]
4	RDY# / TRDY#	40	A [24] / HIMEM0	76	AD [3] / D [3]
5	INTR / INTR#	41	A [25] / HIMEM1	77	AD [2] / D [2]
6	VSS1	42	VSS2	78	AD [1] / D [1]
7	CLK / LCLK	43	AD [31] / D [31]	79	AD [0] / D [0]
8	IRDY# / RDYRTN#	44	AD [30] / D [30]	80	VSS5
9	ADS# / FRAME#	45	AD [29] / D [29]	81	SLEEP#
10	IDSEL / W/R#	46	AD [28] / D [28]	82	VAVSS
11	M/IO#	47	BVDD2	83	VFILTER
12	RESET# / RST#	48	AD [27] / D [27]	84	VAVDD
13	C / BE3#	49	AD [26] / D [26]	85	OSC / XVCLK / DDCD
14	C / BE2#	50	AD [25] / D [25]	86	ACTI / FCEVIDEO# / SBYI
15	C / BE1#	51	AD [24] / D [24]	87	BLI / SUSPI
16	C / BE0#	52	VSS3	88	DACVSS1
17	A [2]	53	AD [23] / D [23]	89	CLK32K
18	A [3]	54	AD [22] / D [22]	90	DACVDD1
19	A [4]	55	AD [21] / D [21]	91	HSYNC
20	A [5]	56	AD [20] / D [20]	92	CRTVDD
21	A [6]	57	AD [19] / D [19]	93	VSYNC
22	A [7] / STOP#	58	AD [18] / D [18]	94	NTSC / PAL
23	A [8] / PAR	59	AD [17] / D [17]	95	CSYNC
24	A [9]	60	AD [16] / D [16]	96	BLUE
25	A [10]	61	AD [15] / D [15]	97	GREEN
26	A [11]	62	CVDD2	98	RED
27	A [12]	63	AD [14] / D [14]	99	IREF
28	A [13]	64	AD [13] / D [13]	100	TWR#
29	A [14]	65	AD [12] / D [12]	101	FCBLANK#
30	A [15]	66	AD [11] / D [11]	102	FPVEE <BIAS>
31	A [16]	67	VSS4	103	FCDCLK / VCLK / DDCC
32	A [17]	68	AD [10] / D [10]	104	VSS6
33	A [18]	69	AD [9] / D [9]	105	FPBL
34	A [19]	70	AD [8] / D [8]	106	FPVCC
35	A [20]	71	AD [7] / D [7]	107	FPVDD2
36	CVDD1	72	AD [6] / D [6]	108	FPDE

Table 1-1. CL-GD7541/GD754 3 Pins in Numerical Orde r *(cont.)*

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
109	DACVDD2	143	FCP [6]	177	MA [3]
110	LFS	144	FCP [7]	178	MA [2]
111	DACVSS2	145	VSS8	179	MA [1]
112	LLCLK	146	TVON / XRDACCS	180	MA [0]
113	FPVDCLK	147	FCESYNC#	181	CAS# / WE#
114	FP [0] / FCVCLK	148	PROG	182	OE#
115	FP [1] / OVRW#	149	SW1 / **MGNT#**	183	RAS [0]
116	FP [2]	150	SW2 / **MRQIN**	184	RAS [1]
117	FP [3] / MOD	151	MD [31]	185	VSS10
118	FP [4]	152	MD [30]	186	MD [15]
119	FP [5]	153	MD [29]	187	MD [14]
120	FP [6]	154	MD [28]	188	MD [13]
121	CVDD3	155	MD [27] / **SW2PU**	189	MD [12]
122	FP [7]	156	MD [26] / **SW1PU**	190	MD [11]
123	FP [8] / SBYST# / FCP [0]	157*	MD [25] / FCPU	191	MD [10]
124	VSS7	158	MD [24]	192	CVDD4
125	FP [9] / SUSPST# / FCP [1]	159*	MD [23] / PCI-MGPU	193	MD [9]
126	FP [10]	160*	MD [22] / **DFBSPU**	194	CAS [0]# / WE [0]#
127	FP [11]	161*	MD [21] / S46PU	195	CAS [1]# / WE [1]#
128	FP [12]	162	MVDD2	196	MD [8]
129	FP [13]	163	MD [20]	197	SW0 / **MCLK** / **XMCL K**
130	FP [14]	164*	MD [19] / XCLKPU	198	VSS11
131	FP [15]	165*	MD [18] / FVLPU	199	MAVDD
132	FPVDD1	166	MD [17] / ISAPU	200	MFILTER
133	FP [16] / FCP [2]	167*	MD [16] / PCIPU	201	MAVSS
134	FP [17] / FCP [3]	168	VSS9	202	MD [7]
135	FP [18]	169	CAS [3]# / WE [3]#	203	MD [6]
136	FP [19]	170	CAS [2]# / WE [2]#	204	MD [5]
137	FP [20]	171	MA [9]	205	MVDD1
138	FP [21]	172	MA [8]	206	MD [4]
139	FP [22]	173	MA [7]	207	MD [3]
140	FP [23]	174	MA [6]	208	MD [2]
141	FCP [4]	175	MA [5]		
142	FCP [5]	176	MA [4]		

NOTES:

1) Pins numbers with an asterisk (*) have pull-up options, discussed in Section 2.7, "Configuration Input Pins ".

2) Pin names in bold print apply only to the CL-GD7541.

Table 1-2 lists the CL-GD7541/GD7543 pins that connect through a DB-44 connector to corresponding pins of LCD flat panels. In Table 1-2, the following abbreviations are used:

- (O) indicates pin type is an output function

Table 1-2. CL-GD7541/GD7543 Interface Pins to LCD Flat Panels

CL-GD7541/GD7543			DB-44 Connector	LCD Flat Panel Type – Corresponding Pins						
Pin No.	Pin Name	Pin Type	Pin No.	TFT LCD Types				STN LCD Types		
								Color		Mono (Dual-Scan)
				24-Bit	18-Bit	12-Bit	9-Bit	16-Bit	8-Bit	Bits
140	FP[23]	O	13	R[7]	R[5]	R[3:]	R[2]	SUD[3]	—	—
139	FP[22]	O	14	R[6]	R[4]	R[2]	R[1]	SUD[2]	—	—
138	FP[21]	O	15	R[5]	R[3]	R[1]	R[0]	SUD[1]	—	—
137	FP[20]	O	16	R[4]	R[2]	R[0]	—	SUD[0]	—	—
136	FP[19]	O	9	R[3]	R[1]	—	—	SUD[7]	—	—
135	FP[18]	O	10	R[2]	R[0]	—	—	SUD[6]	—	—
134	FP[17]	O	44	R[1]	—	—	—	—	—	—
133	FP[16]	O	42	R[0]	—	—	—	—	—	—
131	FP[15]	O	8	G[7]	G[5]	G[3]	G[2]	SLD[7]	SUD[3]	UD[3]
130	FP[14]	O	7	G[6]	G[4]	G[2]	G[1]	SLD[6]	SUD[2]	UD[2]
129	FP[13]	O	6	G[5]	G[3]	G[1]	G[0]	SLD[5]	SUD[1]	UD[1]
128	FP[12]	O	5	G[4]	G[2]	G[0]	—	SLD[4]	SUD[0]	UD[0]
127	FP[11]	O	11	G[3]	G[1]	—	—	SUD[5]	—	—
126	FP[10]	O	12	G[2]	G[0]	—	—	SUD[4]	—	—
125	FP[9]	O	20	G[1]	—	—	—	—	—	—
123	FP[8]	O	29	G[0]	—	—	—	—	—	—
122	FP[7]	O	4	B[7]	B[5]	B[3]	B[2]	SLD[3]	SLD[3]	LD[3]
120	FP[6]	O	3	B[6]	B[4]	B[2]	B[1]	SLD[2]	SLD[2]	LD[2]
119	FP[5]	O	2	B[5]	B[3]	B[1]	B[0]	SLD[1]	SLD[1]	LD[1]
118	FP[4]	O	1	B[4]	B[2]	B[0]	—	SLD[0]	SLD[0]	LD[0]
117	FP[3] / MOD	O	23	B[3]	B[1]	—	—	MOD	MOD	MOD
116	FP[2]	O	39	B[2]	B[0]	—	—	—	—	—
115	FP[1]	O	43	B[1]	—	—	—	—	—	—
114	FP[0]	O	24	B[0]	—	—	—	—	—	—
113	FPVDCLK	O	18	FPVDCLK				SCLK	SCLK	CP2
112	LLCLK	O	35	LLCLK				LP	LP	CP1
110	LFS	O	22	LFS				FLM	FLM	S
108	FPDE	O	26	FPDE				—	—	—

NOTE: Pin numbers and names for specific LCDs are given in the "Panel Interface Guide" in the *CL-GD754X Application Book*.

Table 1-3 lists the power connections for the CL-GD7541/GD7543 interface pin groups. For design flexibility and to minimize overall power consumption, each of the CL-GD7541/GD7543 interface pin groups listed below may receive either +3.3 or 5 V from independent sources.

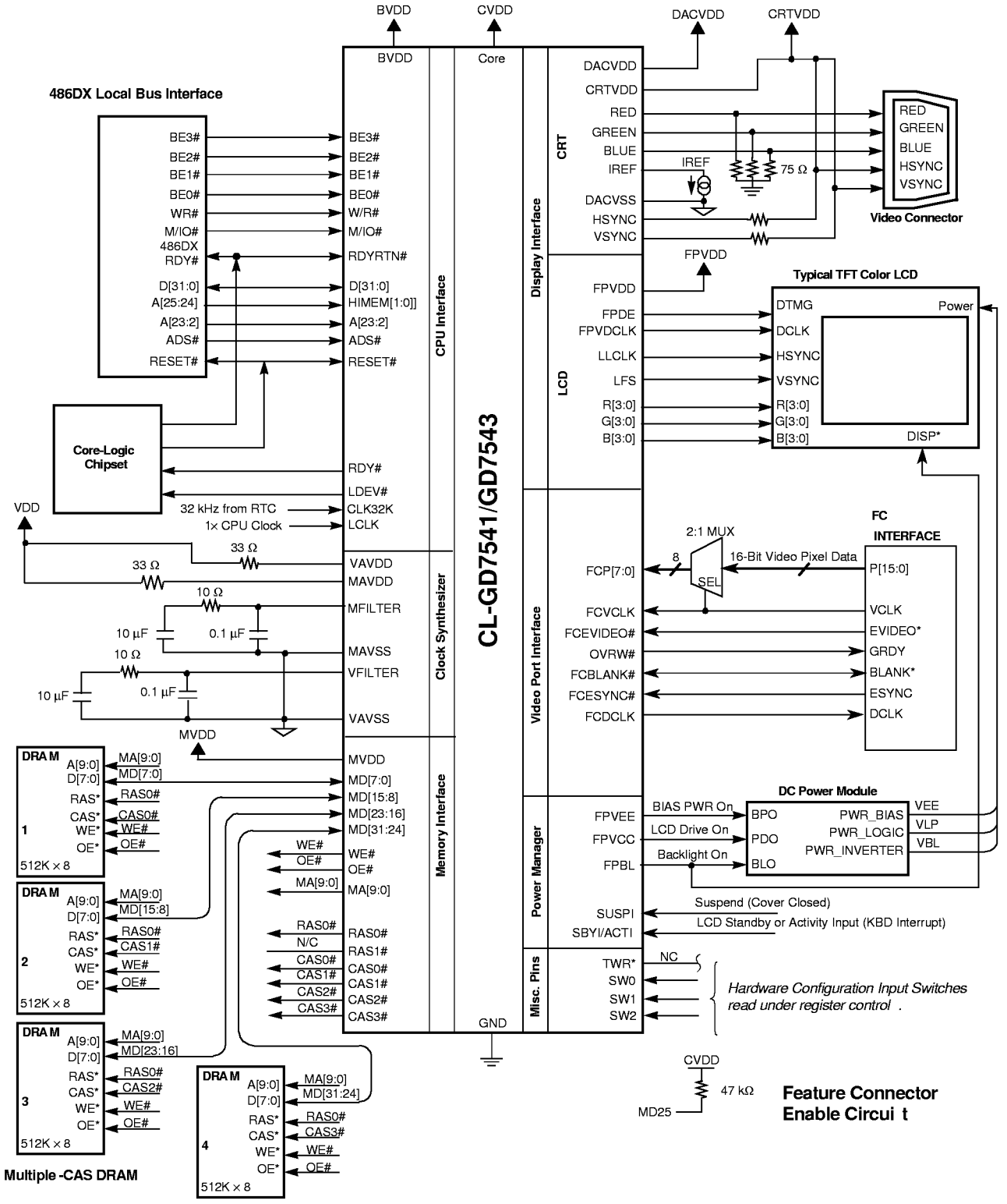
NOTE: Pins that have asterisks must all be set to the same voltage level .

Table 1-3. Power Connections for Interface Pin Groups

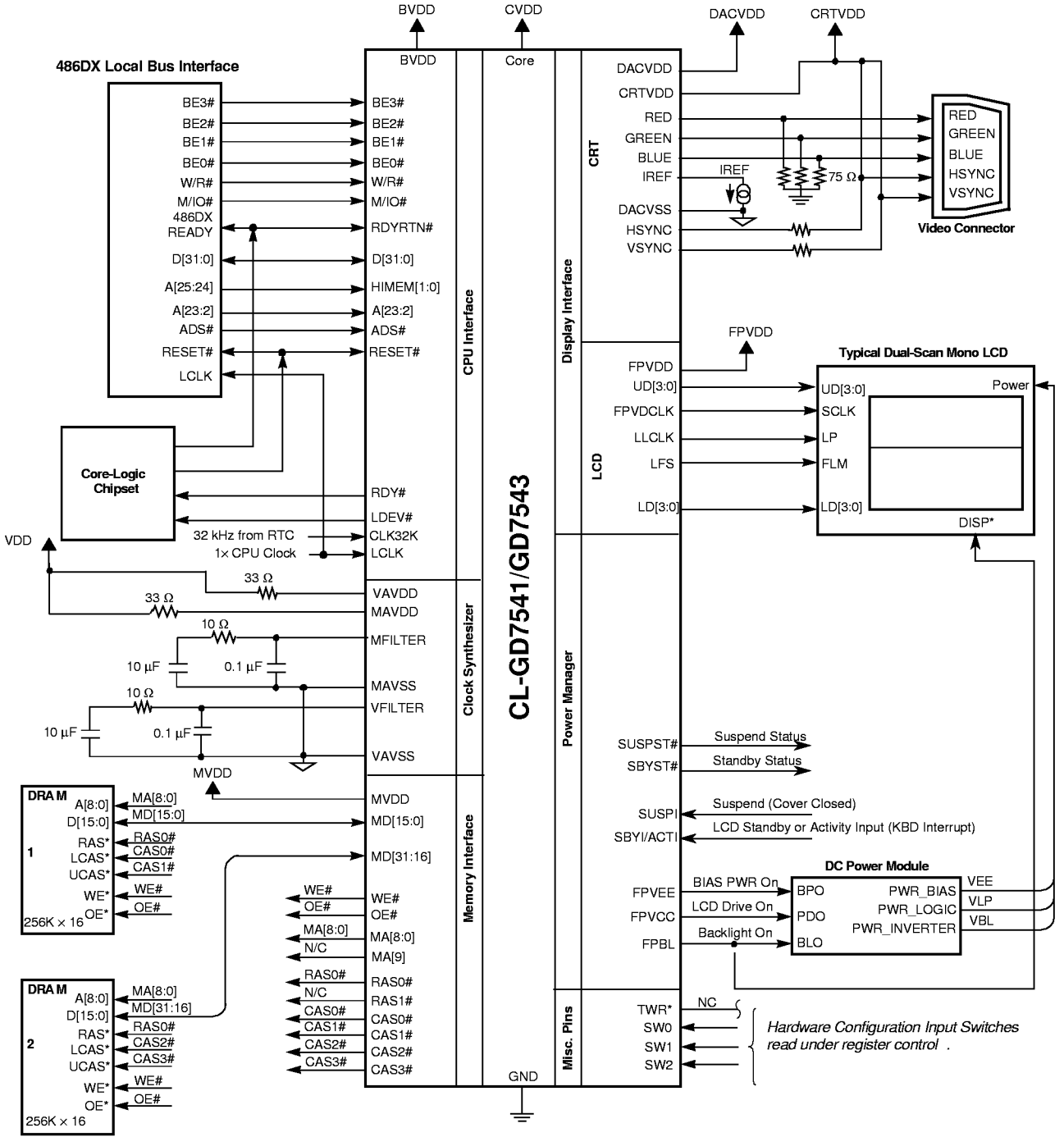
Name of Interface Pin Group	Power Pin to Interface Pin Group		CL-GD7541/GD7543 Pins in Interface Pin Group
	Power Pin Name	Power Pin Number	
Clock Frequency Synthesizer:			
MCLK (Memory Clock) Frequency Synthesizer	MAVDD*	199	82, 85, 89, 197, 199–201
VCLK (Video Clock) Frequency Synthesizer	VAVDD*	84	83, 84, 85
Core Logic	CVDD1*	36	6, 36, 42, 52, 62, 67, 80, 100, 104, 121, 145, 149, 150, 168, 185, 192, 198
	CVDD2*	62	
	CVDD3*	121	
	CVDD4*	192	
CPU Host Bus	BVDD1	47	3–5, 7–35, 37–41, 43–46, 51, 53–61, 63–66, 68–79, 81
	BVDD2	73	
CRT	CRTVDD	92	88, 91–99, 111, 146
CRT: NTSC (and PAL)	CRTVDD	92	94–98, 146
Digital-to-Analog (RAMDAC)	DACVDD1*	109	90, 109
	DACVDD2*	90	
LCD	FPVDD1	107	86, 87, 101–103, 105–108, 110, 112–120, 122–144, 147, 148
	FPVDD2	132	
Video Memory	MVDD1	162	1, 2, 151–167, 169, 170–184, 186–191, 193–196, 202–208
	MVDD2	205	

1.3 Block Diagrams: CL-GD7541/GD754 3 Interface s

1.3.1 Local Bus (32-Bit '486DX or VES A® VL-Bu s™), 2-Mbyte 512K × 8 DRAM, 12-Bit TFT Color, Video Por t

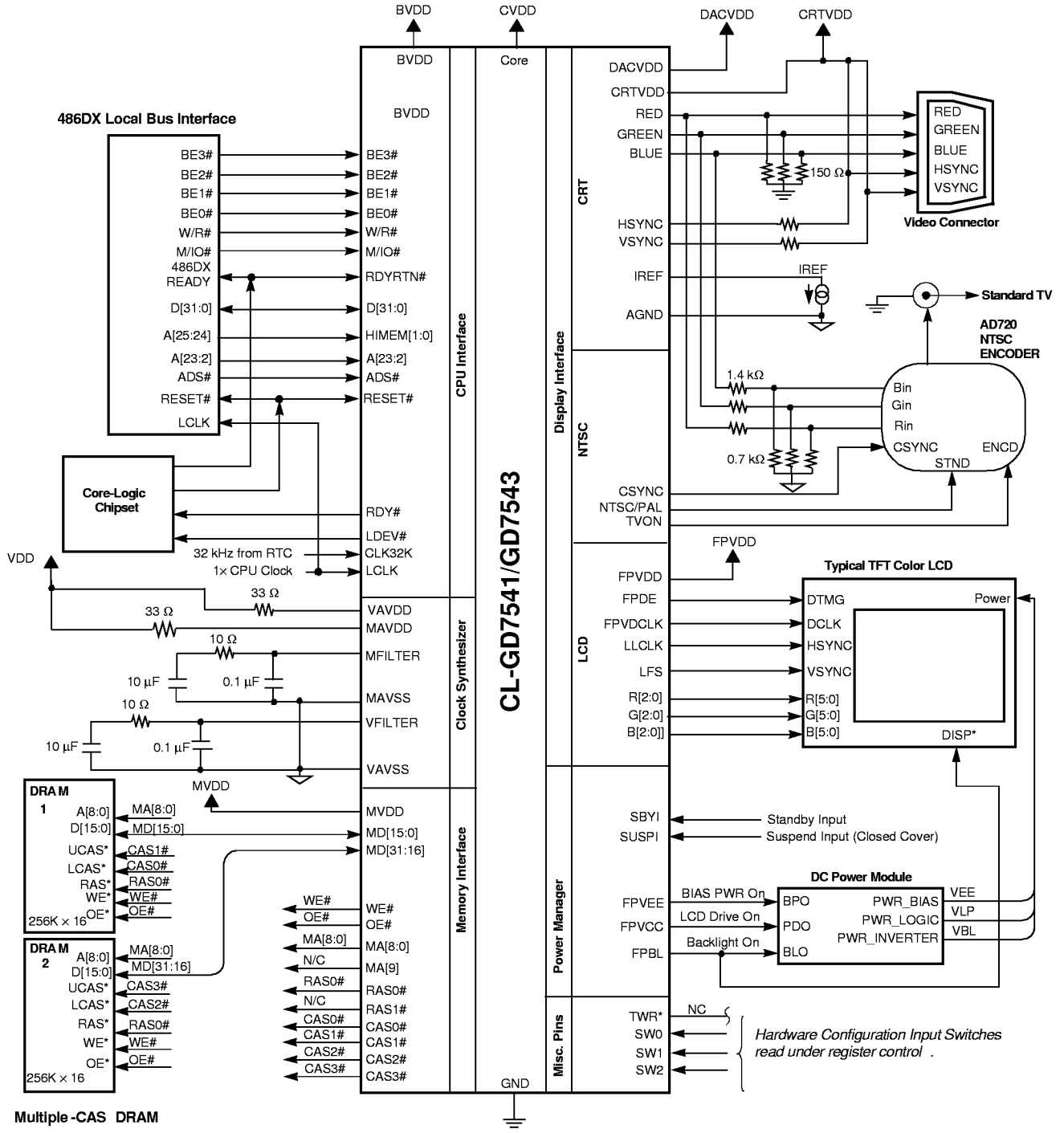


1.3.2 Local Bus (32-Bit '486DX or VESA® VL-Bus™), 1-Mbyte 256K × 16 DRAM, 8-Bit Dual-Scan Monochrome



Multiple-CAS DRAM

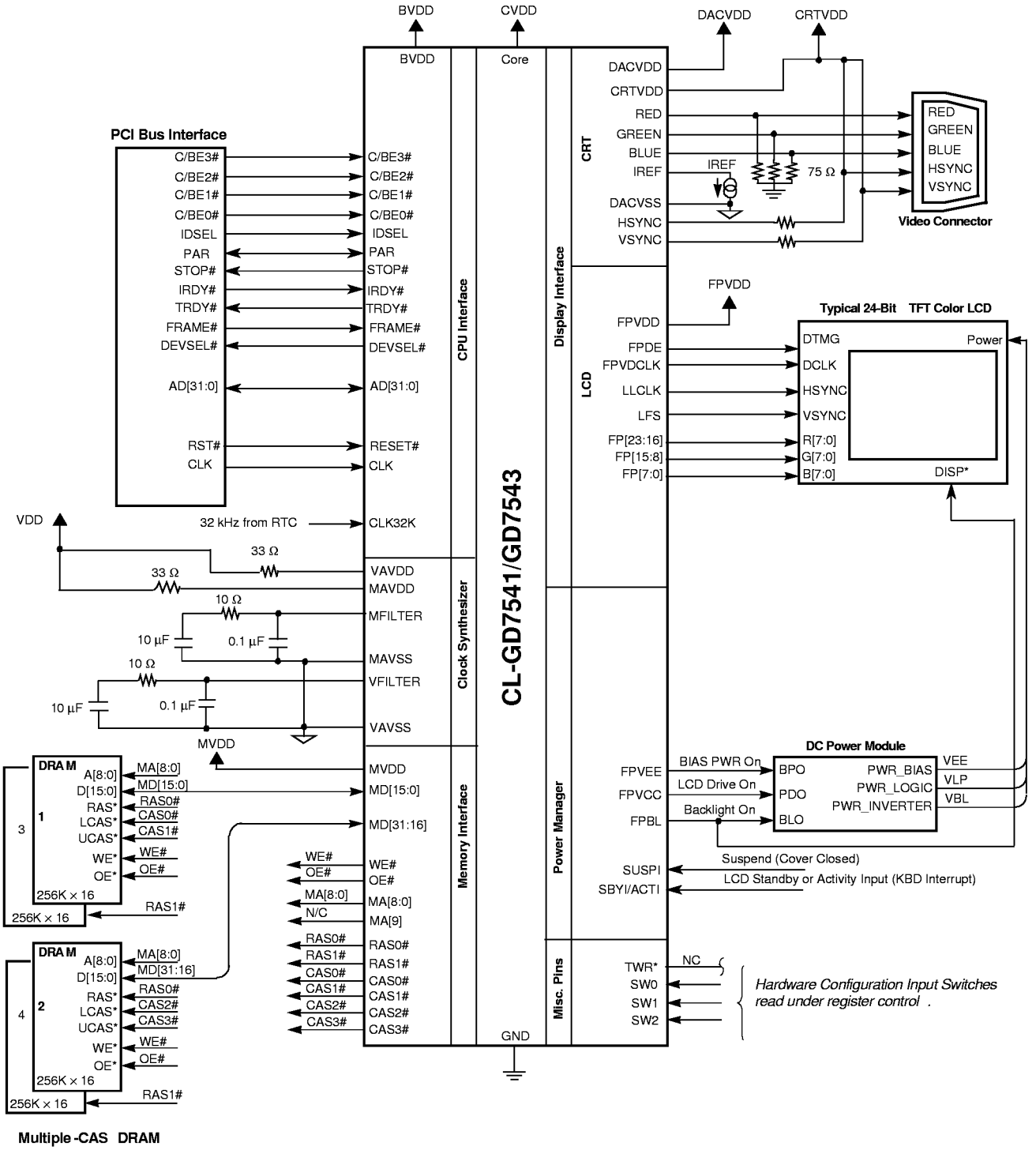
1.3.3 Local Bus (32-Bit '486DX or VES A® VL-Bus™), 1-Mbyte 256K × 16 DRAM, 18-Bit TFT Color, NTSC Outpu t



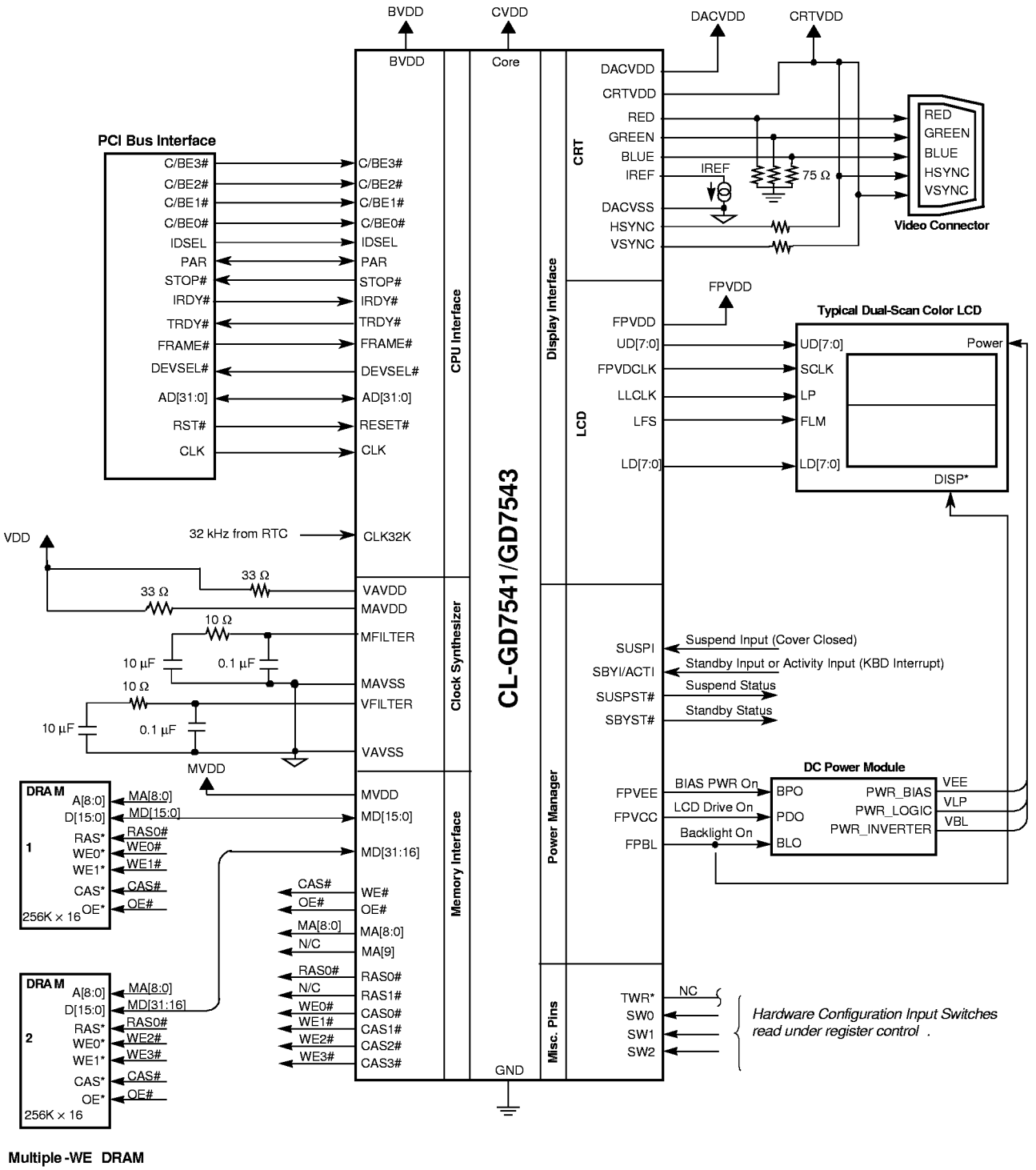
NOTE: When using the design featured in this diagram, the CRT must be disconnected when using the NTSC output .

This diagram illustrates general signal connections. All information is preliminary and subject to change. For detailed design examples, refer to the *CL-GD754X Application Boo k*.

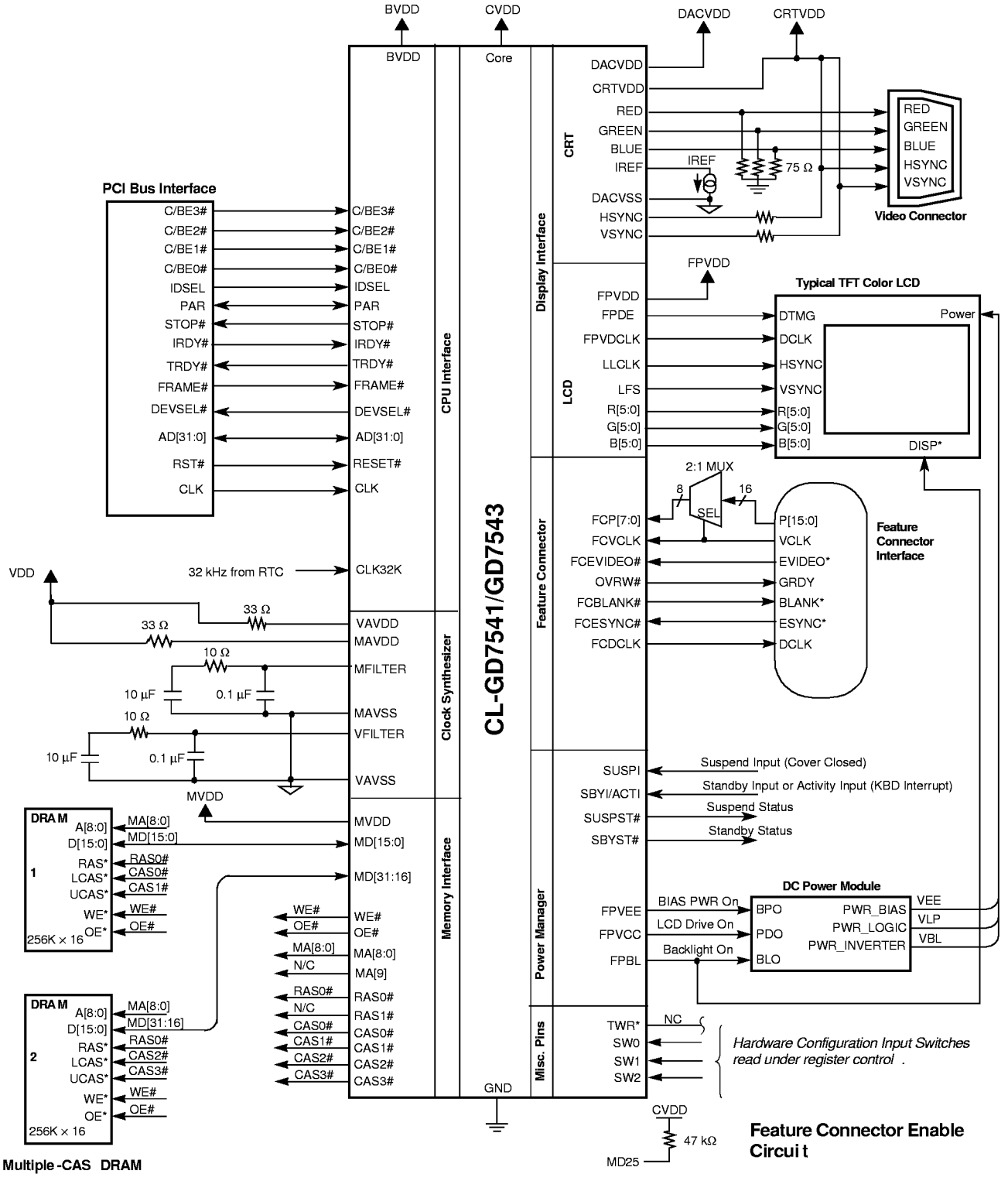
1.3.4 PCI Bus, 2-Mbyte 256K × 16 DRAM, 24-Bit TFT Color



1.3.5 PCI Bus, 1-Mbyte 256K × 16 DRAM, 16-Bit Dual-Scan Color



1.3.6 PCI Bus, 1-Mbyte 256K × 16 DRAM, 18-Bit TFT Color, Feature Connector Interface



2. PIN DESCRIPTIONS

The following abbreviations are used for pin types in the following sections:

- (I) indicates input function
- (O) indicates output function
- (I/O) indicates a bidirectional function
- (I or O) indicates either an input or output function, depending on the mode
- (O-OD) indicates open-drain output (electrically equivalent to open-collector)
- (O-TS) indicates tristate output
- (#) indicates active-low function

2.1 CPU Host Bus Interface Pins

As explained in this section, a number of CL-GD7541/GD7543 pins that interface to the CPU host bus pins are defined according to the type of CPU host to which the CL-GD7541/GD7543 is connected.

2.1.1 CL-GD7541/GD7543 CPU Host Bus Interface Pins to '486 or VESA® VL-Bus™ Local Bus

Pin Name	Pin No.	Type	Pin Description
A[23:2]	39:37 35:17	I	**ADDRESS [23:2] :** These inputs are used to select the resource to be accessed during memory or I/O operations.
ADS#	9	I	**ADDRESS DATA STROBE# :** This active-low input indicates that a new cycle has begun. The ADS# signal is generated from a decode of the CPU output signals, A[23:2] and M/IO#. This output goes low before the middle of the first timing (T2) cycle after ADS# goes low. When connecting the CL-GD7541/GD7543 to a '486 local bus, this pin must be connected directly to the '486 local bus ADS# pin.
BE[3:0]#	13:16	I	**BYTE ENABLE [3:0]# :** These active-low inputs are connected directly to the corresponding CPU byte-enable output.
D[31:0]	43:46 48:51 53:61 63:66 68:72 74:79	I/O	**DATA [31:0]:** These bidirectional pins are used to transfer data during any memory or I/O operation. When connecting the CL-GD7541/GD7543 to a local bus (either a '486 local bus or a VESA VL-Bus), these pins must be connected directly to the local bus D[31:0] pins.
HIMEM[1:0] / A[25:24]	41,40	I	**HIGH MEMORY [1:0]:** These active-high inputs are a decode of the upper CPU Address bits. Normally, these inputs are used as CPU Address bits A[25:24]. However, in conjunction with Extension registers SR7 and SR2D, they can be used as CPU Address bits A[31:30] in order to leave 2 Gbytes of upper address space for MPEG (Moving Picture Experts Group) and JPEG (Joint Picture Expert Group) boards.
INTR	5	O-TS	**INTERRUPT REQUEST :** This active-high output indicates that the CL-GD7541/GD7543 has reached the end of an active field. Specifically, the transition occurs at the beginning of the bottom border. For a description of controls for this pin, refer to CRT Controller register CR11[3:0].

2.1.1 CL-GD7541/GD7543 CPU Host Bus Interface Pins to '486 or VESA® VL-Bus™ Local Bus *(cont.)*

Pin Name	Pin No.	Type	Pin Description
LCLK	7	I	**LOCAL BUS CLOCK:** This active-low input is the timing reference when the CL-GD7541/GD7543 is connected to a local bus. When connecting the CL-GD7541/GD7543 to a '486 local bus, this pin must be connected directly to the '486 local bus CLK1X# pin. If no CLK1X is available from the '486, CLK2 must be divided by two and connected to the CL-GD7541/GD7543 LCLK pin, and clock skew must be less than 2.0 ns. When connecting the CL-GD7541/GD7543 to a VESA VL-Bus, this pin must be connected directly to the VESA VL-Bus LCLK pin.
LDEV#	3	O-OD	**LOCAL BUS DEVICE#:** This open-drain (open-collector) output is driven low to indicate that the CL-GD7541/GD7543 is responding to the current cycle. When connecting the CL-GD7541/GD7543 to a VESA VL-Bus, this pin is connected to the VESA VL-Bus LDEV# pin.
M/IO#	11	I	**MEMORY I/O#:** This input indicates whether a memory or I/O operation is to occur. This pin *must* be connected directly to the M/IO# pin on the CPU. When M/IO# is high, a memory operation is selected. When M/IO is low, an I/O operation is selected.
RDY#	4	O-TS	**READY#:** This active-low signal is used as an output to terminate a CL-GD7541/GD7543 bus cycle. When connecting the CL-GD7541/GD7543 to a '486 local bus, this pin must be connected to the '486 local bus RDY# pin. When connecting the CL-GD7541/GD7543 to a VESA VL-Bus, this pin must be connected to the VESA VL-Bus LRDY# pin.

2.1.1 CL-GD7541/GD754 3 CPU Host Bus Interface Pins to '486 or VESA® VL-Bus™ Local Bus *(cont.)*

Pin Name	Pin No.	Type	Pin Description
RDYRTN#	8	I	**READY RETURN# :** This input establishes a handshake between the CL-GD7541/GD7543 and a local bus so that the CL-GD7541/GD7543 is informed when the cycle has ended. RDYRTN# typically goes low in the same LCLK cycle that LRDY# goes low. When LCLK is higher than 33 MHz, RDYRTN# may trail LRDY# by one LCLK cycle. During DMA or system I/O bus master operations, RDYRTN# goes low for one LCLK cycle when the DMA or system I/O bus masters command ends. When connecting the CL-GD7541/GD7543 to a '486 local bus, this pin must be connected to the '486 local bus RDY# pin. When connecting the CL-GD7541/GD7543 to a VESA VL-Bus, this pin must be connected to the VESA VL-Bus RDYRTN# pin.
RESET#	12	I	**RESET# :** This input, when low, initializes the CL-GD7541/GD7543 to a known state. The trailing (rising) edge of this input loads the configuration registers SR22[7:0] and SR24[7] with the data on MD[25:16] pins. The data on the MD[25:16] pins is determined either by internal pull-down resistors or optional external pull-up resistors. When RESET# is low, it forces all outputs to a high-impedance state, and it initializes all registers to their system reset state.
SLEEP#	81	I	**SLEEP# :** This active-low input is used by the external hardware to put the CL-GD7541/GD7543 into bus Sleep mode. When this input is low, the memory and I/O interfaces are disabled. Once this pin is low, no other chip access is possible until this pin goes high.
W/R#	10	I	**WRITE/READ# :** This input indicates whether a write or read operation is selected by the CPU. This pin *must* be connected directly to the W/R# pin on the CPU. When W/R# is high, a write occurs. When W/R# is low, a read occurs.

2.1.2 CL-GD7541/GD754 3 CPU Host Bus Interface Pins to PCI Bus

Pin Name	Pin No.	Type	Pin Description
AD[31:0]	43:46 48:51 53:61 63:66 68:72 74:79	I/O	**ADDRESS AND DATA [31:0]:** These multiplexed, bidirectional pins are used to transfer system address and data during any memory or I/O operation on the PCI bus. During the first clock of a transaction, these pins contain a 32-bit physical byte address. During subsequent clocks, they contain data. These pins directly connect to the PCI Bus AD[31:0] pins.
C/BE[3:0]#	13:16	I or O	**COMMAND AND BYTE ENABLE [3:0]# :** These multiplexed pins are used to transfer Bus Command and Byte Enables during any memory or I/O operation on the PCI bus. During the address phase of the operation, these pins define the bus command (refer to Table 2-1). During the data phase, these pins are used as Byte Enable outputs. C/BE0# applies to byte 0. C/BE3# applies to byte 3. These pins directly connect to the PCI Bus C/BE[3:0]# pins.

Table 2-1. Command and Byte Enable #

C/BE#				Command Type	Comments
[3]	[2]	[1]	[0]		
0	0	0	0	Interrupt Acknowledge	–
0	0	0	1	Special Cycle	–
0	0	1	0	I/O Read	Valid
0	0	1	1	I/O Write	Valid
0	1	0	0	Reserved	–
0	1	0	1	Reserved	–
0	1	1	0	Memory Read	Valid
0	1	1	1	Memory Write	Valid
1	0	0	0	Reserved	–
1	0	0	1	Reserved	–
1	0	1	0	Configuration Read	Valid
1	0	1	1	Configuration Write	Valid
1	1	0	0	Memory Read Multiple	–
1	1	0	1	Dual Address Cycle	–
1	1	1	0	Memory Read Line	–
1	1	1	1	Memory Write and Invalidate	–

2.1.2 CL-GD7541/GD754 3 CPU Host Bus Interface Pins to PCI Bus *(cont.)*

Pin Name	Pin No.	Type	Pin Description
CLK	7	I	**CLOCK :** This pin is the timing reference for the CL-GD7541/GD7543, when it is connected to a PCI bus. This pin must be connected directly to the PCI bus CLK pin.
DEVSEL#	3	O-OD	**DEVICE SELECT# :** This open-drain (open-collector) output is driven low to indicate that the CL-GD7541/GD7543 is responding to the current cycle.
FRAME#	9	I	**FRAME# :** This active-low input indicates the beginning and duration of an access. FRAME# goes low to indicate the beginning of a bus transaction. While FRAME# is low, data transfers continue. The transaction is in its final data phase when FRAME# goes high.
IDSEL	10	I	**INITIALIZATION DEVICE SELECT# :** This active-high input signal is used as a chip select in lieu of the upper 24 address lines during configuration read and write cycles.
INTR#	5	O-TS	**INTERRUPT REQUEST# :** This active-low output, controlled by CRT Controller register CR11[3:0], indicates the CL-GD7541/GD7543 has reached the end of an active field. Specifically, the transition occurs at the beginning of the bottom border.
IRDY#	8	I	**INITIATOR READY# :** This active-low input establishes a handshake between the CL-GD7541/GD7543 and PCI bus, so that the CL-GD7541/GD7543 can detect when the cycle has ended. Wait states are inserted until both IRDY# and TRDY# are low.
PAR	23	O-TS	**PARITY :** This signal provides even parity across AD[31:0] and C/BE[3:0]#. The CL-GD7541/GD7543 samples this signal during write cycles and transmits the correct parity for read cycles.
RST#	12	I	**RESET#:** When low this input initializes the CL-GD7541/GD7543 to a known state. The trailing (rising) edge of this input loads the configuration registers SR22[7:0] and SR24[7] with the data on MD[25:16], which is determined by internal pull-down resistors or optional external pull-up resistors.
STOP#	22	O-TS	**STOP# :** This active-low output indicates a current request to the PCI bus master to stop the current transaction.
TRDY#	4	O-TS	**TARGET READY# :** This active-low signal is used as an output to terminate a CL-GD7541/GD7543 bus cycle.

2.2 LCD Interface Pins

The LCD interface is determined by the type of LCD used. For specific connection information, refer to the Cirrus Logic "Panel Interface Guide" in the *CL-GD754X Application Book*.

Pin Name	Pin No.	Pin Type	Pin Function	Pin Description
FP[0]	114	O	B0	**24-BIT TFT BLUE BIT [0]:** This bit is BLUE Color Data bit 0 (LSB) for 24-bit TFT color LCDs.
FP[1]	115	O	B1	**24-BIT TFT BLUE BIT [1]:** This bit is BLUE Color Data bit 1 for 24-bit TFT color LCDs.
FP[2]	116	O	B2	**24-BIT TFT BLUE BIT [2]:** This bit is BLUE Color Data bit 2 for 24-bit TFT color LCDs.
			B0	**18-BIT TFT BLUE BIT [0]:** This bit is BLUE Color Data bit 0 (LSB) for 18-bit TFT color LCDs.
FP[3]	117	O	B3	**24-BIT TFT BLUE BIT [3]:** This bit is BLUE Color Data bit 3 for 24-bit TFT color LCDs.
			B1	**18-BIT TFT BLUE BIT [1]:** This bit is BLUE Color Data bit 1 for 18-bit TFT color LCDs.
FP[4]	118	O	B4	**24-BIT TFT BLUE BIT [4]:** This bit is BLUE Color Data bit 4 for 24-bit TFT color LCDs.
			B2	**18-BIT TFT BLUE BIT [2]:** This bit is BLUE Color Data bit 2 for 18-bit TFT color LCDs.
			B0	**12-BIT TFT BLUE BIT [0]:** This bit is BLUE Color Data bit 0 (LSB) for 12-bit TFT color LCDs.
			SLD0	**16-BIT STN COLOR LOWER BIT [0]:** This bit is Lower Data bit 0 (LSB) for 16-bit dual- and single-scan STN color LCDs.
			SLD0	**8-BIT STN COLOR LOWER BIT [0]:** This bit is Lower Data bit 0 (LSB) for 8-bit dual- and single-scan STN color LCDs.
			LD0	**LOWER DATA [0]:** This bit is Lower Panel Data bit 0 (LSB) for dual-scan STN monochrome LCDs.

2.2 LCD Interface Pins *(cont.)*

Pin Name	Pin No.	Pin Type	Pin Function	Pin Description
FP[5]	119	O	B5	**24-BIT TFT BLUE BIT [5]:** This bit is BLUE Color Data bit 5 for 24-bit TFT color LCDs.
			B3	**18-BIT TFT BLUE BIT [3]:** This bit is BLUE Color Data bit 3 for 18-bit TFT color LCDs.
			B1	**12-BIT TFT BLUE BIT [1]:** This bit is BLUE Color Data bit 1 for 12-bit TFT color LCDs.
			B0	**9-BIT TFT BLUE BIT [0]:** This bit is BLUE Color Data bit 0 (LSB) for 9-bit TFT color LCDs.
			SLD1	**16-BIT STN COLOR LOWER BIT [1]:** This bit is Lower Data bit 1 for 16-bit dual- and single-scan STN color LCDs.
			SLD1	**8-BIT STN COLOR LOWER BIT [1]:** This bit is Lower Data bit 1 for 8-bit dual- and single-scan STN color LCDs.
			LD1	**LOWER DATA [1]:** This bit is Lower Panel Data bit 1 for dual-scan STN monochrome LCDs.
FP[6]	120	O	B6	**24-BIT TFT BLUE BIT [6]:** This bit is BLUE Color Data bit 6 for 24-bit TFT color LCDs.
			B4	**18-BIT TFT BLUE BIT [4]:** This bit is BLUE Color Data bit 4 for 18-bit TFT color LCDs.
			B2	**12-BIT TFT BLUE BIT [2]:** This bit is BLUE Color Data bit 2 for 12-bit TFT color LCDs.
			B1	**9-BIT TFT BLUE BIT [1]:** This bit is BLUE Color Data bit 1 for 9-bit TFT color LCDs.
			SLD2	**16-BIT STN COLOR LOWER BIT [2]:** This bit is Lower Data bit 2 for 16-bit dual- and single-scan STN color LCDs.
			SLD2	**8-BIT STN COLOR LOWER BIT [2]:** This bit is Lower Data bit 2 for 8-bit dual- and single-scan STN color LCDs.
			LD2	**LOWER DATA [2]:** This bit is Lower Panel Data bit 2 for dual-scan STN monochrome LCDs.

2.2 LCD Interface Pins *(cont.)*

Pin Name	Pin No.	Pin Type	Pin Function	Pin Description
FP[7]	122	O	B7	**24-BIT TFT BLUE BIT [7]:** This bit is BLUE Color Data bit 7 (MSB) for 24-bit TFT color LCDs.
			B5	**18-BIT TFT BLUE BIT [5]:** This bit is BLUE Color Data bit 5 (MSB) for 18-bit TFT color LCDs.
			B3	**12-BIT TFT BLUE BIT [3]:** This bit is BLUE Color Data bit 3 (MSB) for 12-bit TFT color LCDs.
			B2	**9-BIT TFT BLUE BIT [2]:** This bit is BLUE Color Data bit 2 (MSB) for 9-bit TFT color LCDs.
			SLD3	**16-BIT STN COLOR LOWER BIT [3]:** This bit is Lower Data bit 3 for 16-bit dual- and single-scan STN color LCDs.
			SLD3	**8-BIT STN COLOR LOWER BIT [3]:** This bit is Lower Data bit 3 (MSB) for 8-bit dual- and single-scan STN color LCDs.
			LD3	**LOWER DATA [3]:** This bit is Lower Panel Data bit 3 (MSB) for dual-scan STN monochrome LCDs.
FP[8]	123	O	G0	**24-BIT TFT GREEN BIT [0]:** This bit is GREEN Color Data bit 0 (LSB) for 24-bit TFT color LCDs.
FP[9]	125	O	G1	**24-BIT TFT GREEN BIT [1]:** This bit is GREEN Color Data bit 1 for 24-bit TFT color LCDs.
FP[10]	126	O	G2	**24-BIT TFT GREEN BIT [2]:** This bit is GREEN Color Data bit 2 for 24-bit TFT color LCDs.
			G0	**18-BIT TFT GREEN BIT [0]:** This bit is GREEN Color Data bit 0 (LSB) for 18-bit TFT color LCDs.
			SUD4	**16-BIT STN COLOR UPPER BIT [4]:** This bit is Upper Data bit 4 for 16-bit dual- and single-scan STN color LCDs.
FP[11]	127	O	G3	**24-BIT TFT GREEN BIT [3]:** This bit is GREEN Color Data bit 3 for 24-bit TFT color LCDs.
			G1	**18-BIT TFT GREEN BIT [1]:** This bit is GREEN Color Data bit 1 for 18-bit TFT color LCDs.
			SUD5	**16-BIT STN COLOR UPPER BIT [5]:** This bit is Upper Data bit 5 for 16-bit dual- and single-scan STN color LCDs.

2.2 LCD Interface Pins *(cont.)*

Pin Name	Pin No.	Pin Type	Pin Function	Pin Description
FP[12]	128	O	G4	**24-BIT TFT GREEN BIT [4]:** This bit is GREEN Color Data bit 4 for 24-bit TFT color LCDs.
			G2	**18-BIT TFT GREEN BIT [2]:** This bit is GREEN Color Data bit 2 for 18-bit TFT color LCDs.
			G0	**12-BIT TFT GREEN BIT [0]:** This bit is GREEN Color Data bit 0 (LSB) for 12-bit TFT color LCDs.
			SLD4	**16-BIT STN COLOR LOWER BIT [4]:** This bit is Lower Data bit 4 for 16-bit dual- and single-scan STN color LCDs.
			SUD0	**8-BIT STN COLOR UPPER BIT [0]:** This bit is Upper Data bit 0 (LSB) for 8-bit dual- and single-scan STN color LCDs.
			UD0	**UPPER DATA [0]:** This bit is Upper Panel Data bit 0 (LSB) for dual-scan STN monochrome LCDs.
FP[13]	129	O	G5	**24-BIT TFT GREEN BIT [5]:** This bit is GREEN Color Data bit 5 for 24-bit TFT color LCDs.
			G3	**18-BIT TFT GREEN BIT [3]:** This bit is GREEN Color Data bit 3 for 18-bit TFT color LCDs.
			G1	**12-BIT TFT GREEN BIT [1]:** This bit is GREEN Color Data bit 1 for 12-bit TFT color LCDs.
			G0	**9-BIT TFT GREEN BIT [0]:** This bit is GREEN Color Data bit 0 (LSB) for 9-bit TFT color LCDs.
			SLD5	**16-BIT STN COLOR LOWER BIT [5]:** This bit is Lower Data bit 5 for 16-bit dual- and single-scan STN color LCDs.
			SUD1	**8-BIT STN COLOR UPPER BIT [1]:** This bit is Upper Data bit 1 for 8-bit dual- and single-scan STN color LCDs.
			UD1	**UPPER DATA [1]:** This bit is Upper Panel Data bit 1 for dual-scan STN monochrome LCDs.

2.2 LCD Interface Pins *(cont.)*

Pin Name	Pin No.	Pin Type	Pin Function	Pin Description
FP[14]	130	O	G6	**24-BIT TFT GREEN BIT [6]:** This bit is GREEN Color Data bit 6 for 24-bit TFT color LCDs.
			G4	**18-BIT TFT GREEN BIT [4]:** This bit is GREEN Color Data bit 4 for 18-bit TFT color LCDs.
			G2	**12-BIT TFT GREEN BIT [2]:** This bit is GREEN Color Data bit 2 for 12-bit TFT color LCDs.
			G1	**9-BIT TFT GREEN BIT [1]:** This bit is GREEN Color Data bit 1 for 9-bit TFT color LCDs.
			SLD6	**16-BIT STN COLOR LOWER BIT [6]:** This bit is Lower Data bit 6 for 16-bit dual- and single-scan STN color LCDs.
			SUD2	**8-BIT STN COLOR UPPER BIT [2]:** This bit is Upper Data bit 2 for 8-bit dual- and single-scan STN color LCDs.
			UD2	**UPPER DATA [2]:** This bit is Upper Panel Data bit 2 for dual-scan STN monochrome LCDs.
FP[15]	131	O	G7	**24-BIT TFT GREEN BIT [7]:** This bit is GREEN Color Data bit 7 (MSB) for 24-bit TFT color LCDs.
			G5	**18-BIT TFT GREEN BIT [5]:** This bit is GREEN Color Data bit 5 (MSB) for 18-bit TFT color LCDs.
			G3	**12-BIT TFT GREEN BIT [3]:** This bit is GREEN Color Data bit 3 (MSB) for 12-bit TFT color LCDs.
			G2	**9-BIT TFT GREEN BIT [2]:** This bit is GREEN Color Data bit 2 (MSB) for 9-bit TFT color LCDs.
			SLD7	**16-BIT STN COLOR LOWER BIT [7]:** This bit is Lower Data bit 7 (MSB) for 16-bit dual- and single-scan STN color LCDs.
			SUD3	**8-BIT STN COLOR UPPER BIT [3]:** This bit is Upper Data bit 3 (MSB) for 8-bit dual- and single-scan STN color LCDs.
			UD3	**UPPER DATA [3]:** This bit is Upper Panel Data bit 3 (MSB) for dual-scan STN monochrome LCDs.
FP[16]	133	O	R0	**24-BIT TFT RED BIT [0]:** This bit is RED Color Data bit 0 (LSB) for 24-bit TFT color LCDs.
FP[17]	134	O	R1	**24-BIT TFT RED BIT [1]:** This bit is RED Color Data bit 1 for 24-bit TFT color LCDs.

2.2 LCD Interface Pins *(cont.)*

Pin Name	Pin No.	Pin Type	Pin Function	Pin Description
FP[18]	135	O	R2	**24-BIT TFT RED BIT [2]:** This bit is RED Color Data bit 2 for 24-bit TFT color LCDs.
			R0	**18-BIT TFT RED BIT [0]:** This bit is RED Color Data bit 0 (LSB) for 18-bit TFT color LCDs.
			SUD6	**16-BIT STN COLOR UPPER BIT [6]:** This bit is Upper Data bit 6 for 16-bit dual- and single-scan STN color LCDs.
FP[19]	136	O	R3	**24-BIT TFT RED BIT [3]:** This bit is RED Color Data bit 3 for 24-bit TFT color LCDs.
			R1	**18-BIT TFT RED BIT [1]:** This bit is RED Color Data bit 1 for 18-bit TFT color LCDs.
			SUD7	**16-BIT STN COLOR UPPER BIT [7]:** This bit is Upper Data bit 7 (MSB) for 16-bit dual- and single-scan STN color LCDs.
FP[20]	137	O	R4	**24-BIT TFT RED BIT [4]:** This bit is RED Color Data bit 4 for 24-bit TFT color LCDs.
			R2	**18-BIT TFT RED BIT [2]:** This bit is RED Color Data bit 2 for 18-bit TFT color LCDs.
			R0	**12-BIT TFT RED BIT [0]:** This bit is RED Color Data bit 0 (LSB) for 12-bit TFT color LCDs.
			SUD0	**16-BIT STN COLOR UPPER BIT [0]:** This bit is Upper Data bit 0 (LSB) for 16-bit dual- and single-scan STN color LCDs.
FP[21]	138	O	R5	**24-BIT TFT RED BIT [5]:** This bit is RED Color Data bit 5 for 24-bit TFT color LCDs.
			R3	**18-BIT TFT RED BIT [3]:** This bit is RED Color Data bit 3 for 18-bit TFT color LCDs.
			R1	**12-BIT TFT RED BIT [1]:** This bit is RED Color Data bit 1 for 12-bit TFT color LCDs.
			R0	**9-BIT TFT RED BIT [0]:** This bit is RED Color Data bit 0 (LSB) for 9-bit TFT color LCDs.
			SUD1	**16-BIT STN COLOR UPPER BIT [1]:** This bit is Upper Data bit 1 for 16-bit dual- and single-scan STN color LCDs.

2.2 LCD Interface Pins *(cont.)*

Pin Name	Pin No.	Pin Type	Pin Function	Pin Description
FP[22]	139	O	R6	**24-BIT TFT RED BIT [6]:** This bit is RED Color Data bit 6 for 24-bit TFT color LCDs.
			R4	**18-BIT TFT RED BIT [4]:** This bit is RED Color Data bit 4 for 18-bit TFT color LCDs.
			R2	**12-BIT TFT RED BIT [2]:** This bit is RED Color Data bit 2 for 12-bit TFT color LCDs.
			R1	**9-BIT TFT RED BIT [1]:** This bit is RED Color Data bit 1 for 9-bit TFT color LCDs.
			SUD2	**16-BIT STN COLOR UPPER B IT [2]:** This bit is Upper Data bit 2 for 16-bit dual- and single-scan STN color LCDs.
FP[23]	140	O	R7	**24-BIT TFT RED BIT [7]:** This bit is RED Color Data bit 7 (MSB) for 24-bit TFT color LCDs.
			R5	**18-BIT TFT RED BIT [5]:** This bit is RED Color Data bit 5 (MSB) for 18-bit TFT color LCDs.
			R3	**12-BIT TFT RED BIT [3]:** This bit is RED Color Data bit 3 (MSB) for 12-bit TFT color LCDs.
			R2	**9-BIT TFT RED BIT [2]:** This bit is RED Color Data bit 2 (MSB) for 9-bit TFT color LCDs.
			SUD3	**16-BIT STN COLOR UPPER B IT [3]:** This bit is Upper Data bit 3 for 16-bit dual- and single-scan STN color LCDs.
FPDE	108	O		**FLAT PANEL DISPLAY ENABLE:** For those LCDs that require an external display enable, this pin is used to provide a data enable. For the CL-GD7541/GD7543, it is the second Shift Clock output for single-scan dual-clock STN color LCDs.
FPVDCLK	113	O		**FLAT PANEL VIDEO CLOCK:** This signal is used to drive the LCD shift clock, which is designated as CP2 by some LCD manufacturers.
LFS	110	O		**LCD FRAME START:** This output provides a pulse to start a new frame on LCDs.
LLCLK	112	O		**LCD LINE CLOCK:** This output is used to drive the LCD line clock. This signal is also designated as LP or CP1 by some LCD manufacturers.

2.2 LCD Interface Pins *(cont.)*

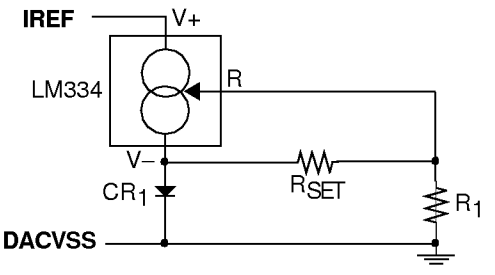
Pin Name	Pin No.	Pin Type	Pin Function	Pin Description
MOD	117	O		**MODULATION:** This output provides AC inversion. This pin must be connected to the MOD, FR, or DF inputs of the LCD, as appropriate. Some LCD manufacturers provide this function in the LCD circuitry, in which case this pin does not need to be connected.

2.3 CRT Interface Pins

Pin Name	Pin No.	Type	Pin Description
BLUE	96	O	**BLUE VIDEO:** This analog output supplies current that corresponds to the **blue** value of the pixel being displayed. Each of the three DACs consists of 255 summed current sources. For each pixel, the 6-bit value from the lookup table is applied to each DAC input to determine the number of current sources to be summed. Full-scale current on the RED, GREEN, and BLUE outputs is related to the IREF signal as follows: $I_{full\text{-}scale} = (63/30) \cdot IREF$ To maintain IBM VGA compatibility, each DAC output is typically terminated to monitor ground with a 150-Ω 2% resistor. This resistor, in parallel with the 150-Ω resistor in the monitor, yields a 50-Ω resistance to ground. For a full-scale voltage of 700 mV, the full-scale current output must be 14 mA.
GREEN	97	O	**GREEN VIDEO:** This analog output supplies current corresponding to the **green** value of the pixel being displayed. *To terminate this pin, refer to information under BLUE VIDEO.*
HSYNC	91	O-TS	**HORIZONTAL SYNC:** This output supplies the horizontal synchronization pulse to the monitor. The polarity of this output is programmable. This pin can be connected directly to the corresponding pin on the monitor connector.
IREF	99	I	**DAC CURRENT REFERENCE:** The current drawn from DACVDD1 and DACVDD2 through this pin determines the full-scale output of each DAC. This pin must be connected to a constant-current source. For information on how to calculate the IREF constant current, refer to the application note "IREF Current Source" in the *CL-GD754X Application Book*.

Table 2-2. Example

R_{SET} (± 1%)	R_1 (± 1%)	Diode CR_1
15 Ω	150 Ω	Schottky diode ($V_F < 0.4$ V)



2.3 CRT Interface Pins *(cont.)*

Pin Name	Pin No.	Type	Pin Description
RED	98	O	**RED VIDEO:** This analog output supplies current corresponding to the **red** value of the pixel being displayed. *To terminate this pin, refer to information under BLUE VIDEO.*
VSYNC	93	O-TS	**VERTICAL SYNC:** This output supplies the vertical synchronization pulse to the monitor. The polarity of this output is programmable. This pin can be connected directly to the corresponding pin on the monitor connector.

2.4 NTSC and PAL Interface Pins

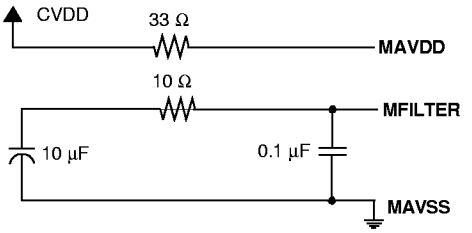
Because LCD control pins are used with NTSC and PAL interfaces, while the NTSC and PAL interface pins are used, LCDs must be isolated. External AND gates must be used to force LCD control signals to the proper levels. (For design details, refer to the application note "Driving NTSC/PAL Display Signals" in the *CL-GD754X Application Book*.)

Pin Name	Pin No.	Type	Pin Description
BLUE	96	O	**BLUE VIDEO:** This analog output supplies current corresponding to the **blue** value of the pixel being displayed. Each of the three DACs consists of 255 summed current sources. For each pixel, the 6-bit value from the lookup table is applied to each DAC input to determine the number of current sources to be summed. Full-scale current on the RED, GREEN, and BLUE outputs is related to IREF as follows: $I_{full\text{-}scale} = (63/30) \cdot IREF$ When an NTSC/PAL encoder is used at the same time as the CRT, there must be a 1.4-kΩ series termination resistor between the CL-GD7541/GD7543 and the R, G, and B inputs of the encoder. There is also a 0.7-kΩ resistor connected to ground from each R, G, and B input, to provide the correct input-voltage level for the encoder. To maintain a full-scale voltage of 700 mV across the CRT inputs, the full-scale current output must be 14 mA. For termination details, refer to Section 2.3, "CRT Interface Pins".
CSYNC	95	O	**COMPOSITE SYNC :** This output provides the Composite SYNC for the analog NTSC/PAL encoder. For NTSC/PAL interfaces, connect CSYNC to the encoder SYNC input.
GREEN	97	O	**GREEN VIDEO:** This analog output supplies current corresponding to the **green** value of the pixel being displayed. *To terminate this pin, refer to information under BLUE VIDEO.*
NTSC/PAL	94	O	**NTSC/PAL ENCODING SELECTION :** This output is used by the CL-GD7541/GD7543 to select the desired NTSC or PAL encoding format. Extension register bits CR30[3:2] control the level on this pin.
RED	98	O	**RED VIDEO:** This analog output supplies current corresponding to the **red** value of the pixel being displayed. *To terminate this pin, refer to information under BLUE VIDEO.*

2.4 NTSC and PAL Interface Pin s *(cont.)*

Pin Name	Pin No.	Type	Pin Description
TVON	146	O	**TV ON:** When Extension register SR25[6] = 0, this output controls the power to the NTSC/PAL encoder. When this output is high, the encoder is powered on. When this output is low, the encoder is turned off.
XRDACCS	146	O	**EXTERNAL RAMDAC CHIP SELECT :** When SR25[6] = 1, a high on this output is used to enable an external RAMDAC. This function is not supported for PCI bus applications.

2.5 Dual-Frequency Synthesizer Interface Pins

Pin Name	Pin No.	Type	Pin Description
CLK32K	89	I	**32-kHz CLOCK:** This input may be connected to an externally supplied 32-kHz clock signal to be used for memory refresh during Suspend mode and panel sequencing. If this pin is not used, it must be connected to the OSC input.
MCLK / XMCLK	197	I or O	**MEMORY CLOCK / EXTERNAL MEMORY CLOCK (CL-GD7541 Only):** This pin's function depends on register settings and whether or not a pull-up resistor is connected to the CL-GD7541 DFBSPU pin. This pin is intended primarily for test purposes. (For details, refer to Section 2.8, "Switch and Miscellaneous Configuration Input Pins", and the description of DFBSPU in Section 2.7, "Configuration Input Pins".)
MFILTER	200	O	**MEMORY CLOCK FILTER:** This pin *must* be connected to a π-RC filter which is returned to MAVSS. The filter components, especially the input capacitor and the resistor, *must* be placed as close as possible to the MFILTER pin.  **Figure 2-1. Typical Memory Clock Filter**
OSC	85	I	**OSCILLATOR INPUT:** This TTL input pin supplies the reference frequency for the dual-frequency synthesizer. It requires an input frequency of 14.318 MHz $\pm$ 0.01% with a duty cycle of 50% $\pm$ 10%. This input can be supplied from the appropriate pin on the PCI bus, or from an oscillator.
XVCLK	85	I	**EXTENDED VIDEO CLOCK INPUT:** When a pull-up resistor is connected to the XCLKPU pin (pin 164), this pin is configured for an external clock input. This pin is intended for test purposes only.

2.5 Dual-Frequency Synthesizer Interface Pin s *(cont.)*

Pin Name	Pin No.	Type	Pin Description
VFILTER	83	O	**VIDEO CLOCK FILTER :** This pin *must* be connected to a π-RC filter which is returned to VAVSS. The filter components, especially the input capacitor and the resistor, *must* be placed as close as possible to the VFILTER pin.

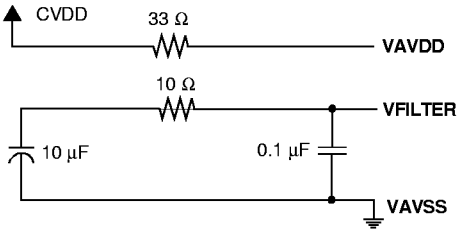


Figure 2-2. Typical Video Clock Filte r

2.6 Display Memory Interface Pin s

Pin Name	Pin No.	Type	Pin Description
CAS#	181	O	**COLUMN ADDRESS STROBE#:** This active-low output is used to latch the column address from MA[9:0] into the DRAMs. When register SRF[0] = 0 (multiple-WE# DRAM configuration), this pin is defined as CAS# and must be connected to the CAS# inputs of the DRAMs.
WE#	181	O	**WRITE ENABLE# :** When Extension register SRF[0] = 1 (multiple-CAS# DRAM configuration), this pin is defined as WE# and must be connected to the WE# inputs of the DRAMs.
CAS[3:0]#	169–170 195:194	O	**COLUMN ADDRESS STROBE [3:0]#:** These active-low outputs are used to control the CAS# (or WE#) inputs to the DRAMs. When Extension register SRF[0] = 1 (multiple-CAS# DRAM configuration), these active-low outputs must be connected to the CAS# inputs of the DRAMs.
WE[3:0]#	169–170 195:194	O	**WRITE ENABLE [3:0]# :** When Extension register SRF[0] = 0 (multiple-WE# DRAM configuration), these active-low outputs must be connected to the WE# inputs of the DRAMs.
MA[9:0]	171–180	O	**MEMORY ADDRESS [9:0] :** These outputs drive the address inputs of the DRAMs.
MD[31:0]	151–161 163–167 186–191 193,196 202–204 206–208 1–2	I/O	**MEMORY DATA [31:0] :** These bidirectional pins are used to transfer data between the CL-GD7541/GD7543 and display memory. These pins must be connected to the data pins of the DRAMs.
OE#	182	O	**OUTPUT ENABLE# :** This active-low output is used to control the Output Enables of the DRAMs. For 256K × 16 DRAMs with Dual-Write Enables, this pin must be connected to the OE# pins of all the DRAMs in the display memory array.
RAS[1:0]#	184:183	O	**ROW ADDRESS STROBE [1:0]#:** These active-low outputs are used to latch the row address from MA[9:0] into the DRAMs. Each RAS pin is used for one bank of memory, for a total of two banks. These pins must be connected to the RAS# pins of all the DRAMs in the display memory array.

2.7 Configuration Input Pins

The configuration input pins may be under either hardware or software control.

- When hardware control is used, the state of all external pull-ups on the memory data pins (MD31:0) are read and latched by the CL-GD7541/GD7543 during hardware reset only.
- When software control is used, any 1-to-0 transition of Extension register bit SR24[3] allows the state of all external pull-ups on the memory data pins to be read and latched by the CL-GD7541/GD7543 at any time, not just at hardware reset. Software control is used whenever it is desired to read configuration pins independent of system reset. With software control:
  - Power to all parts of the graphics controller is turned off.
  - The system reset pulse is too short to read the switches that have large pull-up or pull-down resistance.

Pin Name	Pin No.	Type	Pin Description
DFBSPU	160	I	**DYNAMIC FRAME-BUFFER SHARING PULL-UP (CL-GD7541 Only)**: This pin configures the CL-GD7541 for dynamic frame-buffer sharing (DFBS). For DFBS configuration, a pull-up resistor must be connected to DFBSPU, and SR25[7] must be set to 1. As a result: • The SW0 / MCLK / XMCLK pin is configured for MCLK or XMCLK. • The SW1 pin is configured for its memory grant function. • The SW2 pin is configured for its memory request function. For details, refer to Section 2.8, "Switch and Miscellaneous Configuration Input Pins".
FCPU	157	I	**FEATURE CONNECTOR PULL-UP:** When a pull-up is connected to this pin, at system reset SR24[7] stores the logic high, and the CL-GD7541/GD7543 is configured to supply all Feature Connector signals. (Refer to Section 2.9, "Feature Connector Pins".)
FVLPU	165	I	**FAST VESA VL-BUS PULL-UP[a]:** When a pull-up is connected to this pin, at system reset SR22[2] stores the logic high, and the CL-GD7541/GD7543 is configured for a 50-MHz bus clock input.
PCI-MGPU	159	I	**PCI BUS SELECT AND MINUMUM-GRANT EXTEND PULL-UP[a]:** When a pull-up is connected to this pin, at system reset SR22[7] stores the logic high. As a result, the CL-GD7541/GD7543 is configured for PCI bus operation, and the minimum-grant value is extended from 250 ns to 500 ns. When GRE[4] = 1, PCI Burst mode is selected.
PCIPU	167	I	**PCI BUS SELECT PULL-UP[a]:** When a pull-up is connected to this pin, at system reset SR22[0] stores the logic high. As a result, the CL-GD7541/GD7543 is configured for PCI bus operation and a minimum-grant value of 250 ns. When GRE[4] = 1, PCI Burst mode is selected.

[a] To choose the system bus, a pull-up resistor can be supplied on only one of the following: PCI-MGPU (pin 159), FVLPU (pin 165), or PCIPU (pin 167). When no pull-up resistor is supplied, the CL-GD7541/GD7543 is configured for a VESA VL-Bus operation of 33 MHz or less.

2.7 Configuration Input Pins *(cont.)*

Pin Name	Pin No.	Type	Pin Description
S46PU	161	I	**SLEEP ADDRESS SELECT PULL-UP:** When a pull-up resistor is: • *Connected*, at system reset, Extension register SR22[5] stores the logic high. The CL-GD7541/GD7543 is configured for the 46E8[3] sleep address, which is used when the CL-GD7541/GD7543 is used with an adapter board. • *Not connected*, the CL-GD7541/GD7543 selects the 3C3[0] sleep address, normally used when the CL-GD7541/GD7543 is used with a motherboard.
SW1PU	156	I	**SWITCH 1 PULL-UP (CL-GD7541 Only)**: If the CL-GD7541 DFBSPU pin has a pull-up resistor connected, this pin is used to define the value of SW1. This pin is either read at system reset, or if Extension register SR24[3] is 1, this pin is read at any time. The value of this pin is read into SR24[1].
SW2PU	155	I	**SWITCH 2 PULL-UP (CL-GD7541 Only)**: If the CL-GD7541 DFBSPU pin has a pull-up resistor connected, this pin is used to define the value of SW2. This pin is either read at system reset, or if Extension register SR24[3] is 1, this pin is read at any time. The value of this pin is read into SR24[2].
XCLKPU	164	I	**EXTERNAL CLOCK SELECT PULL-UP (CL-GD7541 Only)**: When a pull-up resistor is: • *Connected*, at system reset the CL-GD7541 is configured for external clock inputs on the SW0 / MCLK / XMCLK and OSC / XVLCK pins. This configuration is used for test purposes only. • *Not connected*, the CL-GD7541 uses internal clock sources. (No pull-up must be connected during normal operation.)

2.8 Switch and Miscellaneous Configuration Input P ins

Pin Name	Pin No.	Type	Pin Description
CL-GD7541 (Pull-up resistor connected to DFBSPU)			
The pin descriptions in this section apply only to the CL-GD7541, and only when DFBSPU (pin 160) is connected to a pull-up resistor.			
MCLK / XMCLK	197	I or O	**MEMORY CLOCK / EXTERNAL MEMORY CLOCK:** When the DFBSPU pin is connected to a pull-up resistor, this pin is configured to output MCLK or accept XMCLK as an input, depending on the setting for Extension register SR23[0]. When Extension register SR23[0] is: • 0, this pin can be used to output the internal MCLK. The MCLK output is available only if : — A <60-Ω pull-up resistor is attached to DFBSPU . — Extension Register SR25[7] is set to 1 . • 1, this pin can be used to input an external XMCLK source.
MGNT#	149	O	**MEMORY GRANT:** When the DFBSPU pin is connected to a pull-up resistor, this pin is configured to output the memory grant value.
MRQIN	150	O	**MEMORY REQUEST INPUT:** When the DFBSPU pin is connected to a pull-up resistor, this pin is configured to output the memory data stored in register SR24[2].
TWR#	100	I	**TEST WRITE# :** This active-low input is for factory test purposes only. For normal operation, this pin *must not* be connected to the system. It has an internal pull-up resistor connected.
CL-GD7541 or CL-GD7543 (Pull-up resistor not connected to DFBSPU)			
The pin descriptions in this section apply to both the CL-GD7541 and to the , and only when the DFBSPU pin is *not* connected to a pull-up resistor.			
SW0	197	I	**SWITCH 0:** This pin is configured as a hardware input that can be read under register control. The level on this pin is stored in SR24[0].
SW1	149	I	**SWITCH 1:** This pin is configured as a hardware input that can be read under register control. The level on this pin is stored in SR24[1].
SW2	150	I	**SWITCH 2:** This pin is configured as a hardware input that can be read under register control. The level on this pin is stored in SR24[2].
TWR#	100	I	**TEST WRITE# :** This active-low input is for factory test purposes only. For normal operation, this pin *must not* be connected to the system. It has an internal pull-up resistor connected.

2.9 Feature Connector Pins

When an external pull-up resistor (<60-kΩ) is connected to the FCPU / MD[25] pin, a logic high is read and stored in Extension register SR24[7] during the rising edge of the system reset pulse. This high level configures the CL-GD7541/GD7543 to supply all the following Feature Connector signals. When no pull-up resistor is supplied, these pins are configured for other operations.

Pin Name	Pin No.	Type	Pin Description
FCBLANK#	101	I or O	**FEATURE-CONNECTOR BLANK #**: When FCESYNC# is high, FCBLANK# is an output that supplies a blanking signal to the feature connector. When FCESYNC# is low, FCBLANK# is an input which can force RGB outputs to zero current.
FCDCLK	103	O	**FEATURE-CONNECTOR DOT CLOCK :** When the Feature Connector configuration is active, this pin provides the dot clock output to the sub-system that is driven by the Feature Connector.
VCLK	103	O	**VIDEO CLOCK :** This is a video clock output. This pin is intended to be used for test purposes only.
FCESYNC#	147	I	**FEATURE-CONNECTOR ENABLE SYNC#:** When this input is high, the HSYNC, VSYNC, and FCBLANK# outputs are enabled. When this input is low, the HSYNC and VSYNC outputs are forced to high-impedance (off), and FCBLANK# is configured as an input.
FCEVIDEO#	86	I or O	**FEATURE-CONNECTOR ENABLE VIDEO#:** This pin controls the buffers on FCP[7:0]. When FCEVIDEO# is low, the FCP[7:0] pins are inputs, and display memory contents are ignored. When FCEVIDEO# is high, the FCP[7:0] pins are pixel data outputs.
FCP[15:8]	24:17	I or O	**FEATURE-CONNECTOR PIXEL DATA [15:8]**. When implementing a CL-GD7543 design, to ensure pin compatibility with other SVGA controllers in the CL-GD754X family, reserve these FCP[15:8] pins for Feature Connector implementation.
FCP[7:0]	144:141 134:133 125,123		**FEATURE-CONNECTOR PIXEL DATA [7:0] (CL-GD7541/GD754 3):** When FCEVIDEO# is low, these pins are inputs that can be used to drive pixel data into the palette DAC. When FCEVIDEO# is high, these pins are pixel data outputs that copy the pixel address to the palette RAM.
FCVCLK	114	I	**FEATURE-CONNECTOR VIDEO CLOCK :** This pin must be connected to the pixel clock from the Feature Connector. For more information, refer to Extension register SR23[7].

2.9 Feature Connecto r Pins *(cont.)*

Pin Name	Pin No.	Type	Pin Description
OVRW#	115	O	**OVERLAY WINDOW:** This active-low output is asserted during the active portion of the video overlay window. It is intended to be used in applications involving video overlays. When Extension register CR1A[3:2] is used to select the color key as the dynamic overlay method, this pin goes high when a color key match occurs one or more clocks before valid data is expected on the pixel bus. For additional information, refer to the application note "The 8-Bit Dynamic Video Overlay" in the *CL-GD754X Application Boo k*.

2.10 Power Management Pins

Pin Name	Pin No.	Type	Pin Description
ACTI	86	I	**ACTIVITY:** When Extension register SR23[6] = 1, this pin is configured for ACTI, an optional activity-sense input. With register masking, any low-to-high transition on this pin may be used to reset the internal power-down timers. When SR23[6] is 1, CR2D[6] is 1, and the ACTI input is: – *High*, ACTI resets the Standby timer. – *Low*, ACTI resets the Backlight timer.
SBYI	86	I	**STANDBY INPUT:** When SR23[6] = 0, this pin is configured for SBYI, the hardware control for Standby mode. When SBYI goes high, it initiates the power-down sequence that starts Standby mode. When not used, this input must be connected to ground.
BLI	87	I	**BACKLIGHT INPUT:** When Extension register SR23[5] = 1, a high on this input turns off the backlight of the LCD display.
SUSPI	87	I	**SUSPEND INPUT:** When Extension register SR23[5] = 0, a high on this internally de-bounced input initiates hardware-controlled Suspend mode. The hardware-controlled Suspend mode is the most efficient power-saving mode for the system.
CLK32K	89	I	**32-kHz CLOCK:** This input may be connected to an externally supplied 32-kHz clock signal to be used for memory refresh during Suspend mode and panel sequencing. If not used, this pin must be connected to the OSC input.
FPBL	105	O	**FLAT PANEL BACKLIGHT:** This output is part of LCD power sequencing. This pin must be connected to the LCD backlight enable.
FPVCC	106	O	**FLAT PANEL VCC:** This output is part of LCD power sequencing. This pin must be connected to the LCD logic-power enable.
FPVEE	102	O	**FLAT PANEL VEE:** This output is part of LCD power sequencing. This pin must be connected to the LCD power enable.
PROG	148	O	**PROGRAMMABLE OUTPUT:** This output pin is forced high or low under the control of register CR30[7]. It is used by the VGA BIOS to select 3.3- or 5.0-V power supplies to support the operating frequencies selected.
SBYST#	123	O	**STANDBY STATUS#:** When low, this output indicates that the CL-GD7541/GD7543 is in Standby mode.

2.10 Power Management Pin s *(cont.)*

Pin Name	Pin No.	Type	Pin Description
SLEEP#	81	I	**SLEEP# :** This active-low input is used by the external hardware to put the CL-GD7541/GD7543 into bus Sleep mode.
SUSPST#	125	O	**SUSPEND STATUS#:** This active-low output indicates that the CL-GD7541/GD7543 is in Suspend mode.

2.11 Ground Pins

Pin Name	Pin No.	Pin Description
DACVSS[2:1]	88, 111	**DIGITAL-TO-ANALOG CONVERTER VSS GROUND [2:1] :** These two pins are used to supply ground reference to the palette DAC of the CL-GD7541/GD7543. Each pin *must* be connected to the analog ground rail, which must be isolated from VSS (digital) ground.
MAVSS	201	**MEMORY CLOCK ANALOG VSS GROUND :** This pin is used to supply ground reference to the memory clock synthesizer of the CL-GD7541/GD7543. This pin *must* be connected to the analog ground rail, which must be isolated from VSS (digital) ground.
VAVSS	82	**VIDEO CLOCK ANALOG VSS GROUND:** This pin is used to supply ground reference to the video clock synthesizer of the CL-GD7541/GD7543. This pin *must* be connected to the analog ground rail, which must be isolated from VSS (digital) ground.
VSS[11:1]	198, i85, 168, 145, 124, 104, 80, 67, 52, 42, 6	**VSS (Digital) GROUND :** These pins are used to supply ground reference for the core logic and pin interface groups of the CL-GD7541/GD7543. • Each pin *must* be connected directly to the ground rail. • When a multi-layer board is used, each VSS pin *must* be connected to the ground plane.

2.12 Power Pins

Pin Name	Pin No.	Pin Description
BVDD[2:1]	47,73	**BUS VDD :** These two pins are used to supply either +3.3 or +5.0 V to the bus interface pin group of the CL-GD7541/GD7543. • Each pin *must* be connected directly to the VDD rail . • Each pin *must* be bypassed with a 0.1 -µF capacitor that has the proper high-frequency characteristics and is as close to each pin as possible. • When a multi-layer board is used, conne ct BVDD pins to the power plane.
CRTVDD	92	**CRT VDD :** This pin is used to supply +3.3 or +5.0 V to the CRT interface pin group of the CL-GD7541/GD7543. • This pin *must* be connected directly to the VDD rail . • This pin *must* be bypassed with a 0.1 -µF capacitor that has the proper high-frequency characteristics and is as close to the pin as possible . • When a multi-layer board is used, connect t he CRTVDD pin to the power plane.
CVDD[4:1]	192, 121, 62, 36	**CORE VDD [4:1]:** These four pins are used to supply +3.3 or +5.0 V to the internal core logic of the CL-GD7541/GD7543. • Each pin *must* be connected directly to the VDD rail . • Each pin *must* be bypassed with a 0.1 -µF capacitor that has the proper high-frequency characteristics and is as close to each pin as possible. • When a multi-layer board is used, connect CVDD pins to the power plane.
DACVDD[2:1]	109, 90	**DIGITAL-TO-ANALOG CONVERTER VDD [2:1] :** These two pins are used to supply voltage to the palette DAC of the CL-GD7541/GD7543. • Each pin *must* be connected directly to the CVDD rail. • Each pin *must* be bypassed with 0.1- and 10 -µF capacitors that have the proper high-frequency characteristics and are as close to each pin as po s-sible. • When a multi-layer board is used, connect DACVDD pins to the power plane.
FPVDD[2:1]	107, 132	**FLAT PANEL VDD [2:1]:** This pin is used to supply +3.3 or +5.0 V to the LCD interface pin group of the CL-GD7541/GD7543. • Each pin *must* be connected directly to the VDD rail . • Each pin *must* be bypassed with a 0.1 -µF capacitor that has the proper high-frequency characteristics and is as close to the pin as possible . • When a multi-layer board is used, connect FPVDD pins to the power plane.

2.12 Power Pin s *(cont.)*

Pin Name	Pin No.	Pin Description
MAVDD	199	**MCLK ANALOG VD D:** This pin is used to supply +3.3 or +5.0 V to the memory clock synthesizer of the CL-GD7541/GD7543. This pin *must* be connected to the CVDD rail via a 33-Ω resistor and bypassed to MAVSS with 0.1- and 10-µF capacitors.
MVDD[2:1]	205, 162	**MEMORY VDD [2:1]:** These two pins are used to supply +3.3 or +5.0 V to the internal memory (DRAM) interface pin group of the CL-GD7541/GD7543. • Each pin *must* be connected directly to the VDD rail. • Each pin *must* be bypassed with a 0.1 -µF capacitor that has the proper high-frequency characteristics and is as close to each pin as possible. • When a multi-layer board is used, connect MVDD pins to the power plane .
VAVDD	84	**VCLK ANALOG VD D:** This pin is used to supply +3.3 or +5.0 V to the video clock synthesizer of the CL-GD7541/GD7543. This pin *must* be connected to the CVDD rail via a 33-Ω resistor and bypassed to VAVSS with 0.1- and 10-µF capacitors.

3. FUNCTIONAL DESCRIPTION

This section provides functional information and design guidelines for the CL-GD7541/GD7543.

3.1 Introduction

The CL-GD7541/GD7543 offers a tightly integrated, high-performance motherboard solution. Multiple designs can be developed, ranging from a relatively simple GUIX (Graphical User Interface Accelerator) solution to a portable multimedia solution capable of displaying accelerated video playback windows with graphics or an overlaid live video window with graphics. All hardware needed for CPU updates to memory, display refresh, and DRAM refresh is included in the CL-GD7541/GD7543. A complete SVGA-compatible motherboard solution can be implemented with the CL-GD7541/GD7543 plus two 256K × 16 DRAMs.

3.2 Functional Blocks

Figure 3-1 shows a block diagram of the CL-GD7541/GD7543. The functional blocks integrated in the CL-GD7541/GD7543 controllers are described in the following sections.

3.2.1 CPU Bus Interface

The CL-GD7541/GD7543 connects directly to a '486 local bus, a VESA VL-Bus, or a PCI bus. No additional logic circuitry is required to implement these bus interfaces.

NOTE: The CL-GD7541/GD7543 is optimized for motherboard implementations that integrate system and VGA BIOS. As a result, the CL-GD7541/GD7543 does not support external BIOSs.

'486/VL-Bus

The CL-GD7541/GD7543 interfaces directly to '486DX microprocessors and the VESA VL-Bus, at MCLK speeds up to 60 MHz with the core VDD at 5 V.

PCI Bus

The CL-GD7541/GD7543 interfaces directly to the PCI bus. No additional logic is required to support the CL-GD7541/GD7543 multiplexed address and data pins. The CL-GD7541/GD7543 executes 32-bit I/O and memory accesses at speeds up to 33 MHz. The CL-GD7541/GD7543 also supports memory burst cycles. PCI bandwidth is at least 33% more efficiently utilized with burst cycles.

In the PCI bus configuration, the CL-GD7541/GD7543 supports big-endian word swapping, allowing the loading of 'X86 little-endian data or PowerPC big-endian data into display memory, depending upon the application requirements.

Linear Memory Addressing

The CL-GD7541/GD7543 supports linear memory addressing, as an alternative to the standard VGA method of accessing display memory with 64-Kbyte segments. With linear memory addressing, the CL-GD7541/GD7543 is configured to access display memory as a 1- or 2-Mbyte linearly addressed string of bytes.

For applications or drivers that support this method, linear memory addressing improves graphics performance by simplifying access to display memory, since it is not necessary to calculate offsets into a relatively small window, nor is it necessary to test for a crossing of the window boundary.

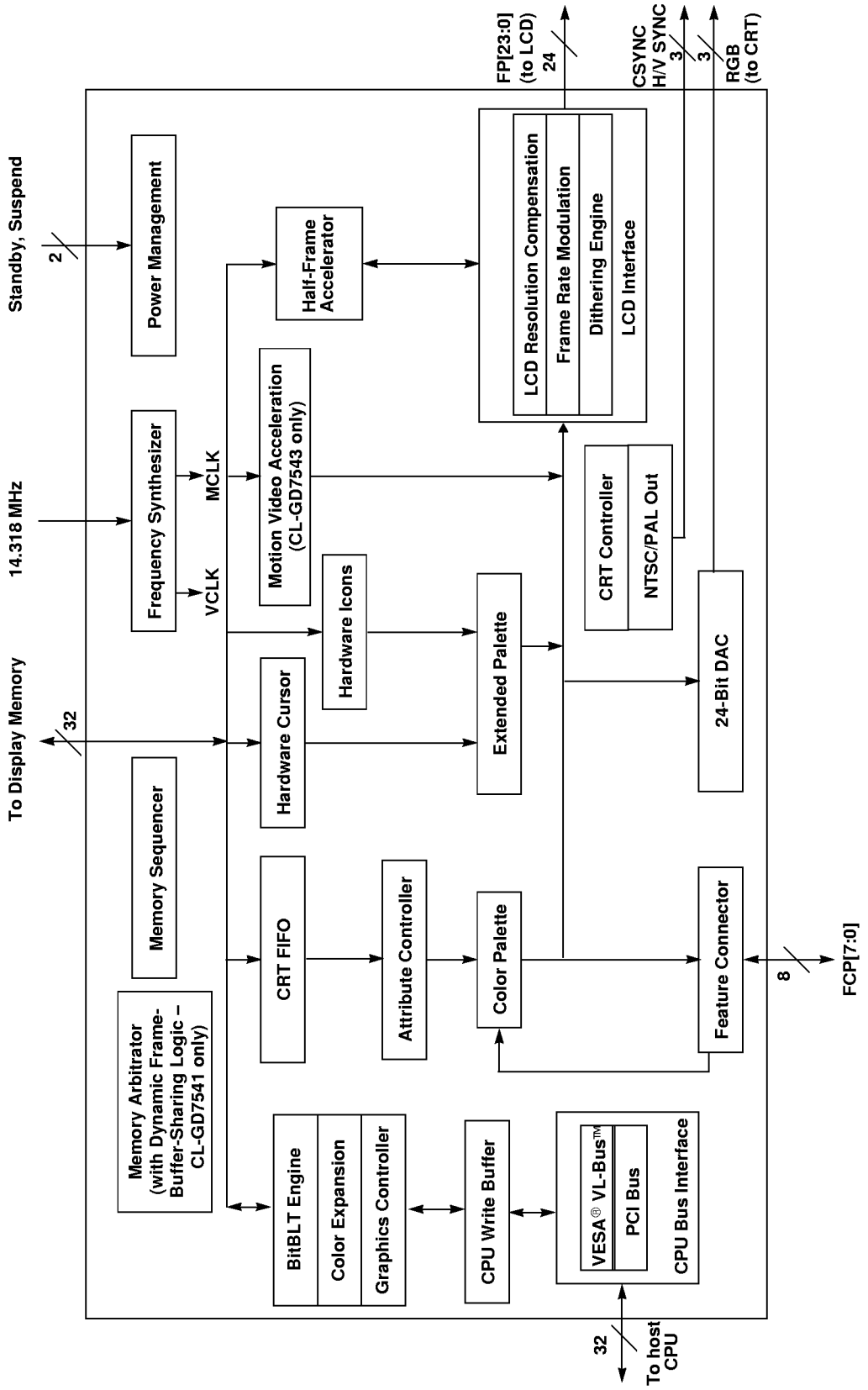


Figure 3-1. CL-GD7541/GD754 3 Block Diagra m

The CL-GD7541/GD7543 supports linear memory addressing of the VGA address space, which may reside within any 1-Mbyte segment above the first 16 Mbytes in a 4-Gbyte address space. For'486 local bus interfaces that use a 32-bit address, to select the desired 16-Mbyte partition with the A[31:24] address line, an external decoder may be needed. However, in general, there is no need for an external decode of the CPU addresses. Any one of the A[31] to A[24] lines can be directly connected to HIMEM0 or HIMEM1. For instance, if HIMEM1 is connected to A[31], then the CL-GD7541/GD7543 is mapped into the upper 2 Gbytes of the CPU address space.

The register bits SR2D[7:6] extend the address space to 64 Mbytes by re-mapping HIMEM0 and HIMEM1 within this address space. An external decoder may be needed only if a fully decoded 16-Mbyte partition within the 4-Gbyte address space is desired. The output from this address-line decoder drives the HIMEM0 and HIMEM1 inputs. Extension register bits SR7[7:4] are used to select the 1-Mbyte through 16-Mbyte range in any 16-Mbyte space allowed by the microprocessor.

NOTE: HIMEM0 and HIMEM1 are used only with the VESA VL-Bus and 32-bit local buses.

3.2.2 CPU Write Buffer

The CPU write buffer contains a queue of CPU write accesses to display memory that have not been executed due to memory arbitration. Maintaining this queue of write accesses allows the CL-GD7541/GD7543 to release the CPU bus as soon as it has recorded the address and data. The CL-GD7541/GD7543 therefore executes the operation when display memory is available, increasing CPU performance.

For all text and graphics modes, the write buffer depth is two 32-bit or four 16-bit levels. The CL-GD7541/GD7543 has the capability to page CPU cycles if they are accumulated in the write buffer.

3.2.3 Graphics Controller

The graphics controller operates in either text or graphics modes. It performs these major functions:

- Provides the host CPU a read/write access path to display memory
- Controls all four memory planes in planar modes
- Allows data to be manipulated prior to being written to display memory
- Formats data for use in various backward compatibility modes
- Provides color read comparators for use in color painting modes
- Reads/writes 32-bit words through the 32-bit display memory interface

The graphics controller directs data from the display memory to the CPU. Figure 3-2 and Figure 3-3 illustrate typical write and read operations, respectively.

For a write operation, the data from the CPU bus are combined with the data from the Set/Reset Logic in the CPU, depending on the Write mode. In addition, the data may be combined with the contents of the read latches, and some bits or planes can be masked (that is, prevented from being changed) by using the Bit Mask register. For more information, refer to the Graphics Controller registers in Chapter 10.

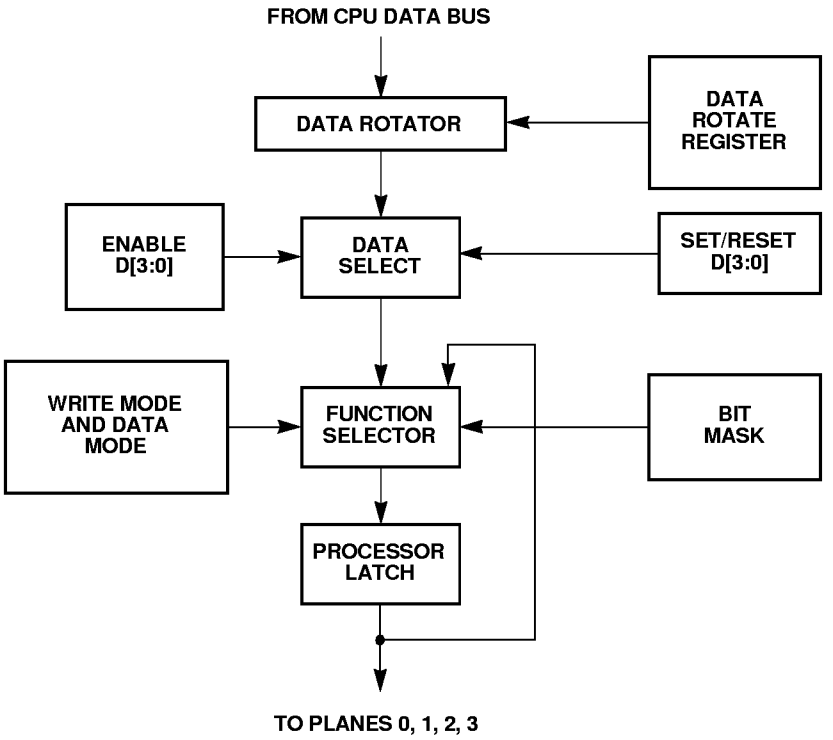


Figure 3-2. Graphics Controller Write Operatio n

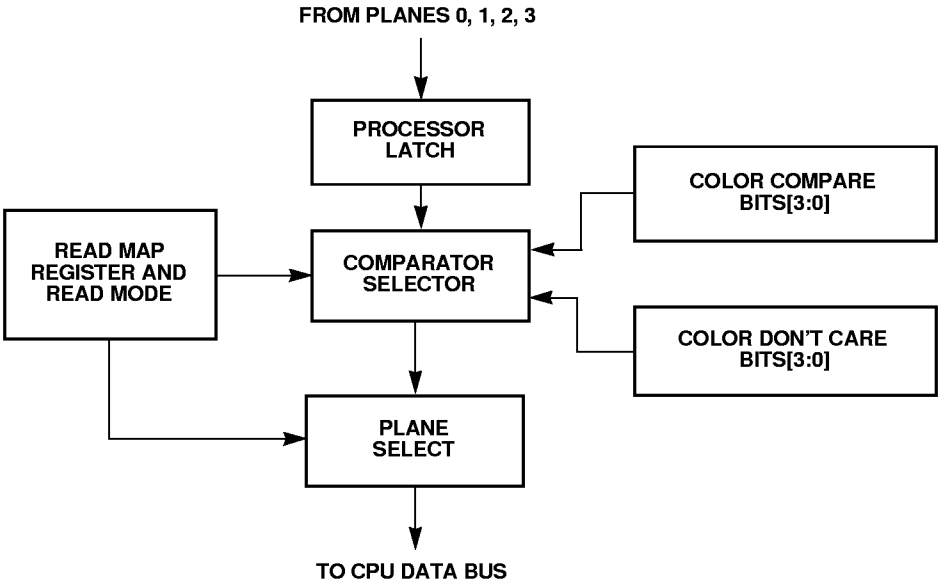


Figure 3-3. Graphics Controller Read Operatio n

3.2.4 Color Expansion

Color expansion is the automatic conversion of a monochrome bit map (which typically defines a character, icon, or pattern) into foreground and background color values. These values are then written into display memory and held in a CL-GD7541/GD7543 register.

Color expansion improves CPU write performance, in that is optimizes use of the available host bandwidth by expanding single bits across the bus into complete 8- or 16-bit pixels.

When color expansion is used, only monochrome bit maps must be transmitted across the bus. Each bit of the monochrome map is converted into 8- or 16-bit pixel modes. The bus traffic is reduced by a factor of 8 to 16, making it possible to use nearly all of the available display memory bandwidth

3.2.5 Bit Block Transfer (BitBLT) Engine

The BitBLT engine moves a rectangle of data either within display memory or between system memory and display memory, with minimal CPU intervention. The BitBLT engine can also performpattern fills (filling an area with a repeating pattern), raster operations (combining the source bytes with the destination bytes using various logic operations), and color expansion or transparency.

The BitBLT engine provides 16 two-operand ROPs (raster operations) to move data in packed-pixel modes from the source area to the destination area. This operation occurs in packed-pixel modes with 8- or 16-bit pixel transfers. The transfers from the CPU are always taken in four-byte increments. For screen-system transfers, the BitBLT operation acts as a read cache. The BitBLT accelerates Graphical User Interfaces (GUIs), such as Microsoft Windows 3.1, Windows NT, and OS/2 2.1. For more information, refer to Appendix A.

3.2.6 Memory Arbitrator

The memory arbitrator allocates bandwidth to the following functions, which compete for the limited bandwidth of display memory:

- CPU access
- Display refresh
- DRAM refresh
- Dynamic frame-buffer-sharing logic (available only in the CL-GD7541)
- BitBLT
- Half-Frame Accelerator (for dual-scan STN LCDs)
- Hardware cursor
- Hardware icons

DRAM refresh is handled invisibly by allocating a selectable number of CAS#-before-RAS# refresh cycles at the beginning of each scanline. Cycles are allocated to display refresh and CPU/BitBLT according to the FIFO-control parameters, with priority given to display refresh.

3.2.7 Memory Sequence r

The memory sequencer generates for display memory all the necessary timing and control signals, including RAS#, CAS#, and multiplexed-address timing, as well as WE# and OE# timing. The sequencer generates CAS#-before-RAS# refresh, random-read, random-early-write, fast-page-mode read, and early-write cycles.

The memory sequencer generates multiple-CAS# or multiple-WE# signals, depending on the memory type being used. The CL-GD7541/GD7543 supports both multiple-CAS# and multiple-WE# 256K × 16 DRAMs. The CL-GD7541/GD7543 supports the following memory configurations, which have a 32-bit-wide memory interface:

- Two 256K × 16 DRAMs for 1-Mbyte display memor y
- Four 256K × 16 DRAMs for a 2-Mbyte display memor y
- Four 512K × 8 DRAMs (symmetric only) for a 2-Mbyte display memo ry
- Two 256K × 16 Extended-Data-Out (or 'Hyper-Page') DRAMs for 1-Mbyte display memor y
- Four 256K × 16 Extended-Data-Out (or 'Hyper-Page') DRAMs for a 2-Mbyte display memor y

For more information on memory configurations, refer to Appendix F.

The memory sequencer ensures that the necessary display refresh transfer cycles and dynamic memory refresh cycles are executed and that the remaining memory cycles are made available for CPU read/write operations.

The CL-GD7541/GD7543 fully supports all the standard IBM VGA memory organizations, along with the following extended graphics memory modes:

- 2-color packed-pixel modes (1-bit/pixel) in linear 32-bit words or VGA-style 8-bit word s
- 16-color planar mode (4 bits/pixe l)
- 256-color packed-pixel modes (8 bits/pixel)
- Direct-color (32K or 64K colors) packed-pixel modes (16 bits/pixel)
- Mixed 32K- and 256-color packed-pixel modes (15 bits/pixel)
- True-color 16M-color packed-pixel modes (24 bits/pixe l)

In true packed-pixel addressing, consecutive pixels are stored at consecutive addresses. This storage method is in contrast with the storage method used by VGA chain-4 addressing, a type of addressing that stores consecutive pixels at every fourth byte address in display memory. For more information, refer to Appendix E and Appendix K.

3.2.8 Dynamic Frame-Buffer-Sharing Logic (CL-GD754 1 Only)

The CL-GD7541 supports dynamic frame-buffer-sharing (DFBS) logic. The DFBS logic presents a method for several controllers with either similar or different functions to share access to the same memory array (normally DRAMs). For example, one controller may do all screen refresh accesses, while at the same time, a second controller may help with CPU accesses to memory data

3.2.9 CRT FIFO

The CRT FIFO (first-in, first-out) is a register that allows the memory sequencer to execute display memory accesses needed for display refresh at maximum memory speed, rather than at the display refresh rate. This register makes it possible to take advantage of DRAM fast-page mode operation. The CRT FIFO register is 16 words deep and 32 bits wide.

3.2.10 Attribute Controller

The attribute controller formats the display for the screen. It performs the following:

- Serialization of memory data
- Display color selection
- Text blinking
- Underlining in both text and graphics modes

The attribute controller is described in Chapter 11. Figure 3-4 is a functional block diagram of the attribute controller.

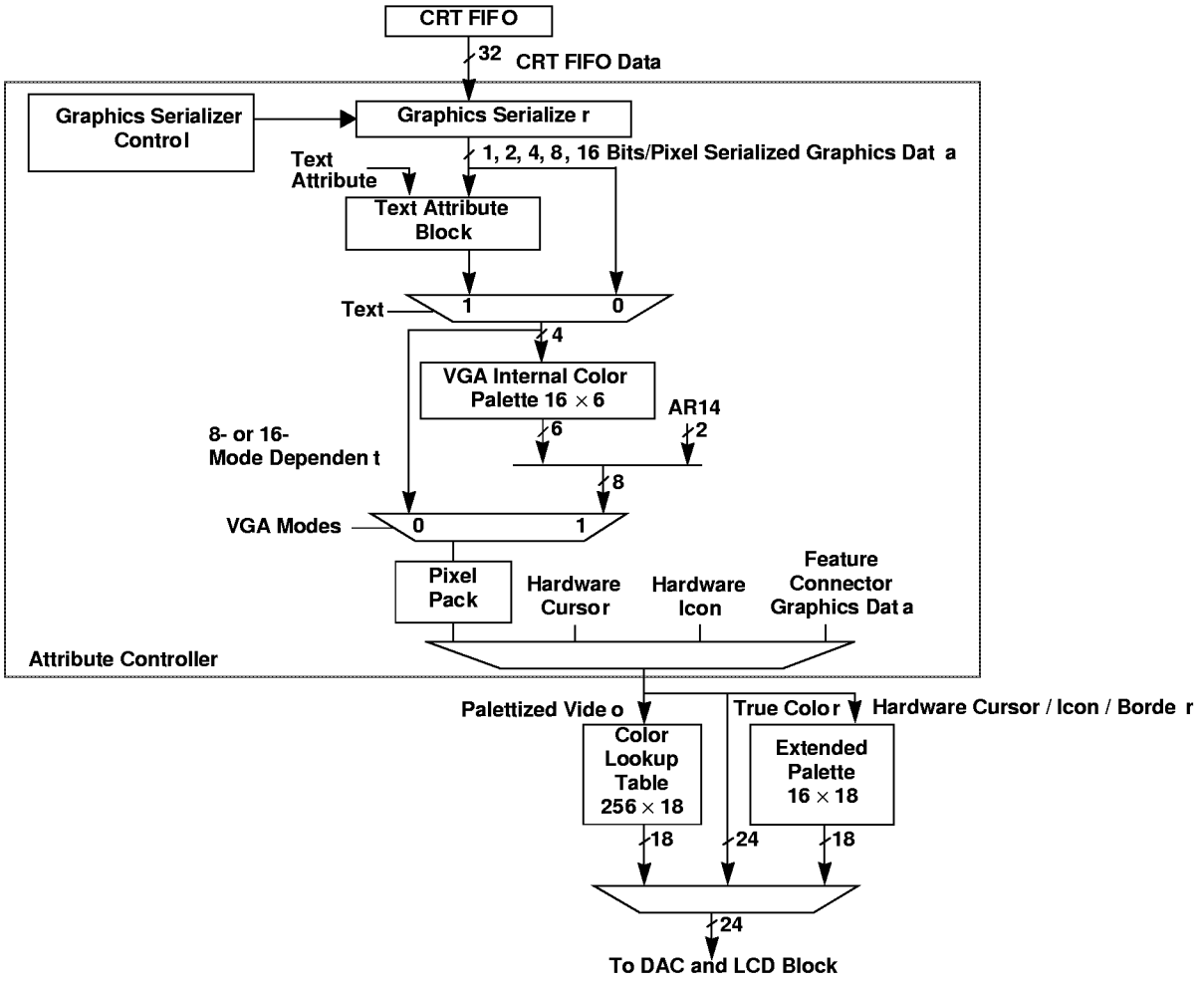


Figure 3-4. Attribute Controller Functional Block Diagram

3.2.11 CRT Controlle r

The CRT controller (CRTC) generates horizontal and vertical synchronization signals (HSYNC and VSYNC) for the CRT display. The CRTC registers generate BLANK# signals required by the palette DAC. They also support standard VGA-compatible modes and extended modes and provide for the following:

- Configuration option s (including user-configurable horizontal/vertical timing and polarity)
- Cursor positioning
- Horizontal scanline s
- Pixel and byte pannin g
- Split-screen capability and smooth scrollin g

The CL-GD7541/GD7543 supports standard VGA text modes and the following additional text modes: 132 × 25, 132 × 43, and 132 × 50. The CL-GD7541/GD7543 supports standard VGA graphics modes and the following additional graphics modes:

- For CRTs
  - 1280 × 1024 interlaced, up to 256 color s
  - 1024 × 768 non-interlaced, up to 256 color s
- For CRTs and LCDs (non-interlaced)
  - 800 × 600, up to 64K color s
  - 640 × 480, up to 16M color s

SimulSCAN™ mode, the simultaneous display capability, is supported at resolutions of 640× 480 or 800 × 600. For a complete listing of all modes supported by the CL-GD7541/GD7543, refer to Chapter 4.

Up to 1024 × 768 16-bit/pixel modes (that is, 5-5-5 R-G-B direct-color modes) are supported with either a 1× VCLK (pixel rate is equal to VCLK) or with a 2× VCLK (pixel rate is equal to twice the VCLK). The 640 × 480 24-bit/pixel modes (8-8-8, the R-G-B true-color modes) are supported with a 3× VCLK (that is, the pixel rate is equal to three times the VCLK). Figure 3-5 is a functional block diagram of the CRT controller.

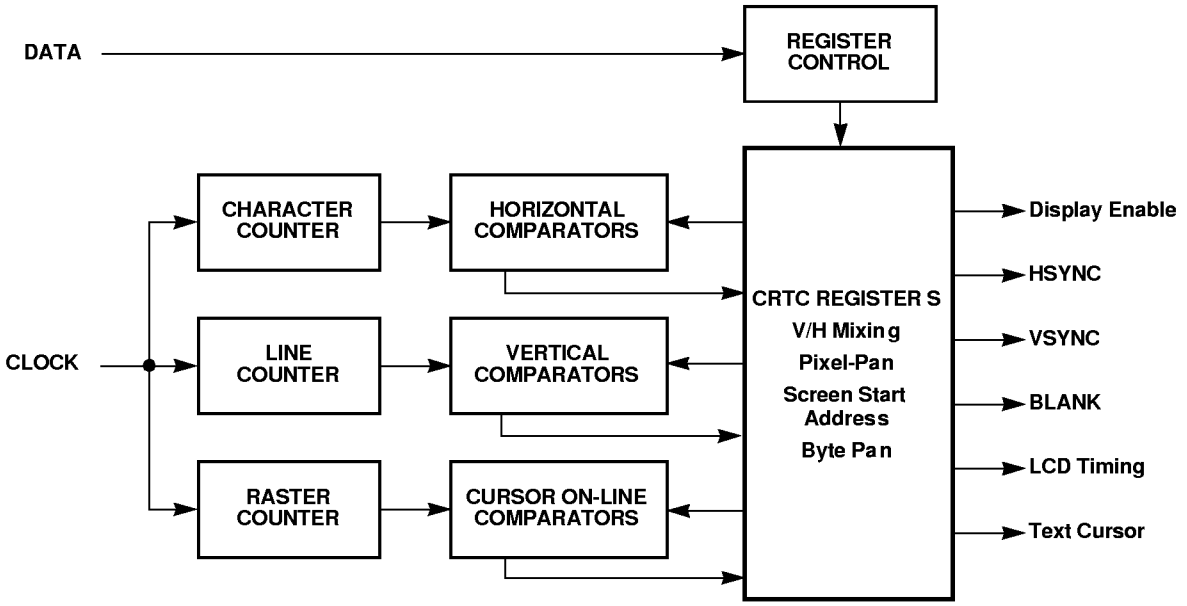


Figure 3-5. CRT Controller Functional Block Diagr am

3.2.12 Hardware Cursor

The hardware cursor replaces the software mouse pointer commonly used by GUI applications. The hardware cursor eliminates the need for application software to save and restore the display data as the mouse pointer position changes. The application software typically initializes the hardware cursor once, and from that point it needs only to update the cursor (x,y) position to move the cursor on the display.

The hardware cursor offers a smoothly moving mouse pointer with improved performance, as compared to a software cursor. The hardware cursor is always displayed on top of graphics, video, or the hardware icons.

The hardware cursor consists of either 64 × 64 two-bit pixels or 32 × 32 two-bit pixels. Each pixel in the hardware cursor can be either transparent or one of two colors from an 18-bit palette.

The hardware cursor's palette is stored in the extended palette, such that it may be different from the VGA color palette. The first bit of each pixel in the hardware cursor defines whether or not the pixel is transparent. If the pixel is not transparent, the second bit defines the pixel's color. The second bit selects one of two 18-bit colors in the extended palette.

The following types of 2-bit hardware cursor patterns can be loaded into upper display memory:

- 64 × 64 hardware cursor patterns — up to 8 patterns
- 32 × 32 hardware cursor patterns — up to 32 patterns

After the hardware cursor patterns are loaded into upper display memory, application programs can quickly select one pattern as the active cursor pattern. The hardware cursor is available in all modes except text modes and graphics mode 13h. Note that the hardware cursor is supported only in 1× video clocking modes. For more information, refer to Appendix B.

3.2.13 Hardware Pop-up Icons

The CL-GD7541/GD7543 provides hardware pop-up icons for displaying small, on-screen symbols that indicate system status (for example, a battery 'fuel gauge'). These hardware icons are stored in upper display memory and can be displayed at the touch of a key. The hardware icons are independent of the graphics mode being used.

The CL-GD7541/GD7543 supports two hardware icon modes:

Hardware Icon Mode 1

Up to four icons, each 64 × 64 pixels in size, can be displayed simultaneously in a vertical column. Each icon is independently controlled for color (up to four colors or three colors plus transparency). Each icon can be expanded either horizontally by pixel doubling, vertically by scanline doubling, or both horizontally or vertically to a maximum size of 128 × 128 pixels per icon.

- When one of the icons is doubled vertically, that icon extends down, which forces the icons below it down.
- When one of the icons is doubled horizontally, that icon expands to the right.
- Each of the four icons is allocated two memory maps. (A total of eight hardware icon memory maps can be stored in display memory.)

Hardware Icon Mode 2

One 64 × 64 pixel hardware icon, from a menu of eight hardware icon memory maps, can be displayed. Each icon is independently controlled for color (up to four colors or three colors plus transparency) and for all other icon attributes (for example, blink, horizontal and vertical doubling, icon enable, and memory map selection).

Hardware icon(s) are supported in all text and graphics modes, except 24-bit/pixel modes with a3× clock, 16-bit/pixel modes with a 2× clock, and interlaced modes. Hardware icon(s) are independent of the hardware cursor. When both a hardware cursor and hardware icon(s) are displayed, the hardware cursor passes on top of the hardware icon(s). The CL-GD7541/GD7543 priority of display overlays is as follows:

- Hardware cursor — always displayed on to p
- Hardware icon
- MotionVideo™ Window data, VGA graphics, or text dat a

3.2.14 Color Palett e

The color palette consists of a 256 18-bit-word CLUT (color lookup table). Each 18-bit word consists of three 6-bit values, one for each primary color (red, green, and blue). The 18-bit word defines one of 2^{18} or 262,144 (referred to as '256K') colors. The CLUT converts an 8-bit color code that specifies the color of a pixel into an 18-bit value, such that 256 simultaneous colors are displayed from a palette of 256K colors. Refer to Figure 3-6.

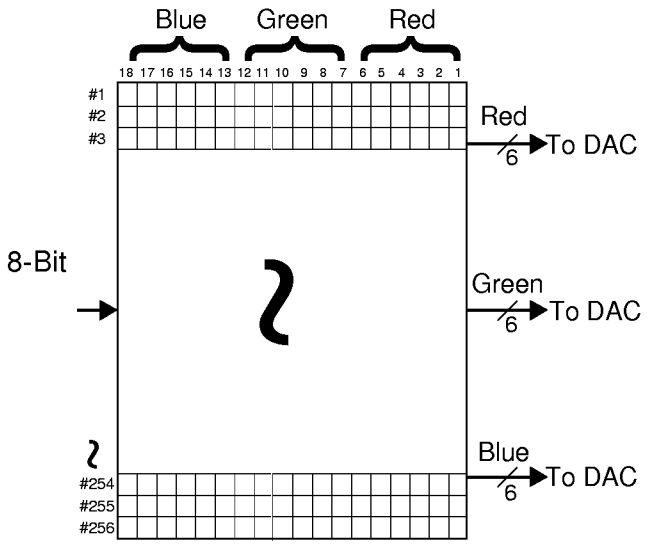


Figure 3-6. Color Lookup Tabl e

The CLUT contents are accessed through its 8-bit-wide host interface. An 8-bit address value applied to the pixel-address inputs defines the memory location for reading an 18-bit color data word from the CLUT. An internal synchronizing circuit allows the color value accesses to be completely asynchronous to the pixel display operation. Special display operations, such as flashing objects and overlays, are possible because the palette incorporates a pixel word mask to allow the incoming pixel address to be altered. As a result, changes to the contents of the CLUT can be made immediately. The CLUT has anti-sparkle circuitry to reduce random noise on the display during CPU accesses to the palette.

Direct-Color and True-Color Modes

In addition to graphics modes that use the 256×18 CLUT, the CL-GD7541/GD7543 supports the following Direct-Color and True-Color modes, which are useful in graphics and multimedia applications:

- **5-5-5 RGB 32K Direct-Color Mode.** This mode bypasses the CLUT. Each pixel is represented by 15 bits, consisting of five bits each of red, green, and blue color information to provide 32,768 (2^{15}) simultaneously displayed colors.
- **5-6-5 RGB 64K Direct-Color Mode.** This mode bypasses the CLUT. Each pixel is represented by 16 bits, consisting of five bits of red, six bits of green, and five bits of blue color information to provide 65,536 (2^{16}) simultaneously displayed colors.

  NOTE: Both the CL-GD7541 and the CL-GD7543 support the 5-6-5 mode in the graphics mode.
- **8-8-8 RGB 16M True-Color Mode.** This mode bypasses the CLUT. Each pixel is represented by 24 bits, consisting of one byte each of red, green, and blue color information to provide 16,777,216 (2^{24}) simultaneously displayed colors.

For a block diagram showing the above-mentioned modes bypassing the CLUT, refer to Figure 3-7. For more information on true-color modes, refer to Appendix E.

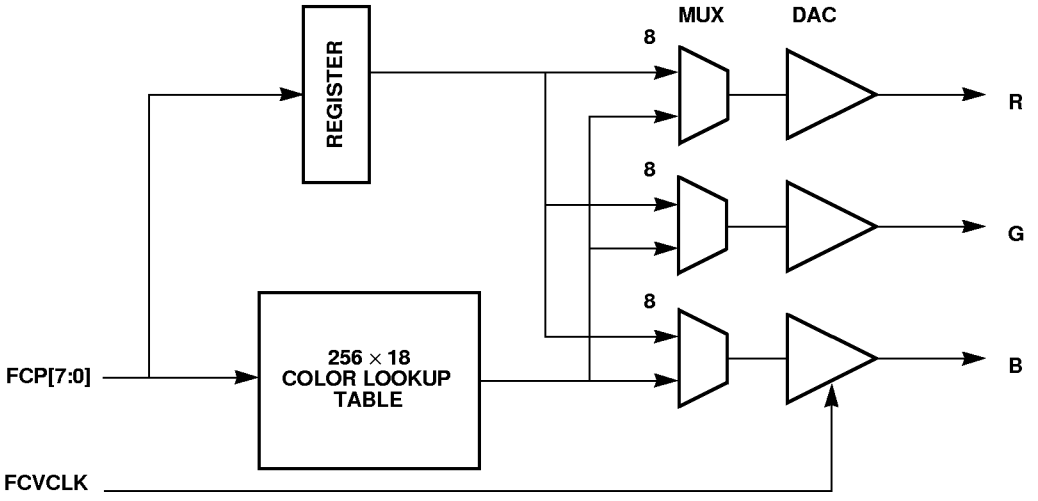


Figure 3-7. 256-Color Direct-Color Palette DAC

Monochrome STN LCDs

On monochrome STN LCDs, the CL-GD7541/GD7543 produces up to 256 grayscales. For more information on grayscales, refer to Section 3.2.21 and Section 3.2.24.

For graphics modes, the following outputs are converted to either 64 or 256 grayscales — the 6-6-6 RGB (from the CLUT), the 5-5-5 RGB, 5-6-5 RGB, and the 8-8-8 RGB. The conversion to grayscales takes place by programming Extension register CR1E[7:6] for one of the following three options:

- NTSC weighting (30% red + 59% green + 11% blue)
- Green-only
- Attribute controller (6 bits)

For text modes, pixel data is converted into grayscales as follows:

- 4-bit pixel data (4 bits for foreground/background color) is directly converted into 16 grayscales.
- 6-bit pixel data (the lower 6 of 8 bits packed-pixel) is directly converted into 64 grayscales.

The CL-GD7541/GD7543 provides the following types of text contrast enhancements as well:

- General Contrast Enhancement:
  - If the background color is *greater* than the foreground color, the foreground color is set to 0, and the background color remains unchanged.
  - If the background color is *less* than the foreground color, the background color is set to 0, and the foreground color remains unchanged.
- Foreground-Only Contrast Enhancement:
  - If the background color is *greater* than the foreground color, the foreground color is set to 0 and the background color remains unchanged.
  - If the background color is *less* than the foreground color, the foreground color is set to 7 and the background color remains unchanged.

The CL-GD7541/GD7543 provides reverse video:

- For text modes by programming Extension register CR1E[5]
- For graphics modes by programming Extension register CR1E[4]

3.2.15 Extended Palette RAM

The extended palette RAM provides 18-bit/pixel data (6-6-6 RGB) for the following functions:

- Hardware cursor
- Hardware icon
- Overscan border color

As shown in Table 3-1, the extended palette RAM enables the colors of the hardware cursor, hardware icons, and the border to be programmed independently from the standard 256× 18 VGA CLUT.

Table 3-1. Extended Palette RAM

I/O Address	Physical RAM Location	Function
X0h	256	Hardware cursor background color
XFh	257	Hardware cursor foreground color
X2h	258	Fix color of overscan (the border)
X3h	259	Hardware icon color #0 (not for 3-colors-and-transparent mode)
X4h	260	Hardware icon color #1
X5h	261	Hardware icon color #2
X6h	262	Hardware icon color #3
XAh	266	Used by VGA BIOS
XBh	267	Used by VGA BIOS
XCh	268	Used by VGA BIOS
XDh	269	Used by VGA BIOS
XEh	270	Used by VGA BIOS

3.2.16 Triple DAC

The DAC includes three 8-bit DACs (digital-to-analog converters). The DAC outputs drive the red, green, and blue color display inputs to the CRT. The DAC outputs are designed to produce a 0.7-volt peak-white amplitude when supplied with a reference current (IREF). The IREF current is supplied with the circuit shown in the IREF pin description in Chapter 2. For all IREF values and output loading:

- $V_{Black\ Level} = 0$ volts
- $V_{Maximum\ White} = 0.7$ volts

To detect the type of CRT monitor that is connected, two sense methods can be used — analog and digital. With the analog sense method, the CL-GD7541/GD7543 places specific color values on the RGB lines and then compares the resulting voltage level against a known internal reference voltage.

For information on CRT-only modes, refer to Section 4.1.

3.2.17 MotionVideo™ Acceleration (CL-GD7543 Only)

The MVA™ (MotionVideo™ Acceleration) provides cost-effective, high-quality video-playback hardware acceleration for .AVI (audio-video interleaved) file formats associated with Microsoft® Video for Windows.

Video playback using a VGA controller *without* MVA has a number of limitations:

- The video playback's pixel color depth must be the same as the pixel color depth of the surrounding graphics. For a 24-bit/pixel video playback window, the entire 640 × 480 or 800 × 600 display must operate in 24-bit/pixel modes.
- Pixel performance on a 640 × 480 24-bit/pixel display is very slow, because bandwidth is limited by the 32-bit display memory interface.
- With a 32-bit display memory interface, 800 × 600 and 1024 × 768 24-bit/pixel resolutions are not possible. The display memory interface would require 2 to 3 Mbytes of display memory, with a 64-bit wide display memory interface, which is not economical in mainstream notebooks.
- Mixing video and graphics functions such as scaling in software introduces additional overhead and exacerbates the display memory bottleneck.

When playing back video while using a VGA controller *without* the MVA advantage, the above limitations result in the following disadvantages:

- The video playback window's pixel color depth is low (typically 8 bits/pixel).
- The screen resolution is small (typically 160 × 120 or 320 × 240).
- The frame rate is low (typically 15 frames per second).
- The graphics performance is sluggish.
- The display memory requirements are high.

3.2.17.1 Video Playback (CL-GD7543 Only)

The MVA provides a MotionVideo Window, consisting of one of the color space formats in Section 3.2.17.2, on top of standard/extended VGA modes. The pixel color depth of the MotionVideo Window can be different from the pixel color depth of the surrounding graphics. The internal color space converter may be used to expand 4:2:2 YUV data to 24-bit RGB. For example, Figure 3-8 shows a 320 × 240 video clip (5-5-5 RGB) that is displayed as a 640 × 480 15-bit/pixel MotionVideo Window on a 256-color 800 × 600 display. This video playback can be accomplished using just 1 Mbyte of display memory.

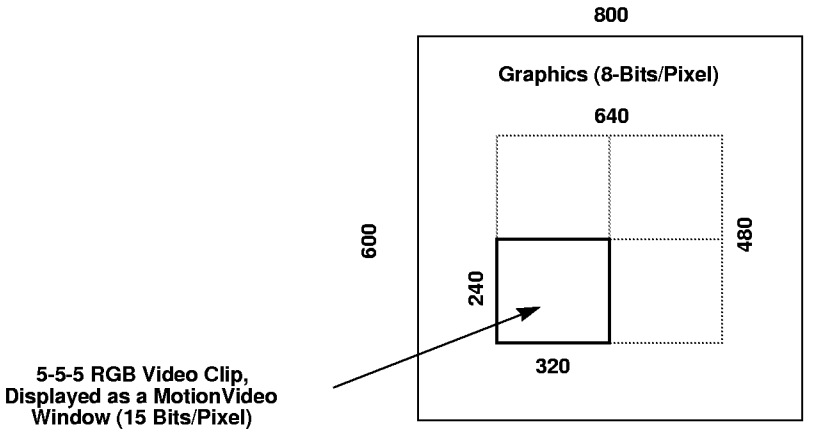


Figure 3-8. MotionVideo Window

For video playback, the hardware scaling feature may be used to double the MotionVideo Window horizontally, vertically, or both horizontally and vertically. For display, the integrated YUV:RGB color space converter converts 4:2:2 YUV to 8-8-8 RGB. For more information, refer to Section 3.2.17.4.

3.2.17.2 MotionVideo™ Window (CL-GD7543 Only)

MVA creates a MotionVideo Window (MVW) that utilizes off-screen memory. The MVW is positioned on top of the VGA graphics mode data, and the hardware icons and hardware cursor are displayed on top of the MVW.

The MotionVideo Window functions as an overlay image that can be positioned anywhere on the display. The position and size of the MotionVideo Window are programmable by using Extension registers CR3X, with 8-pixel horizontal resolution and 1-scanline vertical resolution. The MotionVideo Window can be displayed with SimulSCAN on both CRT monitors and LCDs that have 640 × 480 or 800 × 600 resolutions.

With MVA, the display memory becomes a multi-format display memory. As a result, as listed below, different color pixel depths and data formats can be mixed in the MotionVideo Window display.

- The color pixel depth of the MotionVideo Window is independent of the color pixel depth of the surrounding graphics.
  - For example, a MotionVideo Window may operate in a 24-bits/pixel mode, while the surrounding graphics operate in a 8-bits/pixel mode (even in planar modes).
- The data format of the MotionVideo Window is independent of the data format of the surrounding graphics.
  - For example, 4:2:2 YUV video data can be stored with 8-bit RGB graphics data in display memory. (The 4:2:2 YUV format is compressed, since 4:2:2 uses 16 bits/pixel on average to provide the same color quality as 24-bit/pixel RGB modes.)

If the display color resolution is less than 24 bits/pixel, the MVA dithering algorithm can be used by programming Extension registers CR4D and CR4E to increase the displayed pixel color depth to 24 bits/pixel, independently of the graphics color resolution. This mixing of color pixel depth modes and data formats provides high-quality video playback, along with high-performance graphics, while minimizing display memory requirements.

The video data of the MotionVideo Window is stored in MotionVideo memory, which is located in any available contiguous off-screen display memory space. As shown in Figure 3-9, MotionVideo memory is located as follows:

- MotionVideo memory is located *above* graphics memory (where pixel data for standard and extended VGA modes is stored).
- MotionVideo memory is located *below* the last 16 Kbytes of display memory (where data for the hardware cursor and the hardware icons is stored).

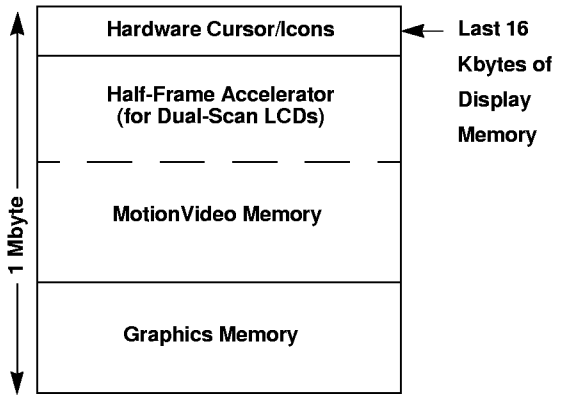


Figure 3-9. MotionVideo™ Memory, Stored as Part of Display Memory

During display refresh, data is accessed from either MotionVideo memory or graphics memory on a pixel-by-pixel basis, with 8-pixel alignment. Note that no double accesses to display memory are required, alleviating the display memory bandwidth bottleneck. Any data format supported by MVA can be displayed. Furthermore, new data formats can be added as needed.

The MotionVideo Window supports the following color space formats:

- 24-bit/pixel RGB 8-8-8
- 16-bit/pixel 4:2:2 YUV linear (Y0UY1V)
- 16-bit/pixel RGB 5-6-5
- 16-bit/pixel RGB 5-5-5
- 8-bit/pixel RGB 3-3-2 through the palette
- 8-bit/pixel RGB 3-3-2 direct

For a description of 16-bit/pixel and 24-bit/pixel RGB formats, refer to Section 3.2.14.

The MVA optimizes display memory bandwidth while minimizing display memory requirements. As a result, high-quality MVWs may be displayed with high-resolution graphics modes by using only 1 Mbyte of display memory.

MVWs can use several aspect ratios, and they are not limited to a 4:3 aspect ratio. However, one MVW limitation is the amount of display memory available for MotionVideo memory, as demonstrated in the following equation.

$$MVWM = DMEM - GMEM - ACEL - 16\ Kbytes \qquad \textbf{Equation 3-1}$$

where

MVWM = MotionVideo Window memory
DMEM = Total available memory
GMEM = Memory required for graphics
ACEL = Memory required to support the half-frame accelerator required for dual-scan STN LCDs
16 Kbytes = Memory reserved for hardware cursor and icon

MVA, which can be used in full-screen configurations, enables the creation of special graphics modes (for example, 24-bit/pixel with a 1× dot clock).

Table 3-2 and Table 3-3 show the minimum MCLK needed for various MVW playback configurations.

Note the following:

- With a 640 × 480 graphics display mode (on either a color TFT LCD, STN LCD, or a CRT) the MVW start address is 16 Kbytes aligned. The following MVWs can be displayed:
  - A 640 × 480 (full-screen) MVW, with 8, 16, or 24 bits/pixel format. SGDMs (surrounding graphics display modes) can be 8 or 16 bits/pixel.
  - A 320 × 240 MVW, with any bits/pixel format. SGDMs can be 8, 16, or 24 bits/pixel.
- With an 800 × 600 color graphics display mode (on either a color TFT LCD or a CRT), the following MVWs can be displayed:
  - A 640 × 480 MVW, with 8 bits/pixel format. SGDMs can be 8 bits/pixel.
  - A 640 × 480 MVW, with 16 bits/pixel format.
  - A 320 × 240 MVW, with 8 or 16 bits/pixel. SGDMs can be 8 bits/pixel.
  - MVWs with SGDMs of 24 bits/pixel are not possible because of the display memory size and the 32-bit memory interface.
- With a 800 × 600 color dual-scan STN LCD, MVWs are restricted due to memory bandwidth limitations.

The MVW pixel color depth corresponds to the formats above. The MVW resolution is for the source data. Using hardware scaling, this resolution can be doubled horizontally and vertically on the display without a corresponding decrease in performance. For more information, refer to Section 3.2.17.

Table 3-2. Recommended MCLKs for 800 × 600 × 8-Bit/Pixel MVWs (CL-GD7543 Only)

Resolution	Display Type	MotionVideo™ Window			
		.AVI Source File Resolution	RGB (Bits/Pixel)	MVW Size	
				Minimum MCLK for 1× Scaling	Minimum MCLK for 2× Scaling
800 × 600 × 8 bits/pixel	Color TFT LCD	160 × 120	8	50 MHz	50 MHz
			16	50 MHz	50 MHz
			24	SW	55.4 MHz
		320 × 240	8	50 MHz	50 MHz
			16	50 MHz	50 MHz
			24	SW	55.4 MHz
	Color Dual-scan STN LCD	160 × 120	8	50 MHz	50 MHz
			16	SW	50 MHz
			24	SW	SW
		320 × 240	8	50 MHz	50 MHz
			16	SW	50 MHz
			24	SW	SW
	CRT monitor only (60 Hz screen refresh)	160 × 120	8	50 MHz	50 MHz
			16	SW	50 MHz
			24	SW	55.4 MHz
		320 × 240	8	50 MHz	50 MHz
			16	SW	50 MHz
			24	SW	55.4 MHz

NOTE: "SW" indicates that video playback is supported through the standard software graphics interface (that is, a non-MVA display control interface) .

Table 3-3. Recommended MCLKs for 640 × 480 × 8-Bit/Pixel MVWs (CL-GD754 3 Only)

Resolution	Display Type	MotionVideo™ Window			
		.AVI Source File Resolution	RGB (Bits/Pixel)	MVW Size	
				Minimum MCLK for 1× Scaling	Minimum MCLK for 2× Scaling
640 × 480 × 8 bits/pixel	Color TFT LCD	160 × 120	8	50 MHz	50 MHz
			16	50 MHz	50 MHz
			24	SW	50 MHz
		320 × 240	8	50 MHz	50 MHz
			16	50 MHz	50 MHz
			24	SW	50 MHz
	Color Dual-scan STN LCD	160 × 120	8	50 MHz	50 MHz
			16	50 MHz	50 MHz
			24	SW	50 MHz
		320 × 240	8	50 MHz	50 MHz
			16	50 MHz	50 MHz
			24	SW	50 MHz
	CRT monitor only (75 Hz screen refresh)	160 × 120	8	50 MHz	50 MHz
			16	50 MHz	50 MHz
			24	SW	53.9 MHz
		320 × 240	8	50 MHz	50 MHz
			16	50 MHz	50 MHz
			24	SW	53.9 MHz

NOTE: "SW" indicates that video playback is supported through the standard software graphics interface (that is, a non-MVA display control interface) .

3.2.17.3 Repositioning the MotionVideo™ Window / Hardware Scaling (CL-GD7543 Only)

By programming Extension registers CR33 through CR39, the MotionVideo Window can be repositioned anywhere on the display. By programming Extension register CR3C, the 320 × 240 MotionVideo™ Window can be expanded so that the 320 × 240 window can be doubled to 640 × 480 on 800 × 600 LCDs.

As explained in Table 3-4, hardware scaling provides a programmable 2× magnification by doubling pixels horizontally only, vertically only, or horizontally and vertically simultaneously.

Table 3-4. Programming for Hardware Scaling

Type of MVW Hardware Scaling	Extension Register
Horizontal pixel doubling	CR3C[7] = 1
Vertical pixel doubling	CR3C[6] = 1
Horizontal and vertical pixel doubling	CR3C[7] = 1 and CR3C[6] = 1

3.2.17.4 YUV-to-RGB Color Space Converter (CL-GD7543 Only)

The integrated YUV-to-RGB color space converter supports two types of YUV-to-RGB algorithms, which are selected by Extension register bit CR36[6]:

- Format 1 (standard):
  - R = Y + 1.375V
  - G = Y – 0.375U – 0.7V
  - B = Y + 1.75U
- Format 2:
  - R = Y + V
  - G = Y – 0.5U – 0.5V
  - B = Y + U

Extension register bit CR36[5] determines whether the YUV-to-RGB conversion uses either the 2's complement U,V formats (which is useful for Philips® SAA9051 TV decoders) or excess 128 format.

3.2.18 Feature Connector

The following CL-GD7541/GD7543 pins provide standard VGA feature connector functionality:

- FCP[7:0]: bidirectional 8-bit data port
- FCDCLK: dot clock output
- FCVCLK: video clock input
- FCESYNC#: enables input of synchronization signals that enable HSYNC, VSYNC, and FCBLANK# outputs
- FCBLANK#: either a blanking signal output, or an input that forces RGB outputs to zero current
- OVRW#: overlay window output

The CL-GD7541/GD7543 supports the Feature Connector, such that video data can be input and displayed as an video overlay window. The Baseline Output mode (8-bit indexed, 1 pixel per clock), is directly supported. This mode is the mode that most current off-the-shelf video overlay boards work with to display video on a CRT.

The CL-GD7541/GD7543 supports 8-bit/pixel indexed data (a Feature Connector extended mode). The 8-bit data is input either by using both phases of the clock or by using a 2× clock. An 8-bit value, stored in the Color Key Compare register GRC, is compared to the video data input from FCP[7:0] on a pixel-by-pixel basis. A match causes the graphics data of the pixel to be replaced with the video data input

3.2.19 NTSC/PAL Out

The CL-GD7541/GD7543 outputs digital RGB data in an interlaced format to an external analog TV encoder (for example, an Analog Devices AD720 encoder or a Motorola MC1377 encoder). Only minimal additional logic circuitry is required. With the addition of an analog encoder, a portable computer can output the following signals for use with a standard TV monitor or VCR (video cassette recorder):

- NTSC (National Television Standards Committee) signals
- PAL (phase alternation line-rate) signals

The CL-GD7541/GD7543 can operate in a locked interlaced mode. In this case, the LCD support shadowing mechanism (which shadows Horizontal and Vertical CRTC registers) is used to prevent an application from changing any part of the CRT Controller setup, including the dot clock frequency. Horizontal and vertical display enable is open to the application.

The CL-GD7541/GD7543 outputs analog RGB, a composite synchronization signal, an NTSC/PAL standard select signal, and TV-On (a power-management signal). Due to differences in the standards between PC displays and CRT monitors, the NTSC/PAL output is limited to graphics modes 1h, 3h, 12h, 13h, 5Fh, and 64h. (A special windows driver allows use of graphics mode 5Fh for Windows®).

Because televisions use interlaced display refresh and have an aspect ratio different than many standard VGA modes, support for additional VGA modes was not included in the CL-GD7541/GD7543, as such support would result in unusable displays. The NTSC/PAL functionality provided in the CL-GD7541/GD7543 is targeted primarily for entertainment use, for display of graphic images, and within certain guidelines, for presentations. However, this functionality was not intended as a direct replacement for a PC CRT. For more information on NTSC/PAL functionality, refer to the application note “Driving NTSC/PAL Display Signals” in the *CL-GD754X Application Book*.

3.2.20 Half-Frame Accelerator

The CL-GD7541/GD7543 integrates a half-frame accelerator, required by dual-scan LCDs. With the half-frame accelerator, a dual-scan LCD can run at twice the CRT refresh rate. The CL-GD7541/GD7543 provides simultaneous CRT and LCD display operation (SimulSCAN) for the following dual-scan LCDs:

- 640 × 480 STN dual-scan LCDs: the half-frame accelerator provides all the standard VGA modes and extended graphics modes up to 640 × 480
- 800 × 600 STN dual-scan LCDs: the half-frame accelerator provides all the standard VGA modes and extended graphics modes up to 800 × 600

3.2.21 LCD Interface

The CL-GD7541/GD7543 interfaces directly with a variety of LCDs (and CRTs, for SimulSCAN operations). These LCDs include the following:

- Monochrome 640 × 480 dual- and single-scan STN LCDs
- Color 640 × 480 and 800 × 600 dual- and single-scan STN LCDs (with 8- and 16-bit interfaces)
- Color 640 × 480 and 800 × 600 TFT LCDs with the following interfaces:
  - 9-bit (3 bits each for red, green, blue)
  - 12-bit (4 bits each for red, green, blue)
  - 18-bit (6 bits each for red, green, blue)
  - 24-bit (8 bits each for red, green, blue)

3.2.22 LCD Resolution Compensation

With its LCD resolution compensation, the CL-GD7541/GD7543 allows a spectrum of PC applications, originally written for analog CRT monitors that use various VGA modes, to run transparently on LCDs. This LCD resolution compensation feature is necessary, in that unlike CRTs, LCDs have a fixed horizontal and vertical resolution. As a result, when a PC application is selected, VGA modes that are concurrently selected can use a resolution that is lower than the fixed resolution of the LCD. Consequently, unless LCD resolution compensation is used, a section of the LCD is left blank.

For example, when VGA text mode 3, which consists of 400 lines, is displayed on a 640× 480 LCD that does not have use of LCD resolution compensation, 80 blank lines remain at the bottom of the LCD. (For a list of various horizontal and vertical resolutions for standard VGA modes, refer to Chapter 4.)

To remove blank space, the CL-GD7541/GD7543 LCD resolution compensation presents these options:

- Automatic expansion of VGA text modes
- Custom fonts to replace standard VGA fonts
- Horizontal centering of displayed lines
- Horizontal expansion of VGA graphics modes
- Vertical centering of displayed lines
- Vertical expansion of VGA graphics modes

Resolution Compensation for 640 × 480 LCDs

For 640 × 480 LCDs, the CL-GD7541/GD7543 provides the following LCD resolution compensation options to display lower-resolution VGA text and graphics:

- **Automatic-Text Expansion.** Automatic-text expansion of a VGA font makes the font consistent across the LCD and eliminates any breaks or artifacts in fonts that connect to adjacent fonts.
  - The 9-pixel-wide VGA fonts (used in the popular VGA text modes 3h and 7h) are horizontally displayed as 8-pixel-wide fonts. As a result, 80 characters fill all 640 pixels across.

  The following methods automatically vertically expand VGA character text fonts to 19 pixels. As a result, 475 lines of the LCD's 480 vertical lines are filled.

  - The 8 × 8 (200-line) VGA fonts are double-scanned, vertically expanding the font to equal 16 pixel lines. An extra top pixel line and two extra bottom pixel lines are added to each character row of the font, further vertically expanding the font to equal 19 pixel lines.
  - For 8 × 14 (350-line) VGA fonts, two extra top pixel lines and three extra bottom pixel lines are added to each character row to vertically expand the font to 19 pixel lines.
  - For the 8 × 16 (400-line) VGA fonts, an extra top pixel line and two extra bottom pixel lines are added to each character row to vertically expand the font to 19 pixel lines.
- **Custom Fonts.** Standard VGA fonts (8 × 8, 8 × 14, and 9 × 16) can be replaced with a custom 8 × 19 font to fill 640 × 475 pixels on a 640 × 480 LCD.
- **Vertical Centering of Displayed Lines**
  - If automatic-text expansion or a custom font is used, the 475 lines that result can be vertically centered on the 480-line LCD.
  - If automatic-text expansion or a custom font is not used, 200-, 350-, or 400-line VGA text or graphics modes can also be vertically centered on the 480-line LCD.
- **Vertical Graphics Expansion.** On a 640 × 480 LCD, vertical graphics expansion can be used to run PC application programs that use lower-resolution VGA graphics modes.
  - The 200-line VGA graphics modes are vertically expanded to 475 lines by expanding every 8 lines to 19 lines, using a pattern of 2,2,3,2,2,3,2,3 (double- and triple-scan).
  - The 350-line VGA graphics modes are vertically expanded to 475 lines by expanding every 14 lines to 19 lines using a pattern of 1,1,2,1,1,2,1,2,1,1,2,1,1,2 (single- and double-scan).

  Popular GUI-based applications, such as Windows or OS/2, use a CL-GD7541/GD7543 driver that selects the proper VGA graphics mode (for example, 2-, 16-, 256-, 32K-, 64K-, or 16M-color modes) to run applications at the full resolution of the 640 × 480 LCD.

Resolution Compensation for 800 × 600 LCDs

For 800 × 600 LCDs, the CL-GD7541/GD7543 provides the following LCD resolution compensation options to display lower-resolution VGA text and graphics.

NOTE: Resolution compensation applies to modes less than or equal to 8 bits/pixel .

- **Automatic-Text Expansion.** Automatic-text expansion of a VGA font makes the font consistent across the LCD and eliminates any breaks or artifacts in fonts that connect to adjacent fonts.
  - The 9-pixel-wide VGA fonts (used in the popular VGA text modes 3h and 7h) are horizontally displayed as 10-pixel-wide fonts, by replicating the last pixel once. As a result, 80 characters fill all 800 pixels across.

  The following methods vertically expand the VGA character fonts .
  - The 8 × 8 (200-line) VGA fonts are triple-scanned, vertically expanding the font to equal 24 pixel lines. As a result, all of the LCD's 600 vertical lines are filled .
  - For the 8 × 14 (350-line) VGA fonts, every odd scanline is replicated to vertically expand the font to 21 lines. As a result, 525 lines of the LCD's 600 vertical lines are filled .
  - For the 8 × 16 (400-line) VGA fonts, every odd scanline is replicated to vertically expand the font to 24 lines. As a result, all of the LCD's 600 vertical lines are filled .
- **Custom Fonts.** Standard VGA fonts (8 × 8, 8 × 14, and 9 × 16) can be replaced with a custom 10 × 24 font to fill all 800 × 600 pixels on a 800 × 600 LCD.
- **Horizontal Centering**
  - VGA text modes that are 720 pixels wide can be horizontally centered, leaving 40 blank pixels each on the left and right sides of the 800 × 600 LCD display.
  - VGA text modes that are 640 pixels wide can be horizontally centered, leaving 80 blank pixels each on the left and right sides of the 800 × 600 LCD display .
- **Horizontal Graphics Expansion.** VGA graphics modes that are 640 pixels wide can be horizontally expanded to 800 pixels by replicating every fourth pixel. (However, currently this expansion is not available for VGA graphics modes that have either 2× dot clocks with 16-bits/pixel or 3× dot clocks with 24-bits/pixel).
- **Vertical Centering**
  - If automatic-text expansion or vertical graphics expansion is used, the 525 lines that result can be vert i-cally centered on the 600-line LCD.
  - If automatic-text expansion is not used, the 200-, 350-, or 400-line VGA text or graphics modes can also be vertically centered on the 600-line LCD .
- **Vertical Graphics Expansion.** On a 800 × 600 LCD, vertical graphics expansion can be used to run PC application programs that use lower-resolution VGA graphics modes .

  For example, VGA graphics modes that are :
  - 350 lines are vertically expanded to 525 lines by replicating all odd scanlines.
  - 400 lines are vertically expanded to 600 lines by replicating all odd scanlines .
  - 480 lines are vertically expanded to 600 lines by replicating every fourth scanline.

  Popular GUI-based applications, such as Windows or OS/2, use a CL-GD7541/GD754 3 driver that selects the proper VGA graphics mode (for example, 2-, 16-, 256-, 32K-, or 64K-color modes) to run the application programs at the full resolution of the 800 × 600 LCD.

3.2.23 Frame Rate Modulation

The CL-GD7541/GD7543 employs a new, improved FRM (frame rate modulation) algorithm to create grayscales on monochrome and color STN LCDs. Over multiple frames in time, the FRM algorithm modulates the 'on' and 'off' times of individual pixels in the LCD, such that the eye integrates the superimposed pixels as perceptible grayscales.

Proprietary techniques reduce or eliminate entirely the grayscale artifacts (for example, flicker, noise and pattern motion). On state-of-the-art STN LCDs with fast response times of approximately 100 ms, the result is an outstanding display quality.

The CL-GD7541/GD7543 provide three FRM options:

- **16-frame FRM.** This FRM option modulates the pixel over 16 frames in time to create 16 shades for each red, green, and blue (RGB) primary color, for 4,096 (16^3) colors total. This option is intended to support STN LCDs currently available and in development, including STN LCDs with very fast response times of approximately 100 ms. This algorithm allows masking of undesirable grayscales (that is, those that exhibit flicker or pattern motion).
  - — By setting register RBX[4], grayscales 7 and 9 can be converted to grayscales 6 and 8, respectively.
  - — By setting register RBX[3], grayscales 1 and 15 can be converted to grayscales 0 and 16, respectively.
  - — If two grayscales are masked, the FRM algorithm produces 2,744 (14^3) colors.
  - — If four grayscales are masked, the FRM algorithm produces 1,728 (12^3) colors.
- **8-frame FRM.** This FRM option modulates the pixel over 8 frames in time to create 8 shades for each RGB primary color, for 512 (8^3) colors total. This option is intended to reduce flicker and 'submarining' (that is, the temporary disappearance of the mouse pointer) on future STN LCDs that may have response times that are too fast for the 16-frame FRM option.
- **4-frame FRM.** This FRM option modulates the pixel over 4 frames in time to create 4 shades for each RGB primary color, for 64 (4^3) colors total. This option is intended to reduce flicker and 'submarining' on future STN LCDs that may have response times too fast for both the 16- and 8-frame FRM options.

In summary, the FRM algorithm produces 2, 3, or 4 bits of color depth for each RGB primary color on STN LCDs.

- To add up to 6 bits of color depth to each primary color, the dithering engine can be used with an FRM algorithm.
- To add up to 8 bits of color depth to each primary color (or 256 grayscales for each primary color) for a total of 16M colors, the dithering engine can be used with only a 4-frame FRM algorithm.

3.2.24 Dithering Engine

The dithering engine increases the number of perceived colors displayed on the LCD and/or CRT, relative to what the display can physically produce without dithering.

A proprietary intercalating spatial dithering technique preserves the spatial resolution of the displayed image. For example, when a 640 × 480 resolution image is dithered, the resolution is maintained instead of being reduced to 320 × 240.

The dithering engine works by automatically selecting a dithering pattern. As shown in Table 3-5, an increase in the dithering pattern increases the number of displayed bits per RGB primary color, dependent on the color depth of the image.

Table 3-5. Effective Dithering Patterns

Effective Dithering Pattern	Increased Number of Displayed Bits per RGB Primary Color
2 × 1	1 bit
2 × 2	2 bits
4 × 2	3 bits
4 × 4	4 bits
8 × 4	5 bits
8 × 8	6 bits

The dithering engine can automatically add up to 6 bits per primary color, and it can be used for color and monochrome STN LCDs, and TFT LCDs. (By programming register CR4C, this automatic feature may be overridden and the number of bits per primary color limited to a programmable number.)

As shown in Figure 3-1 on page 60, in the data path, the dithering engine is after the LCD resolution compensation, so that dithering is applied to the expanded image.

The dithering engine contains these separate dithering registers:

- Dithering register for standard/extended VGA modes (CL-GD7541/GD7543)
- Dithering register for Video Overlay (CL-GD7541/GD7543)
- Dithering register for MotionVideo Window (CL-GD7543 only)

To render the appropriate colors, the CL-GD7541/GD7543 dynamically switches dithering between the surrounding graphics and the MotionVideo Window. (For more information on the MotionVideo Window, refer to Section 3.2.17.2.)

Table 3-6 shows the number of grayscales that can be displayed on a monochrome STN LCD, by using a combination of FRM and dithering options. As shown in the table, the 4-frame FRM option produces only four grayscales (2 bits/pixel), which is insufficient for displaying 32-, 64-, or 256-grayscale images. Dithering options can automatically add up to 6 bits/pixel depending upon the color depth of the displayed image.

For a display with an image that is:

- 32-grayscale (5 bits), the dithering engine automatically adds 3 bits to the 2 bits produced by the FRM.
- 64-grayscale (6 bits), the dithering engine automatically adds 4 bits to the 2 bits produced by the FRM.
- 256-grayscale (8 bits), the dithering engine automatically adds 6 bits to the 2 bits produced by the FRM.

Table 3-6. Number of Grayscales On Monochrome STN LCDs

Frame-Rate Modulation Option	Effective Dithering		Resulting Image on Monochrome STN LCD That Has :		
	Pattern	No. of Bits	32 Shades of Gray (5 bits)	64 Shades of Gray (6 bits)	256 Shades of Gray (8 bits)
4 frames (2 bits)	None	0	4 (2^2)		
	2 × 1	1	8 (2^3)		
	2 × 2	2	16 (2^4)		
	4 × 2	3	32 (2^5)		
	4 × 4	4	Illegal[a]	64 (2^6)	
	8 × 4	5	Illegal		128 (2^7)
	8 × 8	6	Illegal		256 (2^8)
8 frames (3 bits)	None	0	8 (2^3)		
	2 × 1	1	16 (2^4)		
	2 × 2	2	32 (2^5)		
	4 × 2	3	Illegal	64 (2^6)	
	4 × 4	4	Illegal		128 (2^7)
	4 × 8	5	Illegal		256 (2^8)
16 frames (4 bits)	None	0	16 (2^4)		
	2 × 1	1	32 (2^5)		
	2 × 2	2	Illegal	64 (2^6)	
	4 × 2	3	Illegal		128 (2^7)
	4 × 4	4	Illegal		256 (2^8)

[a] 'Illegal' indicates an illegal combination.

Table 3-7 shows the number of displayed colors on a color STN LCD with various FRM and dithering options. As shown in the table, each FRM/dithering option produces the same number of color shades per primary color as grayscales for monochrome LCDs, as shown in Table 3-6. The total number of colors is equal to 3× the number of color per primary color (RGB). For example, a 4-frame FRM and 8× 8 dithering pattern produces 2^8 (256) grayscales on monochrome STN LCDs, and 2^{24} (16M colors) on color STN LCDs.

Table 3-7. Number of Colors on Color STN LCD s

Primary Color RG B			Resulting Image on Color STN LCD That Has :		
Frame-Rate-Modulation Option	Generated by LC D		32K Colors (15 bits)	256K Colors (18 bits)	16M Colors (24 bits)
	Dithering Pattern	No. of Bits			
4 frames (2 bits)	None	0	64 (2^6)		
	2 × 1	1	512 (2^9)		
	2 × 2	2	4K (2^{12})		
	4 × 2	3	32K (2^{15})		
	4 × 4	4	Illegal[a]	256K (2^{18})	
	8 × 4	5	Illegal		2M (2^{21})
	8 × 8	6	Illegal		16M (2^{24})
8 frames (3 bits)	None	0	512 (2^9)		
	2 × 1	1	4K (2^{12})		
	2 × 2	2	32K (2^{15})		
	4 × 2	3	Illegal	256K (2^{18})	
	4 × 4	4	Illegal		2M (2^{21})
	4 × 8	5	Illegal		16M (2^{24})
16 frames (4 bits)	None	0	4K (2^{12})		
	2 × 1	1	32K (2^{15})		
	2 × 2	2	Illegal	256K (2^{18})	
	4 × 2	3	Illegal		2M (2^{21})
	4 × 4	4	Illegal		16M (2^{24})

[a] 'Illegal' indicates an illegal combination .

Table 3-8 shows the number of colors that various dithering patterns produce on 512-color TFT LCDs. If an image using the standard VGA 18-bit color palette is displayed on a 512-color TFT LCD (that is, which has only a 9-bit color palette), significant banding or contour lines are readily apparent.

Consequently, the dithering engine automatically uses a 4×2 pattern to increase the number of displayed colors from the 3 bits per primary color that the LCD produces to the full 6 bits per primary color to meet the 18-bit VGA color palette requirement upon the displayed image's color depth.

Table 3-8. Number of Colors on 512-Color TFT LCDs

Primary Color RGB Generated by LCD		Resulting Image on Color TFT LCD That Has :		
Dithering Pattern	**No. of Bits**	**32K Colors (15 bits)**	**256K Colors (18 bits)**	**16M Colors (24 bits)**
None	0	512 (2^9)		
2 × 1	1	4K (2^{12})		
2 × 2	2	32K (2^{15})		
4 × 2	3	Illegal[a]	256K (2^{18})	
4 × 4	4	Illegal		2M (2^{21})
8 × 4	5	Illegal		16M (2^{24})

[a] 'Illegal' indicates an illegal combination.

Table 3-9 shows the number of colors various dithering patterns produce on 4K-color TFT LCDs.

Table 3-9. Number of Colors on 4K-Color TFT LCDs

Primary Color RGB Generated by LCD		Resulting Image on Color TFT LCD That Has :		
Dithering Pattern	**No. of Bits**	**32K Colors (15 bits)**	**256K Colors (18 bits)**	**16M Colors (24 bits)**
None	0	4K (2^{12})		
2 × 1	1	32K (2^{15})		
2 × 2	2	Illegal[a]	256K (2^{18})	
4 × 2	3	Illegal		2M (2^{21})
4 × 4	4	Illegal		16M (2^{24})

[a] 'Illegal' indicates an illegal combination.

Table 3-10 shows the number of colors that dithering patterns produce on 256K-color TFT LCDs

Table 3-10. Number of Colors on 256K-Color TFT LCD s

Primary Color RGB Generated by LC D		Resulting Image on Color TFT LCD That Has :		
Dithering Patter n	**No. of Bit s**	**32K Color s (15 bits)**	**256K Color s (18 bits)**	**16M Color s (24 bits)**
None	0	32K (2^{15})	256K (2^{18})	256K (2^{18})
2 × 1	1			2M (2^{21})
2 × 2	2			16M (2^{24})

3.2.25 Frequency Synthesize r

The frequency synthesizer generates all clock frequencies for VGA and extended modes operation. Using a single reference frequency of 14.318 MHz that is supplied from an external TTL-level source, the frequency synthesizer generates two fully programmable clocks — the video clock (VCLK) and the memory clock (MCLK).

For a functional diagram of the frequency synthesizer, refer to Figure 3-10.

- **VCLK**
  - VCLK (video clock) is the fundamental video timing clock that generates all clocks needed for video display timing signals (for example, HSYNC and VSYNC) and for the pixel clock.
  - VCLK *must* be changed to support various display resolutions and refresh rates .
  - The VCLK frequencies are programmed with registers SRB through SRE and SR1B through SR1F.
  - The CL-GD7541/GD7543 supports VCLKs up to 80 MHz at 5 V or 77 MHz at 3.3 V.
- **MCLK**
  - MCLK (memory clock) generates all clocks needed for memory timing signals (for example, RAS#, CAS#).
  - MCLK *must* be optimized for the speed of the display memory used .
  - MCLK frequencies are programmed with register SR1F.
  - For optimal selection of DRAM speeds, the CL-GD7541/GD7543 supports MCLKs up to 60 MHz at 5 V or 50 MHz at 3.3 V.

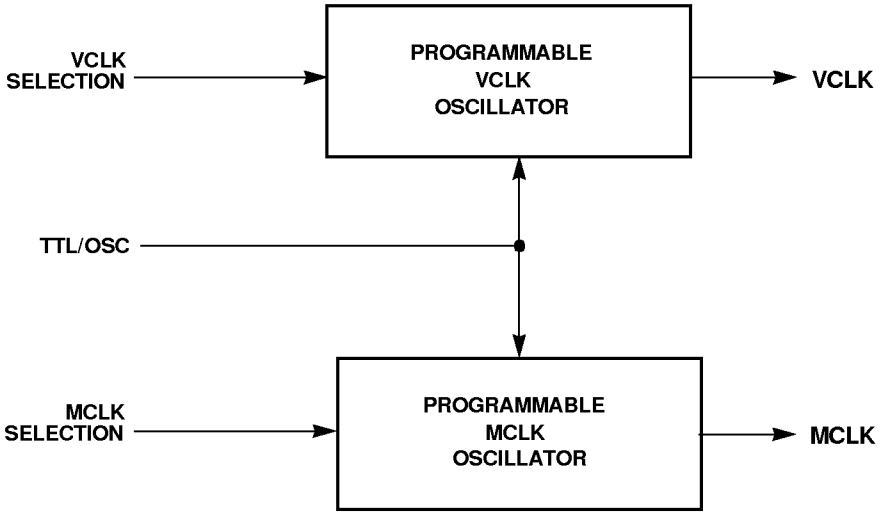


Figure 3-10. Programmable Dual-Frequency Synthesizer Functional Diagra m

3.2.26 Power Management

The CL-GD7541/GD7543 supports power-management techniques to maximize battery life, including:

- **LCD-only power savings.** During LCD-only operations, the video DAC (including its monitor sense comparators) is powered down, and the video clock (VCLK) can be reduced to a level that still minimizes flicker.
- **LCD power-up/down sequence control.** To protect the LCD, the FPVEE and FPVCC output signals control the LCD power-up and power-down sequence. The FPBL output signal controls the LCD backlight enable.

CAUTION: Damage can occur if VEE (the LCD high-voltage power) is applied without VDD (the LCD logic power).

- **Mixed-voltage interfaces.** The host bus, display memory, LCD, and CRT interfaces can each be implemented at either 3.3 or 5 V. The voltages used for each interface can be mixed in any combination.
- **Standby mode.** This mode reduces power consumption by turning off the display while allowing application programs to continue to run normally in the background.
  - Standby is entered either by way of the SBYI pin, by using the internal Standby Counter, or by programming a register.
  - During Standby mode, using proper power sequencing, the LCD and CRT are turned off, the video clock (VCLK) is stopped, and the video DAC is powered down. The CPU can still access and modify the display memory and palette.
  - The Standby mode is exited as it is entered, either by way of the SBYI pin, by using the internal Standby Counter, or by programming a register.
- **Suspend Mode.** This mode reduces power consumption when the system remains inactive for a relatively long period of time, while maintaining the contents of the controller registers, palette, and display memory. Unlike Standby mode, however, during the Suspend mode, applications are suspended and do not continue to run normally in the background.
  - Hardware-controlled Suspend is entered by way of the SUSPI pin. Software-controlled Suspend is entered by setting Extension register CR20[3]. In contrast to hardware-controlled Suspend, software-controlled Suspend allows the CPU to access the internal registers, which requires an active clock and I/O capability, and therefore, more power.
  - During hardware-controlled Suspend, the display is turned off, the video (VCLK) and memory (MCLK) clocks are both stopped, and CPU accesses to the display memory, palette, and I/O registers cease. The CL-GD7541/GD7543 configures display memory for self-refresh or uses the 32-kHz clock for memory refresh.
  - Hardware-controlled Suspend is exited by way of the SUSPI pin. When Suspend mode is exited, any application programs that were previously running can be quickly re-started from the point at which they suspended.
- **VESA Display Power Management.** The CL-GD7541/GD7543 supports the VESA Display Power Management Signaling specification for CRT power management to allow systems to comply with the U.S. Environmental Protection Agency's Energy Star Computer qualifications. For more information, refer to Appendix H.

3.3 Performance

The CL-GD7541/GD7543 is designed with the following performance-enhancing features:

- **BitBLT engine.** The BitBLT engine is used to accelerate GUIs (graphical user interfaces), such as Microsoft Windows.
- **Bus interface choices.** The CL-GD7541/GD7543 provides a choice of bus interfaces for optimum performance:
  - 32-bit VESA VL-Bus
  - '486 local-bus interface
  - PCI bus interface with burst mode
- **CPU interfaces to I/O registers and memory.** For increased performance, the CL-GD7541/GD7543 supports the following CPU interfaces:
  - 32-bit CPU interface to display memory, for faster CPU host access to memory for all modes, including planar modes
  - 16-bit CPU interface to I/O registers, for faster CPU host access to the registers
- **Extended-write modes**
  - For faster CPU write performance, the extended-write modes can be used on 8 pixels at a time in 8- or 16-bit/pixel graphics modes that have packed-pixel addressing.
  - These write modes can be used for faster text writing, pattern filling, and block-moving operations in graphics modes.

    For more information, refer to Appendix D.
- **Hardware cursor.** GUI performance can be improved by using the 32 × 32 or the 64 × 64 hardware cursor.
- **Memory data fast access.** To access display memory fast, the CL-GD7541/GD7543 supports the following:
  - 32-bit display memory data bus
  - DRAM fast-page mode operations
- **Video FIFO.** Video FIFO minimizes memory contention.
- **Zero-wait-state performance.** For faster CPU access for writes to display memory, the CL-GD7541/GD7543 provides zero-wait-state performance and a CPU write buffer.

3.4 RAMDAC Operation

3.4.1 Writing to the Color Lookup Table (CLUT)

To write a color definition to the CLUT, a value specifying an address location in the CLUT is first written to the Write Mode Address register. The color values for the red, green, and blue intensities are then written in succession to the Color Value register. After the blue data bits are latched, the new color data bits are then written into the CLUT at the defined address, and the CL-GD7541/GD7543 automatically increments the Address register.

Since the CL-GD7541/GD7543 increments the Address register after each transfer of data to the CLUT, it is best to write a set of consecutive locations at once. The start address of the set of locations is first written to the Write Mode Address register. The color data bits for each address location are then sequentially written to the Color Value register. After each CPU host transfer of three bytes of color data, the CL-GD7541/GD7543 automatically writes data to the CLUT and increments the Address register.

3.4.2 Reading from the CLUT

To read color data from the CLUT, a value specifying the address location of the data is written to the Read Mode Address register. After the address is latched, data bits from this location are automatically read out to the Color Value register, and the CL-GD7541/GD7543 automatically increments the Address register.

The color intensity values are then read from the Color Value register by a sequence of three read (RD*) commands. After the blue value is transferred out, new data bits are read from theCLUT current address to the Color Value register, which causes the CL-GD7541/GD7543 to automatically increment the Address register again.

If the CL-GD7541/GD7543 loads the Address register with a new starting address while an unfinished sequence is in progress, the system resets and starts a new sequence. This action occurs for both read and write operations.

3.5 Programmable Core Voltage

To optimize graphics performance and power consumption, the CL-GD7541/GD7543 supports selective switching of the core VDD between 3.3 and 5 V, based upon the graphics mode that is being used.

3.5.1 3.3-V Core Voltage

When the CL-GD7541/GD7543 operates at 3.3 V, the MCLK operates up to 50 MHz, which is sufficient for the following pixel modes:

- 1024 × 768 4-bit/pixel
- 800 × 600 8-bit/pixel
- 640 × 480 16-bit/pixel

The core VDD and analog VDDs *must always* be at the same voltage.

3.5.2 5.0-V Core Voltage

When the CL-GD7541/GD7543 operates at 5.0 V, the MCLK must be at 60 MHz to maximize performance in the following pixel modes:

- 1024 × 768 8-bit/pixel
- 800 × 600 16-bit/pixel
- 640 × 480 24-bit/pixel

The core VDD and analog VDDs (which *must always* be at the same voltage) must be 5 V with an MCLK of 60 MHz.

3.6 Compatibility

Both the CL-GD7541 and the CL-GD7543 include all registers and data paths required for standard VGA controllers. The CL-GD7541 and the CL-GD7543 also support the following extended VGA modes:

- 1024 × 768 with 256 colors (interlaced and non-interlaced modes)
- 1280 × 1024 with 256 colors (interlaced modes)

Additionally, various 132-column text modes are supported.

3.7 Extension Registers

While expanding or centering VGA modes on 640 × 480 or 800 × 600 LCDs, the appropriate VGA registers are shadowed for VGA compatibility.

3.8 Testability

The CL-GD7541/GD7543 is testable by using pin-scan testing and a signature generator.

Pin-scan testing tests the signal state of every pin on the chip. The test detects any pins that are not connected to the board, or that are shorted to a neighboring pin or trace. For more information, refer to Appendix J.

The signature generator allows the entire system, including display memory, to be tested at speed. For more information, refer to Appendix I.

3.9 Configuration Inputs

To configure the chip for operation, the CL-GD7541/GD7543 uses a combination of hardware and software configurations.

3.9.1 Hardware Configuration Inputs

Pull-up resistors are used on some memory data pins, which are read during the low-to-high transition of the system reset or when Extension register SR24[3] (the External Pull-Up Reset register bit)] is toggled.

- **32-bit PCI bus.** This configuration selects the 32-bit PCI bus with Min-grant timing of 8 PCI CLKs (~250 ns at 33 MHz).
- **32-bit PCI bus with Min-grant extended.** This configuration selects the 32-bit PCI bus, but with Min-grant timing extended from 8 PCI CLKs (~250 ns at 33 MHz) to 16 PCI CLKs (~500 ns at 33 MHz), allowing burst write mode capability.
- **Dynamic frame-buffer sharing.** This configuration allows dynamic frame-buffer sharing to be used in a system that is configured for this feature. (This configuration applies to the CL-GD7541 only.)
- **Enable feature connector.** This configuration uses the appropriate pins for the Feature Connector video port. (For the affected pins, refer to the pin descriptions in Chapter 1 and Chapter 2.)
- **Sleep address select.** This configuration selects a sleep address of either I/O address 46E8h or 3C3h (the default).
- **VESA VL-Bus with Bus Clock of > 33 MHz.** This configuration sets the VL-Bus for >33-MHz local bus operation.

If no resistors are present, the above pins are read as low because of the internal pull-down resistors. The status of these inputs is stored in Extension registers SR22 and SR24.

Three hardware switch inputs (SW[2:0]) are read during each horizontal retrace period. These inputs are used by the VGA BIOS to monitor external activities that can affect the chip operation. The status of these three inputs is stored in SR24[2:0].

3.9.2 Software Configuration Inputs

Software-programmable registers are used to select the desired function of some multi-function pins as defined below:

- **ACTI / FCEVIDEO# / SBYI select.** Extension registers SR23[6] and SR24[7] configure the ACTI / FCEVIDEO# / SBYI input (pin 86) as either the Activity Sense input or the hardware-controlled Standby input.
- **BLI / SUSPI enable.** Extension registers SR23[5] and SR24[7] configure the BLI / SUSPI input (pin 87) as either the backlight input control or the hardware-controlled Suspend input.
- **FCDCLK output select.** Extension register SR24[4] is used to output either the VCLK or PCLK0 on the FCDCLK pin.
- **FCVCLK enable.** Extension register SR23[7] selects whether FCVCLK is sent to the DAC only or is also used for VCLK generation.
- **VCLK output enable.** Extension registers SR23[4] and SR24[7] either make the VCLK output pin low or output the internal VCLK on the FCDCLK / VCLK output (pin 103).

For more configuration information, refer to Appendix L and Section 2.7, "Configuration Input Pins".

3.10 Software Support

The Cirrus Logic CL-GD7541/GD7543 VGA BIOS is a high-quality, feature-rich firmware product designed to take maximum advantage of the CL-GD7541/GD7543 controller, especially in the areas of display quality, power management, and graphics performance. The key features of the VGA BIOS are:

- Super VGA-compatible BIOS
- Supports SimulSCAN operation (simultaneous LCD and CRT displays)
- Supports the power-management modes
- Supports display-enhancement features
- Can be integrated with the System BIOS
- Supports switchless configuration
- Can be customized without source code through using utility programs such as OEMSETUP
- Provides VESA-compatible modes and 1.2-function support for VGA BIOS Extensions (VBE)
- Supports multiple monitor refresh rates

A VGA BIOS, fully compatible with the standard IBM VGA BIOS and the INT 10h graphics service functions, is available from Cirrus Logic and third-party BIOS vendors.

The CL-GD7541/GD7543 VGA controller and BIOS can be implemented as an adapter board or placed directly on the system board. The VESA VL-Bus BIOS can be located at C000h or E000h. There is a separate BIOS for PCI bus implementations.

The core BIOS requires 32 Kbytes. Extra functionality, such as EGA-compatible fonts, can be located in a 16-Kbyte optional BIOS. This optional BIOS can either be appended to the core BIOS (for VESA VL-Bus or PCI bus implementations) or loaded into the same segment as the core BIOS (for VESA VL-Bus implementations). For system implementations that do not have ROM space for the 16-Kbyte optional BIOS, a TSR (terminate and stay resident) is provided to support the extra functionality in DOS environments.

3.10.1 Software Support for OEMs

This section lists CL-GD7541/GD7543 software utilities that Cirrus Logic provides for OEM development use.

- **BRender.** This utility is a high-performance 3D application program interface driver from Argonaut.
- **CLDemo.** This utility is a suite of programs that test and demonstrate some of the various features in the CL-GD7541/GD7543, including hardware icon functions and dithering quality.
- **CL_STEST.** This utility is a DOS-based screen-testing utility that provides the following:
  - CL-STEST enables the user to display and adjust the position and RGB color of a variety of patterns (including color bars, lines, and rectangles) to test the display quality.
  - CL-STEST can operate with pixel resolutions of:
    - 640 × 400 or 640 × 480
    - 800 × 600
    - 1024 × 768
- **LOADROM.** This utility loads the VGA BIOS into RAM. It is used with the CL-GD7541/GD7543 PCI Demonstration Board or to quickly test BIOS variations and modifications before loading the BIOS into an EPROM.
- **OEMSI.** This utility is a Cirrus Logic VGA BIOS-customization utility for OEM development use.
- **PCLRegs.** This utility is a DOS-based VGA-controller register viewer/editor utility that provides the following:
  - PCLRegs enables users to view and edit the standard VGA and extension registers and color palette.
  - The PCLRegs Help screen provides a brief explanation of each bit in each register.
  - PCLRegs enables register values to be changed by typing in a new hex value or toggling individual bits.
  - PCLRegs displays a variety of configuration data, including the status of the CRT controller, the graphics mode being used, information about the VGA BIOS, and hardware cursor information.

3.10.2 Software Support for End Users

Cirrus Logic provides the following CL-GD7541/GD7543 software utilities for distribution to end users:

- **CLMode.** This utility, a DOS-based graphics-mode and display-configuration utility, provides the following:
  - Through its user-friendly VGA Configuration menu, CLMode enables users to turn 'on' and 'off' a variety of graphics configuration options, including the following:
    - Automatic text expansion
    - Bold fonts
    - Power-management options
    - Reverse video
    - Selection between CRT, LCD, and SimulSCAN display options
    - Selection between PAL and NTSC television modes
    - Shading of graphics and text
    - Text enhancement
    - Vertical position of display
  - The CLMode Monitor Type Setup menu enables users to set CRT monitor resolution and refresh rate.
  - The CLMode VGA Modes Preview menu enables users to display the various VGA modes.
  - New settings of the above options enabled by the user can be updated in the AUTOEXEC.BAT file.

- **CLVESA.** This utility is a TSR utility that supports the VESA BIOS extensions.
- **Drivers.** The CL-GD7541/GD7543 simplifies driver support for third-party sources because the CL-GD7541/GD7543 is based on the industry-leading CL-GD542X VGA controller design. As a result, a driver supplier can easily modify an existing CL-GD542X driver to support the CL-GD7541/GD7543. At a minimum, this utility allows the CL-GD7541/GD7543 to operate within the restrictions of the older CL-GD542X driver. The CL-GD7541/GD7543 supports the following drivers:
  - AutoCAD®
  - DCI 1.x drivers for Video to Windows 1.1.2 or later
  - OS/2® (2.0 and 2.1)
  - Windows 3.11 driver
  - Windows NT
  - Driver support for the Japanese version of Windows and OS/2 is also available.
- **Switcher.** This utility is a video-configuration TSR.
- **WinMode.** This utility is a Windows application for video-mode configurations. A unique feature of the WinMode utility is the ability to automatically switch the display resolution without relaunching Windows. This feature ensures that a portable user always sees a Windows display, even though they may dynamically switch from using a high-resolution CRT to an LCD of lower resolution. This feature also enables the user to avoid running the Windows Setup application in order to find and switch driver resolutions. (However, color depth changes still require Windows to restart.)
  - WinMode allows users to set high-refresh rates for CRT monitors.
  - WinMode enables users to set the CRT resolution to 640 × 480, 800 × 600, 1024 × 768, or 1280 × 1024.
  - WinMode enables users to select bit depth used on either the CRT or LCD (such as, 16, 256, 64K, 16M).
  - WinMode enables users to turn the Hardware Cursor 'on' and 'off'.
  - WinMode enables users to make the font size normal or large.
  - New settings of the above options enabled by the user can be updated in the AUTOEXEC.BAT file.
  - WinMode also defines the resolution and bit-depth of the CL-GD7541/GD7543 Windows driver. The WinMode utility provides the following:
    - Automatic text expansion
    - Bold fonts
    - Drivers
    - Power-management options (such as the timer intervals for Standby mode or backlight)
    - Reverse video
    - Selection between display options: CRT, LCD, SimulSCAN, PAL, and NTSC
    - Selection to display WinMode in different foreign languages
    - Selection for virtual display (pan and scroll capability for LCDs)
    - Shading of graphics and text
    - Text enhancement
    - Vertical position of display

3.11 Package

The CL-GD7541/GD7543 is available in a standard EIAJ 208-pin PQFP package with a 28 × 28 mm body size and 0.5-mm lead pitch.

4. MODE TABLES

This chapter lists tables for configuring the CL-GD7541/GD7543 for various CRT and LCD graphics and text modes. For detailed information on specific LCDs that the CL-GD7541/GD7543 can drive, refer to the "Panel Interface Guide" in the *CL-GD754X Application Book*.

NOTE: The parameters detailed in the tables of this chapter define standard capabilities of the CL-GD7541/GD7543 when it is used with the Cirrus Logic VGA BIOS. Consult with the appropriate BIOS vendor for information about modes and parameters supported by BIOSs that are not from Cirrus Logic.

4.1 CRT-Only Mode Tables

This section lists tables for IBM Standard VGA and Cirrus Logic Extended CRT-only modes.

4.1.1 IBM® Standard VGA CRT-Only Modes

The IBM® Standard VGA BIOS supports the CRT-only modes listed in Table 4-1.

Table 4-1. IBM® Standard VGA CRT-Only Modes

Mode No. (hex)	No. of Colors	Characters × Rows	Character Cell (pixels)	Screen Format (pixels)	Display Mode	Video Clock (MHz)	Horiz. Freq. (kHz)	Vert. Frequency (Hz)
0, 1	16/256K	40 × 25	9 × 16	360 × 400	Text	28	31.5	70
2, 3	16/256K	80 × 25	9 × 16	720 × 400	Text	28	31.5	70
4, 5	4/256K	40 × 25	8 × 8	320 × 200	Graphics	25	31.5	70
6	2/256K	80 × 25	8 × 8	640 × 200	Graphics	25	31.5	70
7	Mono.	80 × 25	9 × 16	720 × 400	Text	28	31.5	70
D	16/256K	40 × 25	8 × 8	320 × 200	Graphics	25	31.5	70
E	16/256K	80 × 25	8 × 8	640 × 200	Graphics	25	31.5	70
F	Mono.	80 × 25	8 × 14	640 × 350	Graphics	25	31.5	70
10	16/256K	80 × 25	8 × 14	640 × 350	Graphics	25	31.5	70
11	2/256K	80 × 30	8 × 16	640 × 480	Graphics	25	31.5	60
12	16/256K	80 × 30	8 × 16	640 × 480	Graphics	25	31.5	60
13	256/256K	40 × 25	8 × 8	320 × 200	Graphics	25	31.5	70

4.1.2 Cirrus Logic Extended CRT-Only Modes

The Cirrus Logic VGA BIOS supports the extended CRT-only modes listed in Table 4-2.

- Columns one and two compare the hex number of the Cirrus Logic extended CRT-only mode with the hex number of the equivalent VESA VL-Bus CRT-only mode.
- If the BIOS used is not the Cirrus Logic VGA BIOS, modes may differ.
- Some modes are not supported by all CRT monitors.

Table 4-2. Cirrus Logic Extended CRT-Only Modes

Mode No. (hex)	VESA® No. (hex)	No. of Colors	Char. × Rows	Char. Cell (pixels)	Screen Format (pixels)	Display Mode	VCLK (MHz)	Horiz. Freq. (kHz)	Vert. Freq. (Hz)	MIN MCLK (MHz)[a]
14	–	16/256K	132 × 25	8 × 16	1056 × 400	Text	41.5	31.5	70	45
54	10A	16/256K	132 × 43	8 × 8	1056 × 350	Text	41.5	31.5	70	45
55	109	16/256K	132 × 25	8 × 14	1056 × 350	Text	41.5	31.5	70	45
11[b]	–	2/256K	80 × 30	6 × 16	640 × 480	Graphics	31.5	37.9	72[b]	40
							31.5	37.9	75[b]	40
12[b]	–	16/256K	80 × 30	8 × 16	640 × 480	Graphics	31.5	37.9	72[b]	40
							31.5	37.9	75[b]	40
16[c]	–	16/256K	80 × 30	8 × 16	640 × 480	Graphics	25	31.5	60	40
							31.5	37.9	72	40
							31.5	37.9	75	40
58, 6A[d]	102	16/256K	100 × 37	8 × 16	800 × 600	Graphics	36	35.2	56	40
							40	38.6	60	40
							50	48.1	72	40
							50	47.0	75	40
17[c]	–	16/256K	100 × 37	8 × 16	800 × 600	Graphics	40	38.6	60	40
							50	47.0	75	40
5D	104	16/256K	128 × 48	8 × 16	1024 × 768	Graphics	65	48.3	60	40
							44.9	35.5	87[e]	40
							75	56	70	40
							77	58	72	45
							79	60	75	45
18[c]	–	16/256K	128 × 48	8 × 16	1024 × 768	Graphics	65	48.3	60	40
							77	58	72	45
6C[e]	106	16/256K	160 × 64	8 × 16	1280 × 1024	Graphics	75	48	87[e]	45
5E	100	256/256K	80 × 25	8 × 16	640 × 400	Graphics	25	31.5	70	40

Table 4-2. Cirrus Logic Extended CRT-Only Modes *(cont.)*

Mode No. (hex)	VESA® No. (hex)	No. of Colors	Char. × Rows	Char. Cell (pixels)	Screen Format (pixels)	Display Mode	VCLK (MHz)	Horiz. Freq. (kHz)	Vert. Freq. (Hz)	MIN MCLK (MHz)[a]
5F	101	256/256K	80 × 30	8 × 16	640 × 480	Graphics	25	31.5	60	40
							31.5	37.9	72	40
							31.5	37.9	75	40
5C	103	256/256K	100 × 37	8 × 16	800 × 600	Graphics	36	35.2	56	40
							40	37.9	60	40
							50	48.1	72	40
							50	47.0	75	45
60	105	256/256K	128 × 48	8 × 16	1024 × 768	Graphics	44.9	35.5	87[e]	40
							65	48.3	60	45
							75	56	70	50
							77	58	72	50
							79	60	75	50
6D[e]	–	256/256K	160 × 64	8 × 16	1280 × 1024	Graphics	75	48	87[e]	45
66	110	32K	80 × 30	8 × 16	640 × 480	Graphics	25	31.5	60	45
							31.5	37.9	72	45
							31.5	37.9	75	50
67	113	32K	100 × 37	8 × 16	800 × 600	Graphics	36	31.5	56	45
64	111	64K	80 × 30	8 × 16	640 × 480	Graphics	25	31.5	60	45
							31.5	37.9	72	45
							31.5	37.9	75	50
65	114	64K	100 × 37	8 × 16	800 × 600	Graphics	36	35.2	56	45
							40	38.6	60	50
74[e]	–	64K	128 × 48	8 × 16	1024 × 768	Graphics	44.9	35.5	87[e]	50
71	112	16M	80 × 30	8 × 16	640 × 480	Graphics	25	31.5	60	45

[a] The value of the minimum MCLK frequency defined in this column defines the lowest clock frequency at which the CL-GD7541/GD7543 can run without any adverse effects to functionality. Better benchmark performance may be achieved with an MCLK frequency higher than the frequency specified in this column.

[b] Modes denoted by 'b' are IBM® standard VGA modes that have been enhanced by Cirrus Logic for a higher vertical frequency.

[c] Modes denoted by 'c' are 4-bit-per-pixel packed-pixel modes.

[d] Application programs must use graphics mode 6Ah, rather than 58h, to retain compatibility with other VGA BIOS products.

[e] All modes with a vertical frequency of 87 Hz are interlaced modes.

4.2 LCD-Only/ SimulSCA N™ Mode Table s

This section lists tables for the LCD-only/SimulSCAN modes that the Cirrus Logic VGA BIOS supports.

4.2.1 Cirrus Logic LCD-Only/ SimulSCA N™ Modes for 800 x 600 LCD s

For 800 x 600 LCDs, the Cirrus Logic VGA BIOS supports the LCD-only/SimulSCAN modes in Table 4-4. (Unless otherwise noted, all screen formats expand to 800 x 600 pixels to fill the entire LCD screen

- If the BIOS used is not the Cirrus Logic VGA BIOS, modes may differ .
- Some modes are not supported by all CRT monitors .

Table 4-3. Cirrus Logic LCD-Only/ SimulSCA N™ Modes for 800 x 600 LCD s[a]

Mode No. (hex)	No. of Colors	Char. × Rows	Char. Cell (pixels)	Screen Format (pixels)	Graphics Panel Type	Video Clock (MHz)	Horiz. Freq. (kHz)	Vert. Freq. (Hz)[b]	Mini-mum MCLK (MHz)[c]
0,1	16/256K	40 × 25	8 × 16	360 × 400	DSTN	33.7	33	53	50[d]
					TFT	40	38.6	60	50
2,3	16/256K	80 × 25	8 × 16	720 × 400	DSTN	33.7	33	53	50[d]
					TFT	40	38.6	60	50
4,5	4/256K	40 × 25	8 × 8	320 × 200	DSTN	33.7	33	53	50
					TFT	40	38.6	60	50
6	2/256K	80 × 25	8 × 8	640 × 200	DSTN	33.7	33	53	50
					TFT	40	38.6	60	50
7	Mono.	80 × 25	8 × 16	720 × 400	DSTN	33.7	33	53	50[d]
					TFT	40	38.6	60	50
D	16/256K	40 × 25	8 × 8	320 × 200	DSTN	33.7	33	53	50
					TFT	40	38.6	60	50
E	16/256K	80 × 25	8 × 8	640 × 200	DSTN	33.7	33	53	50
					TFT	40	38.6	60	50
F	Mono.	80 × 25	8 × 14	640 × 350	DSTN	33.7	33	53	50
					TFT	40	38.6	60	50
10	16/256K	80 × 25	8 × 14	640 × 350	DSTN	33.7	33	53	50
					TFT	40	38.6	60	50
11	2/256K	80 × 30	8 × 16	640 × 480	DSTN	33.7	33	53	50
					TFT	40	38.6	60	50
12	16/256K	80 × 30	8 × 16	640 × 480	DSTN	33.7	33	53	50
					TFT	40	38.6	60	50
13	256/256K	40 × 25	8 × 8	320 × 200	DSTN	33.7	33	53	50
					TFT	40	38.6	60	50

Table 4-3. Cirrus Logic LCD-Only/ SimulSCA N™ Modes for 800 x 600 LCD s[a]

Mode No. (hex)	No. of Colors	Char. × Rows	Char. Cell (pixels)	Screen Format (pixels)	Graphics Panel Type	Video Clock (MHz)	Horiz. Freq. (kHz)	Vert. Freq. (Hz)[b]	Mini-mum MCLK (MHz)[c]
16[e]	16/256K	80 × 30	8 × 16	640 × 480	DSTN	33.7	33	53	50
					TFT	40	38.6	60	50
58, 6A[f]	16/256K	100 × 37	8 × 16	800 × 600	DSTN	33.7	33	53	50
					TFT	40	38.6	60	50
17	16/256K	100 × 37	8 × 16	800 × 600	DSTN	33.7	33	53	50
					TFT	40	38.6	60	50
5C	256/256K	100 × 37	8 × 16	800 × 600	DSTN	33.7	33	53	50
					TFT	40	38.6	60	50
5E	256/256K	80 × 25	8 × 16	640 × 400	DSTN	33.7	33	53	50
					TFT	40	38.6	60	50
5F	256/256K	80 × 30	8 × 16	640 × 480	DSTN	33.7	33	53	50[d]
					TFT	40	38.6	60	50
66[g, h]	32K	80 × 30	8 × 16	640 × 480	TFT	40	38.6	60	50
67[g, h]	32K	100 × 37	8 × 16	800 × 600	TFT	40	38.6	60	50
64[g, h]	64K	80 × 30	8 × 16	640 × 480	TFT	40	38.6	60	50
65[g, h]	64K	100 × 37	8 × 16	800 × 600	TFT	40	38.6	60	50

[a] To optimize the LCD display, the Cirrus Logic OEMSI program can be used to customize LCD-only timings. (For details, refer to the document "OEM System Integration Tool", in the binder for the *CL-GD754X VGA BIOS and Utilitie s*.)

[b] For 60-Hz vertical frequency operation for color DSTN panel types, the display memory DRAM random access time (Trc) must be 120 ns. In this case, Extension register SRF[2] must be equal to '1' to optimize the display memory bandwidth .

[c] The value of the minimum MCLK frequency defined in this column defines the lowest clock frequency at which the CL-GD7541/GD7543 can run without any adverse effects to functionality . Better benchmark performance may be achieved with an MCLK frequency other than the frequency specified in this column .

[d] For a centering, non-expanded mode, the MCLK minimum is 53.7 MHz .

[e] Modes denoted by 'e' are 4-bit-per-pixel packed-pixel modes .

[f] Application programs must use graphics mode 6Ah, rather than 58h, to retain compatibility with other VGA BIOS products .

[g] Modes denoted by 'g' indicate that 800 x 600 dual-scan color LCDs are not supported by these mode s

[h] Modes denoted by 'h' indicate that the mode is a centering, non-expanded mode only .

4.2.2 Cirrus Logic LCD-Only/SimulSCAN™ Modes for 640 x 480 LCDs

For 640 x 480 LCDs, the Cirrus Logic VGA BIOS supports the LCD-only/SimulSCAN modes in Table 4-4. (Unless otherwise noted, all screen formats expand to 640 x 480 pixels to fill the entire LCD screen.)

- If the BIOS used is not the Cirrus Logic VGA BIOS, modes may differ.
- Some modes are not supported by all CRT monitors.

Table 4-4. Cirrus Logic LCD-Only/SimulSCAN™ Modes for 640 x 480 LCDs[a]

Mode No. (hex)	No. of Colors	Char. × Rows	Char. Cell (pixels)	Screen Format (pixels)	Graphics Panel Type	Video Clock (MHz)	Horiz. Freq. (kHz)	Vert. Freq. (Hz)	Minimum MCLK (MHz)[b]
0,1	16/256K	40 × 25	8 × 16	360 × 400	DSTN/TFT	25	31.5	60	45
2,3	16/256K	80 × 25	8 × 16	720 × 400	DSTN/TFT	25	31.5	60	45
4,5	4/256K	40 × 25	8 × 8	320 × 200	DSTN/TFT	25	31.5	60	45
6	2/256K	80 × 25	8 × 8	640 × 200	DSTN/TFT	25	31.5	60	45
7	Mono.	80 × 25	8 × 16	720 × 400	DSTN/TFT	25	31.5	60	45
D	16/256K	40 × 25	8 × 8	320 × 200	DSTN/TFT	25	31.5	60	45
E	16/256K	80 × 25	8 × 8	640 × 200	DSTN/TFT	25	31.5	60	45
F	Mono.	80 × 25	8 × 14	640 × 350	DSTN/TFT	25	31.5	60	45
10	16/256K	80 × 25	8 × 14	640 × 350	DSTN/TFT	25	31.5	60	45
11	2/256K	80 × 30	8 × 16	640 × 480	DSTN/TFT	25	31.5	60	45
12	16/256K	80 × 30	8 × 16	640 × 480	DSTN/TFT	25	31.5	60	45
13	256/256K	40 × 25	8 × 8	320 × 200	DSTN/TFT	25	31.5	60	45

[a] To optimize the LCD display, the Cirrus Logic OEMSI program can be used to customize LCD-only timings. (For details, refer to the document "OEM System Integration Tool", in the binder for the *CL-GD754X VGA BIOS and Utilities*.)

[b] The value of the minimum MCLK frequency defined in this column defines the lowest clock frequency at which the CL-GD7541/GD7543 can run without any adverse effects to functionality. Better benchmark performance may be achieved with an MCLK frequency other than the frequency specified in this column.

5. VGA REGISTER PORT MA P

Table 5-1. VGA Register Port Ma p

Address	Port	Port Type
3B4	CRT Controller Index — monochrom e	Read/Write
3B5	CRT Controller Data — monochrom e	Read/Write
3BA	Feature Control — monochrom e	Write
	Input Status register 1 — monochrom e	Read
3C0	Attribute Controller Index / Dat a	Write
3C1	Attribute Controller Index / Dat a	Read
3C2	Miscellaneous Output	Write
	Input Status register 0	Read
3C3	Motherboard Sleep	Read/Write
3C4	Sequencer Index	Read/Write
3C5	Sequencer Data	Read/Write
3C6	Video DAC Pixel Mask (R/W), Hidden DAC register	Read/Write
3C7	Pixel Address Read mode	Write
	DAC State	Read
3C8	Pixel Mask Write mode	Read/Write
3C9	Pixel Data	Read/Write
3CA	Feature Control Readback	Read
3CC	Miscellaneous Output Readback	Read
3CE	Graphics Controller Inde x	Read/Write
3CF	Graphics Controller Data	Read/Write
3D4	CRT Controller Index — colo r	Read/Write
3D5	CRT Controller Data — colo r	Read/Write
3DA	Feature Control — colo r	Write
	Input Status register 1 — colo r	Read
46E8	Adapter Sleep	Read/Write

6. REGISTER SUMMAR Y

The registers in this chapter include standard VGA registers, as well as Extension registers that Cirrus Logic has added.

6.1 Summary of External /General Registers in Chapter 7

The External and General registers in the CL-GD7541/GD7543 are summarized in the following table:

Abbreviation	Register Name	Index	Port	Page
MISC	Miscellaneous Output	–	3C2 (Write)	113
MISC	Miscellaneous Output	–	3CC (Read)	113
FC	Feature Control	–	3?A (Write)	116
FC	Feature Control	–	3CA (Read)	116
FEAT	Input Status Register 0	–	3C2	117
STAT	Input Status Register 1	–	3?A	118
3C3	Sleep Mode	–	3C3	119
3C6	Pixel Mask	–	3C6	119
3C7	Pixel Address Read Mode	–	3C7 (Write)	121
3C7	DAC State	–	3C7 (Read)	122
3C8	Pixel Address Write Mode	–	3C8	123
3C9	Pixel Data	–	3C9	124
PCI00	PCI Device ID / PCI Vendor ID	–	00	125
PCI04	PCI Command	–	04	126
PCI04	PCI Status	–	04	127
PCI10	PCI Base Address	–	10	128
PCI3C	PCI Interrupt Pin and PCI Interrupt Line	–	3C	129
46E8	Alternate Sleep Mode	–	46E8	130

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode .

6.2 Summary of Sequencer Registers in Chapter 8

The CL-GD7541/GD7543 Sequencer registers are summarized in the following table. Note that there are Extension registers that are accessed using the Sequencer ports.

Abbreviation	Register Name	Index	Port	Page
SRX	Sequencer Index	–	3C4	131
SR0	Reset	0	3C5	133
SR1	Clocking Mode	1	3C5	134
SR2	Plane Mask	2	3C5	136
SR3	Character Map Set Select	3	3C5	137
SR4	Memory Mode	4	3C5	139

6.3 Summary of CRT Controller Registers in Chapter 9

The CL-GD7541/GD7543 VGA CRT Controller registers are summarized in the following table. Note that there are Extension registers that are accessed using the CRT Controller ports.

Abbreviation	Register Name	Index	Port	Page
CRX	CRT Controller Index	–	3?4	141
CR0	Horizontal Total	0	3?5	142
CR1	Horizontal Display End	1	3?5	145
CR2	Horizontal Blanking Start	2	3?5	146
CR3	Horizontal Blanking End	3	3?5	147
CR4	Horizontal Sync Start	4	3?5	149
CR5	Horizontal Sync End	5	3?5	150
CR6	Vertical Total	6	3?5	152
CR7	Overflow	7	3?5	153
CR8	Screen A Preset Row Scan	8	3?5	154
CR9	Character Cell Height	9	3?5	155
CRA	Text Cursor Start	A	3?5	156
CRB	Text Cursor End	B	3?5	157
CRC	Screen A Start Address High	C	3?5	158
CRD	Screen A Start Address Low	D	3?5	159
CRE	Text Cursor Location High	E	3?5	160
CRF	Text Cursor Location Low	F	3?5	161
CR10	Vertical Sync Start	10	3?5	162
CR11	Vertical Sync End	11	3?5	163
CR12	Vertical Display End	12	3?5	165
CR13	Offset	13	3?5	166
CR14	Underline Row Scanline	14	3?5	167
CR15	Vertical Blanking Start	15	3?5	168
CR16	Vertical Blanking End	16	3?5	169
CR17	Mode Control	17	3?5	170
CR18	Line Compare	18	3?5	172
CR22	Graphics Controller Data Latches Readback	22	3?5	173
CR24	Attribute Controller Toggle Readback	24	3?5	174
CR26	Attribute Controller Index Readback	26	3?5	175

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode .

6.4 Summary of Graphics Controller Registers in Chapter 1 0

The CL-GD7541/GD7543 Graphics Controller registers are summarized in the following table. Note that there are Extension registers that are accessed using the Graphics Controller port.

Abbreviation	Register Name	Index	Port	Page
GRX	Graphics Controller Index	–	3CE	177
GR0	Set / Reset	0	3CF	178
GR1	Set / Reset Enable	1	3CF	179
GR2	Color Compare	2	3CF	180
GR3	Data Rotate	3	3CF	181
GR4	Read Map Plane Select	4	3CF	182
GR5	Mode	5	3CF	183
GR6	Miscellaneous	6	3CF	187
GR7	Color Don't Care Plane	7	3CF	188
GR8	Display Memory Bit Mask	8	3CF	189

6.5 Summary of Attribute Controller Registers in Chapter 1 1

The CL-GD7541/GD7543 Attribute Controller registers are summarized in the following table:

Abbreviation	Register Name	Index	Port	Page
ARX	Attribute Controller Index	–	3C0/3C1	191
AR0–ARF	Attribute Controller Palette	0–F	3C0/3C1	192
AR10	Attribute Controller Mode	10	3C0/3C1	193
AR11	Overscan (Border) Color	11	3C0/3C1	195
AR12	Color Plane Enable	12	3C0/3C1	196
AR13	Pixel Panning	13	3C0/3C1	198
AR14	Color Select	14	3C0/3C1	199

6.6 Summary of Extension Registers in Chapter 1 2

The CL-GD7541/GD7543 Extension registers are summarized in the following table:

Abbreviation	Register Name	Index	Port	Page
SR6	Unlock All Extension Registers	6	3C5	201
SR7	Extended Sequencer Mode	7	3C5	202
SR8	Miscellaneous Control Register 1	8	3C5	205
SR9	Scratchpad 0	9	3C5	206
SRA	Scratchpad 1	A	3C5	206
SRB	VCLK0 Numerator	B	3C5	207
SRC	VCLK1 Numerator	C	3C5	207
SRD	VCLK2 Numerator	D	3C5	207
SRE	VCLK3 Numerator	E	3C5	207
SRF	Display Memory Control	F	3C5	209
SR10	HW Cursor and HW Icon Coarse Horizontal Position	10	3C5	211
SR11	HW Cursor and HW Icon Coarse Vertical Position	11	3C5	213
SR12	Video Data Path Control	12	3C5	214
SR13	Hardware Cursor Pattern Address Offset	13	3C5	217
SR14	Scratchpad 2	14	3C5	218
SR15	Scratchpad 3	15	3C5	218
SR16	Performance Tuning	16	3C5	219
SR18	Signature Generator Control	18	3C5	221
SR19	Signature Generator Result Low	19	3C5	223
SR1A	Signature Generator Result High	1A	3C5	224
SR1B	VCLK0 Denominator and Post-scalar Value	1B	3C5	225
SR1C	VCLK1 Denominator and Post-scalar Value	1C	3C5	225
SR1D	VCLK2 Denominator and Post-scalar Value	1D	3C5	225
SR1E	VCLK3 Denominator and Post-scalar Value	1E	3C5	225
SR1F	MCLK Frequency and VCLK Source Select	1F	3C5	227
SR20	Miscellaneous Control Register 2	20	3C5	228
SR21	Dual-Scan Color Control	21	3C5	231
SR22	Hardware Configuration Read Register 1	22	3C5	232
SR23	Software Configuration Register 1	23	3C5	234
SR24	LCD-Type Switches and Feature Connector Enable	24	3C5	236
SR25	Timer-Software Reset and Hardware Configuration 2	25	3C5	238
SR26	Shader Signature Lo w	26	3C5	240
SR27	Shader Signature Hig h	27	3C5	241
SR28	Scratchpad 5	28	3C5	242
SR29	Scratchpad 6	29	3C5	242
SR2A	Hardware Icon #0 Control	2A	3C5	243
SR2B	Hardware Icon #1 Control	2B	3C5	244
SR2C	Hardware Icon #2 Control and Miscellaneous PCI	2C	3C5	246
SR2D	Hardware Icon #3 Control and HIMEM Select	2D	3C5	247
SR2E	Hardware Cursor Horizontal Position Extension	2E	3C5	249
SR2F	Half-Frame-Accelerator FIFO Threshold	2F	3C5	251

6.6 Summary of Extension Registers i n Chapter 1 2 *(cont.)*

Abbreviation	Register Name	Index	Port	Page
Graphics Controller Extension Register s				
GR9	Offset Register 0	9	3CF	252
GRA	Offset Register 1	A	3CF	254
GRB	Graphics Controller Mode Extensions	B	3CF	255
GRC	Color Key Compare	C	3CF	257
GRD	Color Key Compare Mask	D	3CF	258
GRE	PCI Burst-Write and Green PC Control	E	3CF	260
GR10	16-Bit Pixel Background Color High	10	3CF	261
GR11	16-Bit Pixel Foreground Color High	11	3CF	262
GR20	BitBLT Width Low	20	3CF	263
GR21	BitBLT Width High	21	3CF	264
GR22	BitBLT Height Low	22	3CF	265
GR23	BitBLT Height High	23	3CF	266
GR24	BitBLT Destination Pitch Low	24	3CF	267
GR25	BitBLT Destination Pitch High	25	3CF	268
GR26	BitBLT Source Pitch Low	26	3CF	269
GR27	BitBLT Source Pitch High	27	3CF	270
GR28	BitBLT Destination Start Low	28	3CF	271
GR29	BitBLT Destination Start Mid	29	3CF	272
GR2A	BitBLT Destination Start High	2A	3CF	273
GR2C	BitBLT Source Start Low	2C	3CF	274
GR2D	BitBLT Source Start Mid	2D	3CF	275
GR2E	BitBLT Source Start High	2E	3CF	276
GR30	BitBLT Mode	30	3CF	277
GR31	BitBLT Start/Status	31	3CF	280
GR32	BitBLT Raster Operation	32	3CF	281
GR34	BitBLT Transparent Color Select Low	34	3CF	282
GR35	BitBLT Transparent Color Select High	35	3CF	283
GR38	BitBLT Transparent Color Mask Low	38	3CF	284
GR39	BitBLT Transparent Color Mask High	39	3CF	285

6.6 Summary of Extension Registers in Chapter 12 *(cont.)*

Abbreviation	Register Name	Index	Port	Page
CRT Controller Extension Registers				
CR19	Interlace End	19	3?5	286
CR1A	Miscellaneous Control	1A	3?5	287
CR1B	Extended Display Controls	1B	3?5	289
CR1D	Video Overlay Mode	1D	3?5	291
CR1E	LCD Shading	1E	3?5	292
CR1F	LCD Modulation Control	1F	3?5	294
CR20	Power Management	20	3?5	296
CR21	Power-Down Timer Control	21	3?5	300
CR23	SUSPI Debounce Timer	23	3?5	302
CR25	Manufacturing Revision ID	25	3?5	304
CR27	Device ID and Manufacturing Revision ID	27	3?5	305
CR29	Configuration Status	29	3?5	306
CR2C	LCD Interface	2C	3?5	307
CR2D	LCD Display Controls	2D	3?5	310
CR2E	LCD High-Resolution Control	2E	3?5	312
CR2F	Driver and BIOS Revision	2F	3?5	313
CR30	TV-OUT Control	30	3?5	314
MotionVideo Window (MVW) Control Registers (CL-GD7543 only)				
CR33	MVW Horizontal Start (XS) / Width (XW) Overflow	33	3?5	316
CR34	MVW Horizontal Start (XS)	34	3?5	317
CR35	MVW Horizontal Width (XW)	35	3?5	318
CR36	YUV-to-RGB Conversion / MVW Vertical-Position High	36	3?5	319
CR37	MVW Vertical Start (YS)	37	3?5	320
CR38	MVW Vertical End (YE)	38	3?5	321
CR39	MVW Surrounding Address Offset	39	3?5	322
CR3A	MVW Memory Address Start	3A	3?5	323
CR3B	MVW Memory Address Offset	3B	3?5	324
CR3C	MVW Scaling, Enable, and Encoding Format	3C	3?5	325
CR3D	MVW Horizontal-Pixel-Width	3D	3?5	326

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode .

6.6 Summary of Extension Registers in Chapter 1 2 *(cont.)*

Abbreviation	Register Name	Index	Port	Page
LCD Timing Control Registers				
CR40	LCD Horizontal-Display-Enable Start – No Centering	40	3?5	327
CR41	LCD HDE Start to Center 720-Dot Display	41	3?5	329
CR42	LCD HDE Start to Center 640-Dot Display	42	3?5	330
CR43	LCD Dot-Clock-Delay Control	43	3?5	331
CR44	LCD Horizontal Display Width	44	3?5	333
CR47	TFT HSYNC Horizontal Start Position	47	3?5	334
CR48	TFT HSYNC and LCD-Height Overflow	48	3?5	335
CR49	Vertical Size for Upper Half of Dual-Scan STN LCDs	49	3?5	336
CR4A	Vertical Size for LCDs	4A	3?5	337
CR4B	Reserved for Scratc hpad	4B	3?5	338
CR4C	Graphics Input-Resolution Override for Dithering	4C	3?5	339
CR4D	Output Resolution for Dithering	4D	3?5	342
CR4E	MVA/Video Overla y Input-Resolution Override	4E	3?5	343
HDR	Hidden DAC Register	–	3C6	345
R2X	LCD Timing — LFS Vertical Position #1	2	3?5	347
R3X	LCD Timing — LFS Vertical Position #2	3	3?5	350
R4X	LCD Timing — LFS Vertical Position #3	4	3?5	351
R5X	LCD Timing — LFS Vertical Position #4	5	3?5	352
R6X	LCD Timing — Overflow Bits for LFS Signal Compare	6	3?5	353
R7X	LCD Timing — Signal Control for Color TFT LCDs	7	3?5	354
R8X	LCD Timing — Shift Clock and Data Select	8	3?5	356
R9X	TFT LCD Data Format	9	3?5	357
RBX	Shade Conversion and Extra LCD Line Clock Insertion	B	3?5	358
RCX	LFS Vertical Position for 525-Line Modes	C	3?5	359
RDX	LCD Timing — LFS Vertical Position #6	D	3?5	360
REX	RDX and RCX Overflo w	E	3?5	361
LCD Horizontal Timing Control Shadow Registers				
R0Y	Horizontal Total Shadow	0	3?5	362
R2Y	Horizontal Blanking Start Shadow	2	3?5	363
R3Y	Horizontal Blanking End Shadow	3	3?5	364
R4Y	Horizontal Sync Start Shadow	4	3?5	365
R5Y	Horizontal Sync End Shadow	5	3?5	366
R0Z	Horizontal Total Shadow	0	3?5	367
R2Z	Horizontal Blanking Start Shadow	2	3?5	368
R3Z	Horizontal Blanking End Shadow	3	3?5	369
R4Z	Horizontal Sync Start Shadow	4	3?5	370
R5Z	Horizontal Sync End Shadow	5	3?5	371

NOTES:

1) '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.
2) The RnX registers are indexed through the settings of CR2D .
3) The R0Y–R5Y and R0Z–R5Z registers are indexed through the settings of CR2C .

7. EXTERNAL/GENERAL REGISTERS

7.1 MISC: Miscellaneous Output Register

I/O Port Address: 3C2 (Write) 3CC (Read)

Index: –

Bit	Description	Reset State
7	Vertical Sync Polarity	0
6	Horizontal Sync Polarity	0
5	Page Select	0
4	Reserved	
3	Clock Select [1]	0
2	Clock Select [0]	0
1	Display Memory Enable	0
0	CRTC I/O Address	0

This standard VGA register has an assortment of bits that have nothing in common.

Bit **Description**

7 **Vertical Sync Polarity :**
When this bit is programmed to:
- 0, Vertical Sync is normally low. A high indicates beginning sync time.
- 1, Vertical Sync is normally high. A low indicates beginning sync time.

6 **Horizontal Sync Polarity:**
- When this bit is programmed to:
  — 0, Horizontal Sync is normally low. A high indicates beginning sync time.
  — 1, Horizontal Sync is normally high. A low indicates beginning sync time.
- For some monitors, the combined polarity of Vertical and Horizontal Sync is used to indicate the number of scanlines per frame, as shown in the table.
- When Extension register CR20[5] = 1 *and* MISC[7:6] = 00, the value of MISC[7:6] is redefined from reserved to an 800 × 600 LCD.

MISC		Vertical Size	Vertical Overscan	Vertical Total =
[7] Vertical Sync Polarity	[6] Horizontal Sync Polarity	(Scanlines appearing on screen)	(Scanlines appearing off screen)	(Vertical Size + Vertical Over-scan)
0 (+)	0 (+)	Reserved	Reserved	Reserved
0 (+)	1 (–)	400	14	414
1 (–)	0 (+)	350	12	362
1 (–)	1 (–)	480	16	496

7.1 MISC: Miscellaneous Output Register *(cont.)*

Bit — **Descriptio n**

5 — **Page Select :**
When SR4[2] (the odd/even bit of the Sequencer Memory Mode register) is 1, MISC[5] affects how display memory addresses are selected.
- When SR4[2] = 1, and this bit = 0, only odd memory locations are selected.
- When SR4[2] = 1, and this bit = 1, only even memory locations are selected.
- This bit takes effect for Graphics modes 6h, Dh, Eh, 11h, and 12h.
- This bit is ignored if either of the following are true:
  - — Graphics Controller register GR6[1] = 1.
  - — Sequencer register SR4[3] = 1.

4 — **Reserve d**

3:2 — **Clock Select :**
This field is used with Extension register bits to choose a video clock source for the CL-GD7541/GD7543, as shown in the following table.

SR22 [3]	SR23 [7]	MISC [3]	MISC [2]	SR1F [6]	SR1E [0]	Video Clock Sourc e for CL-GD7541/GD754 3
0	0	0	0	0	X	SR0B (N) / SR1B (D) [a]
0[b]	X	X	X	0	X	OSC if TV-out enable d
X	X	X	X	1	0	MCLK
X	X	X	X	1	1	MCLK ÷ 2 [c]
0	0	0	1	0	X	SR0C (N) / SR1C (D) [a]
0	0	1	0	0	X	SR0D (N) / SR1D (D) [a]
0	0	1	1	0	X	SR0E (N) / SR1E (D) [a]
0	1	0	X	0	X	FCVCLK to only DA C
0	1	1	X	0	X	FCVCLK to both DAC and CRT C
1	1	0	X	0	X	OSC (pin)

[a] These are Nume rator/Denominator registers. For information on programming alternative fr e-quencies, refer to Appendix G.

[b] True only if CR30[3] = 1 and SR25[4] = 1 .

[c] True only if SR12[4] = 1 .

1 — **Display Memory Enable :**
When this bit is programmed to:
- 0, the CL-GD7541/GD7543 does not respond to display memory accesses.
- 1, the CL-GD7541/GD7543 responds normally to display memory accesses.

7.1 MISC: Miscellaneous Output Register *(cont.)*

Bit	Descriptio n
0	**CRTC I/O Address :** This bit selects either monochrome or color I/O addresses.

MISC[0]	Mode	Input Status / Feature Control	CRTC Index	CRTC Data
0	Monochrome	3BA	3B4	3B5
1	Color	3DA	3D4	3D5

7.2 FC: Feature Control Registe r

I/O Port Address: 3?A (Write) 3CA (Read)

Index: –

Bit	Description	Reset Stat e
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	CRT VSYNC Control	0
2	Reserved	
1	Reserved	
0	Reserved	

This register is one of the original IBM PC registers. Nearly all the bits are no longer used

Bit	Descriptio n
7:4	**Reserve d**
3	**CRT VSYNC Contro l:** This bit is normally used for CRTs that have a internal vertical display enable signal pin. Program this bit to: • 0 to keep the CRT VSYNC signal unchanged and maintain IBM compatibility. • 1 to logically OR the CRT VSYNC signal with the CL-GD7541/GD7543 internal vertical display enable signal prior to sending it to the VSYNC pin.
2:0	**Reserve d**

NOTE: '?' in the above register address is 'B' in Monochrome mode and 'D' in Color mode.

7.3 FEAT: Input Status Register 0

I/O Port Address: 3C2

Index: –

Bit	Description	Reset State
7	Vertical Interrupt Request Pending	0
6	Reserved	
5	Reserved	
4	DAC Switch Sensing	0
3	Reserved	
2	Reserved	
1	Reserved	
0	Reserved	

The bits in this read-only register are nearly all undefined.

Bit	Description
7	**Vertical Interrupt Request Pending:** When this bit is: • 1, there is a vertical interrupt request pending. • 0, there is no vertical interrupt request pending. For more information on the CL-GD7541/GD7543 vertical interrupt system, refer to CRT Controller register CR11.
5	**Reserved**
4	**DAC Switch Sensing:** This read-only bit is used to report the on-off status of one of four analog comparator RAMDAC sense switches, as selected by MISC[3:2]. This bit is: • 1 when the selected DAC sense switch is on. • 0 when the selected DAC sense switch is off.
3:0	**Reserved**

7.4 STAT: Input Status Register 1

I/O Port Address: 3?A

Index: –

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Diagnostic [1]	0
4	Diagnostic [0]	0
3	Vertical Retrace	0
2	Reserved	
1	Reserved	
0	Video Display Enable	0

This read-only register contains some status bits.

Bit — **Description**

7:6 — **Reserved**

5:4 — **Diagnostic [1:0]:**

- As a standard VGA feature, these bits reflect the status of 2 bits selected from the 8 output bits of Attribute Controller register bits AR12[5:4]. (The table indicates how the 2 bits are selected.)

AR12		STAT	
[5]	[4]	[5]	[4]
0	0	FP[2] Red	FP[0] Blue
0	1	FP[3] Secondary Blue	FP[1] Green
1	0	FP[5] Secondary Red	FP[4] Secondary Green
1	1	FP[7]	FP[6]

- As a feature of the CL-GD7541/GD7543, for debugging, the STAT[5:4] bits can reflect data on the Feature Connector FCP[7:0] if both of the following are true:
  - — The Feature Connector is enabled.
  - — The Feature Connector is configured to input data into the CL-GD7541/GD7543.

3 — **Vertical Retrace**:
A 1 on this bit indicates that vertical retrace is in progress.

2:1 — **Reserved**

0 — **Video Display Enable:**

- When this bit is 0, video data bits are being serialized and displayed.
- When this bit is 1, vertical or horizontal blanking is active.

NOTE: '?' in the above register address is 'B' in Monochrome mode and 'D' in Color mode.

7.5 3C3: Sleep Mode Register

I/O Port Address: 3C3

Index: –

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	Reserved	
1	Sleep Mode Readback	1
0	Sleep Mode Write / Readback	1

The CL-GD7541/GD7543 may be put into the sleep mode in one of several ways.

1) Sleep Mode Method 1:
This 3C3 Sleep Mode register is normally recommended for motherboard applications.

2) Sleep Mode Method 2:
When the S46 / MD[21] pin has an external pull-up resistor attached, the alternate Sleep Mode register, 46E8, is selected. (The 3C3 Sleep Mode register is then inactive.)

3) Sleep Mode Method 3:
The sleep mode may also be activated when the SLEEP# input pin is low.

Bit	Description
7:2	**Reserved**
1	**Sleep Mode Readback**: This bit is read-only. When 3C3[0] is: • 1, this bit is also 1. • 0, this bit is also 0.
0	**Sleep Mode Write / Readback :** This read/write bit is normally 1. When this bit is: • 1, the CL-GD7541/GD7543 is active and can respond to normal bus and display activity. • 0, the CL-GD7541/GD7543 turns off the interface to the display memory, the interface to the CPU I/O, and the displays. Also, no other chip accesses except those to 3C3 are allowed until this bit is set to 1.

7.6 3C6: Pixel Mask Registe r

I/O Port Address: 3C6

Index: –

Bit	Description	Reset Stat e
7	Pixel Mask Bit [7]	0
6	Pixel Mask Bit [6]	0
5	Pixel Mask Bit [5]	0
4	Pixel Mask Bit [4]	0
3	Pixel Mask Bit [3]	0
2	Pixel Mask Bit [2]	0
1	Pixel Mask Bit [1]	0
0	Pixel Mask Bit [0]	0

The bits in this read-only register form the pixel mask for the palette DAC. Typically, the Cirrus Logic BIOS programs all these bits to 1. This same 3C6 address is used to access the hidden DAC register, described in the Extension registers in Chapter 12.

Bit	Descriptio n
7:0	**Pixel Mask [7:0] :** This field is the pixel mask for the palette DAC. When a bit in this field is pro-grammed to 0, the corresponding bit in the pixel data is ignored in looking up an entry in the CLUT.

7.7 3C7: Pixel Address Read Mode Register (Write Only)

I/O Port Address: 3C7

Index: –

Bit	Description	Reset State
7	Pixel Address Bit (Read Mode) [7]	0
6	Pixel Address Bit (Read Mode) [6]	0
5	Pixel Address Bit (Read Mode) [5]	0
4	Pixel Address Bit (Read Mode) [4]	0
3	Pixel Address Bit (Read Mode) [3]	0
2	Pixel Address Bit (Read Mode) [2]	0
1	Pixel Address Bit (Read Mode) [1]	0
0	Pixel Address Bit (Read Mode) [0]	0

The bits in this write-only register form the Pixel Address (Read mode) for the palette DAC. This Pixel Address is then used to specify the CLUT entry that is to be read.

Bit	Description
7:0	**Pixel Address (Read Mode) [7:0] :** This field is the Pixel Address (Read mode) for an entry in the CLUT. At the conclusion of every third read of the Pixel Data register (3C9), this address is incremented by one.

7.8 3C7: DAC State Register (Read Only)

I/O Port Address: 3C7

Index: –

Bit	Description	Reset Stat e
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	Reserved	
1	DAC State [1]	0
0	DAC State [0]	0

The bits in this read-only register indicate whether a read or a write to the CLUT occurred last

Bit	Descriptio n
7:2	**Reserve d**
1:0	**DAC State [1:0] :** This 2-bit field indicates which pixel address register was accessed last. • Both bits in this field are always the same digit. • When the bits are: — 00, a write operation is in progress, meaning that the last accessed register for the CLUT was the Pixel Address Write register. — 11, a read operation is in progress, meaning that the last accessed register for the CLUT was the Pixel Address Read register.

7.9 3C8: Pixel Address Write Mode Register

I/O Port Address: 3C8

Index: –

Bit	Description	Reset State
7	Pixel Address Bit (Write Mode) [7]	0
6	Pixel Address Bit (Write Mode) [6]	0
5	Pixel Address Bit (Write Mode) [5]	0
4	Pixel Address Bit (Write Mode) [4]	0
3	Pixel Address Bit (Write Mode) [3]	0
2	Pixel Address Bit (Write Mode) [2]	0
1	Pixel Address Bit (Write Mode) [1]	0
0	Pixel Address Bit (Write Mode) [0]	0

The bits in this registers form the Pixel Address (Write mode) for the palette DAC. This Pixel Address is then used to specify the CLUT entry that is to be written.

Bit	Description
7:0	**Pixel Address (Write Mode) [7:0] :** This field is the Pixel Address (Write mode) for an entry in the CLUT. At the conclusion of every third write to the Pixel Data register (3C9), this address is incremented by one.

7.10 3C9: Pixel Data Registe r

I/O Port Address: 3C9

Index: –

Bit	Description	Reset Stat e
7	Pixel Data Bit [7]	0
6	Pixel Data Bit [6]	0
5	Pixel Data Bit [5]	0
4	Pixel Data Bit [4]	0
3	Pixel Data Bit [3]	0
2	Pixel Data Bit [2]	0
1	Pixel Data Bit [1]	0
0	Pixel Data Bit [0]	0

This register contains the Pixel Data for the palette DAC.

Bit	Descriptio n
7:0	**Pixel Data [7:0]**: These read/write register bits store the Pixel Data for the palette DAC. Writing to this register: • Prior to writing to this register, register 3C8 (the Pixel Address Write Mode register) is written with the first or only pixel address. • Three values, corresponding to the red, green, and blue values for the pixel, are then written to this address. • Following the third write, values are transferred to the CLUT. • The Pixel Address is incremented, in case new values for the next pixel address are to be written. Reading from this register: • Prior to reading from this register, register 3C7 (the Pixel Address Read Mode register) is written with the first or only pixel address. • Three values, corresponding to the red, green, and blue values for the pixel, are then read from this address. • Following the third read, the Pixel Address is incremented, in case new values for the next pixel address are to be read.

7.11 PCI00: PCI Device ID / PCI Vendor ID Registe r

PCI Configuration Address: 00

Index: –

Bit	Description	Reset State
31	PCI Device ID [15]	0
30	PCI Device ID [14]	0
29	PCI Device ID [13]	0
28	PCI Device ID [12]	1
27	PCI Device ID [11]	0
26	PCI Device ID [10]	0
25	PCI Device ID [9]	1
24	PCI Device ID [8]	0
23	PCI Device ID [7]	0
22	PCI Device ID [6]	0
21	PCI Device ID [5]	0
20	PCI Device ID [4]	0
19	PCI Device ID [3]	0
18	PCI Device ID [2]	0
17	PCI Device ID [1]	0
16	PCI Device ID [0]	0
15	PCI Vendor ID [15]	0
14	PCI Vendor ID [14]	0
13	PCI Vendor ID [13]	0
12	PCI Vendor ID [12]	1
11	PCI Vendor ID [11]	0
10	PCI Vendor ID [10]	0
9	PCI Vendor ID [9]	0
8	PCI Vendor ID [8]	0
7	PCI Vendor ID [7]	0
6	PCI Vendor ID [6]	0
5	PCI Vendor ID [5]	0
4	PCI Vendor ID [4]	1
3	PCI Vendor ID [3]	0
2	PCI Vendor ID [2]	0
1	PCI Vendor ID [1]	1
0	PCI Vendor ID [0]	1

This register is accessible and effective only if the CL-GD7541/GD7543 is configured for PCI bus. It contains the PCI Device ID and the PCI Vendor ID required for PCI compliance.

Bit	Descriptio n
31:16	**PCI Device ID [15:0]:** When the CL-GD7541/GD7543 is configured for PCI bus, this read-only field returns the PCI device ID assigned by Cirrus Logic. The CL-GD7541 PCI device ID is 1204h. The CL-GD7543 PCI device ID is 1202h.
15:0	**PCI Vendor ID [15:0]:** When the CL-GD7541/GD7543 is configured for PCI bus, this read-only field returns 1013h, the PCI vendor ID assigned to Cirrus Logic by the PCI Special Interest Group.

7.12 PCI04: PCI Command Register

PCI Configuration Address: 04

Index: –

Bit	Description	Reset State
15	Reserved	
14	Reserved	
13	Reserved	
12	Reserved	
11	Reserved	
10	Reserved	
9	Reserved	
8	Reserved	
7	Reserved	
6	Reserved	
5	PCI DAC Shadowing Enable	0
4	Reserved	
3	Reserved	
2	Reserved	
1	Display Memory Accesses Enable	0
0	I/O Accesses Enable	0

This 16-bit register is accessible and effective only if the CL-GD7541/GD7543 is configured for PCI bus. It consists of the least-significant two bytes of the PCI Status / PCI Command register.

Bit	Description
15:6	**Reserved:** These bits are reserved and *must* be programmed to 0.
5:	**PCI DAC Shadowing Enable :** When the CL-GD7541/GD7543 is configured for PCI bus *and* this bit is set to 1: • PCI DAC shadowing is enabled. • Read accesses are executed normally. • Write accesses to the CL-GD7541/GD7543 are executed, in that data bits are latched in the appropriate palette register. However, the CL-GD7541/GD7543 does not acknowledge the access.
4:2	**Reserved:** These bits are reserved and *must* be programmed to 0.
1	**Display Memory Accesses Enable :** When the CL-GD7541/GD7543 is configured for PCI bus and this bit is: • 1, display memory accesses are enabled to the CL-GD7541/GD7543. • 0, display memory accesses are not enabled to the CL-GD7541/GD7543.
0	**I/O Accesses Enable:** • When the CL-GD7541/GD7543 is configured for PCI bus and this bit is: — 1, I/O accesses are enabled to the CL-GD7541/GD7543. — 0, I/O accesses are not enabled to the CL-GD7541/GD7543. • Regardless of the state of this bit, I/O accesses to PCI configuration registers (PC100, PC104, PC110, and PC13C) are always enabled.

7.13 PCI04: PCI Status Register

PCI Configuration Address: 04

Index: –

Bit	Description	Reset Stat e
31	Reserved	
30	Reserved	
29	Reserved	
28	Reserved	
27	Reserved	
26	DEVSEL# Timing [1]	0
25	DEVSEL# Timing [0]	0
24	Reserved	
23	Reserved	
22	Reserved	
21	Reserved	
20	Reserved	
19	Reserved	
18	Reserved	
17	Reserved	
16	Reserved	

This 16-bit register, which is accessible and effective only if the CL-GD7541/GD7543 is configured for PCI bus, consists of the most-significant two bytes of the PCI Status / PCI Command register.

Bit	Descriptio n
31:27	**Reserved**
26:25	**DEVSEL# Timing [1:0] :** When the CL-GD7541/GD7543 is configured for PCI bus, this read-only field always returns the value 00 to indicate fast DEVSEL# timing.
24:16	**Reserve d**

7.14 PCI10: PCI Base Address Register

PCI Configuration Address: 10 Hex

Index: –

Bit	Description	Reset State
31	PCI Base Address for Display Memory [31]	0
30	PCI Base Address for Display Memory [30]	0
29	PCI Base Address for Display Memory [29]	0
28	PCI Base Address for Display Memory [28]	0
27	PCI Base Address for Display Memory [27]	0
26	PCI Base Address for Display Memory [26]	0
25	PCI Base Address for Display Memory [25]	0
24	PCI Base Address for Display Memory [24]	0
23:1	Reserved	
0	Display Memory / I/O Indicator	0

This 32-bit register, which is accessible and effective only when the CL-GD7541/GD7543 is configured for PCI bus, contains the PCI Base Address for display memory.

Bit	Description
31:24	**PCI Base Address for Display Memory [31:24] :** When the CL-GD7541/GD7543 is configured for PCI bus, this field contains the base address of the contiguous 16-Mbyte display memory block reserved for the CL-GD7541/GD7543.
23:1	**Reserved**
0	**Display Memory / I/O Indicator :** • When the CL-GD7541/GD7543 is configured for PCI bus, this bit is used to indicate the type of address space requested, either display memory or I/O. When this bit is: — 0, a display memory address space is requested. — 1, an I/O address space is requested. • For the PCI BIOS, this bit is read/write. • For the VGA BIOS, this bit is read-only.

7.15 PCI3C: PCI Interrupt Pin and PCI Interrupt Line Register

PCI Configuration Address: 3C Hex

Index: –

Bit	Description	Reset State
15	PCI Interrupt Pin [7]	0
14	PCI Interrupt Pin [6]	0
13	PCI Interrupt Pin [5]	0
12	PCI Interrupt Pin [4]	0
11	PCI Interrupt Pin [3]	0
10	PCI Interrupt Pin [2]	0
9	PCI Interrupt Pin [1]	0
8	PCI Interrupt Pin [0]	1
7	PCI Interrupt Line [7]	0
6	PCI Interrupt Line [6]	0
5	PCI Interrupt Line [5]	0
4	PCI Interrupt Line [4]	0
3	PCI Interrupt Line [3]	0
2	PCI Interrupt Line [2]	0
1	PCI Interrupt Line [1]	0
0	PCI Interrupt Line [0]	0

This register, which is accessible and effective only when the CL-GD7541/GD7543 is configured for PCI bus, contains data from the PCI Interrupt pin and PCI interrupt line.

Bit	Description
15:8	**PCI Interrupt Pin [7:0]:** When the CL-GD7541/GD7543 is configured for PCI bus, this read-only field contains the value 01h. This value indicates the CL-GD7541/GD7543 INTR# interrupt request pin is connected to the PCI bus INTA# interrupt request pin.
7:0	**PCI Interrupt Line [7:0]:** When the CL-GD7541/GD7543 is configured for PCI bus, this read/write field contains an 8-bit value that has no direct effect on the CL-GD7541/GD7543. This field is used to transfer an interrupt pointer from the PCI system BIOS to the CL-GD7541/GD7543 VGA BIOS.

7.16 46E8: Alternate Sleep Mode Register

I/O Port Address: 46E8

Index: –

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Alternate Sleep Mode Select	1
2	Reserved	
1	Reserved	
0	Reserved	

This register is active only when the following two conditions are both filled:

1) There is a low-to-high transition of the system reset signal.

2) An external pull-up resistor is on the S46 / MD[21] pin, which disables the 3C3 Sleep Mode register.

Unless both conditions are filled, register 3C3 is the sleep mode register.

Bit	Description
7:4	**Reserved**
3	**Alternate Sleep Mode Select:** When there is a pull-up resistor on the CL-GD7541/GD7543 pin S46 / MD[21] (that is, Extension register SR22[5] reads back a 1) *and* when this bit is: • 1, the CL-GD7541/GD7543: — Is enabled. — Can respond to normal bus and video display activity. • 0, the CL-GD7541/GD7543: — Is disabled and does not affect the video display activity. — Responds normally to BIOS access. — Does not respond to accesses to I/O, except to those addressed to 46E8. — Does not respond to any accesses to display memory.
2:0	**Reserved**

8. SEQUENCER REGISTERS

8.1 SRX: Sequencer Index Register

I/O Port Address: 3C4

Index: –

Bit	Description	Reset State
7	HW Cursor and HW Icon Fine Position [2]	0
6	HW Cursor and HW Icon Fine Position [1]	0
5	HW Cursor and HW Icon Fine Position [0] / Sequencer Index [5]	0
4	Sequencer Index [4]	0
3	Sequencer Index [3]	0
2	Sequencer Index [2]	0
1	Sequencer Index [1]	0
0	Sequencer Index [0]	0

Depending on this register's index value, this register has one of two possible purposes:

1) The primary purpose is to extend the sequencer index from 3 to 6 bits. The index specifies which register in the CL-GD7541/GD7543 sequencer block is to be accessed by the next I/O read or write to Address 3C5. If an index number is greater than 5, the index points to the Extension Registers in Chapter 12.

2) The secondary purpose is to specify the fine position of the hardware cursor and the hardware icon, both horizontal and vertical.

Bit	Description
7:5	**Hardware Cursor and Hardware Icon Fine Positions:** **Hardware Cursor and Hardware Icon Fine Vertical Positions [2:0]:** When Extension register SR11 is programmed, bits SRX[7:5] define in scanlines the fine vertical position of the hardware cursor and icon. **Hardware Cursor and Hardware Icon Fine Horizontal Positions [2:0]:** When Extension register SR10 is programmed, bits SRX[7:5] define in dot clocks (pixels) the fine horizontal position of the hardware cursor and icon. For special modes requiring extra dot clocks for fine position adjustments, a fourth, most-significant bit is in Extension registers SR2E and SR2A. • Hardware Cursor bit: Extension register SR2E[0] — For the fine horizontal position of the hardware cursor, SR2E[0] is an added fourth and most-significant bit. — This bit is used in horizontally expanded graphics modes. • Hardware Icon bit: Extension register SR2A[6] — For the fine horizontal position of the hardware icon, SR2A[6] is an added fourth and most-significant bit. — This bit is used in horizontally expanded graphics modes and for text modes with 9-dot and 10-dot fonts, such as 640 × 480 displays that are expanded to 800 × 600.

8.1 SRX: Sequencer Index Registe r *(cont.)*

Bit	Description
5:0	**Sequencer Index [5:0]:** • When writing to any CL-GD7541/GD7543 sequencer index *except* 10h or 11h: — These bits become a 6-bit sequencer index field, SRX[5:0]. — The SRX[5:0] field selects the register to be accessed with the next I/O read or I/O write to I/O Port Address 3C5. • When writing *to* CL-GD7541/GD7543 sequencer index 10h or 11h: — These bits become a 5-bit sequencer index field, SRX[4:0]. — The SRX[4:0] field selects the sequencer index, SRX[7:5], used to define the fine position for the hardware cursor and hardware icon. — Extension registers SR2A[6] and SR2E[0]) also define the fine position for the hardware cursor and hardware icon.

8.2 SR0: Reset Registe r

I/O Port Address: 3C5

Index: 0

Bit	Description	Reset Stat e
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	Reserved	
1	Synchronous Reset	1
0	Asynchronous Reset	1

This register is used to reset the CL-GD7541/GD7543 sequencer. These bits are for VGA-standard compatibility only, and after reset they need never be used.

Bit	Descriptio n
7:2	**Reserve d**
1	**Synchronous Rese t:** When this bit is programmed to: • 0, the sequencer is cleared and halted, which disables screen refresh and display memory refresh. • 1, and when SR0[0] is 1, the sequencer operates normally.
0	**Asynchronous Rese t:** When this bit is programmed to: • 0, the sequencer is cleared and halted, and SR3 is cleared. • 1, and when SR0[1] is 1, the sequencer operates normally.

8.3 SR1: Clocking Mode Register

I/O Port Address: 3C5

Index: 1

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Full Display Memory Bandwidth	0
4	Shift and Load 32 Data Bits	0
3	Dot Clock Generation	0
2	Shift and Load 16 Data Bits	0
1	Reserved	
0	8/9 Dot Clock	0

This register is used to control miscellaneous functions in the CL-GD7541/GD7543 sequencer.

Bit — **Description**

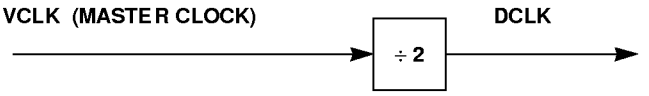
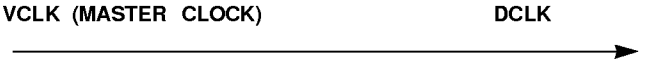
7:6 — **Reserved**

5 — **Full Display Memory Bandwidth :**
When this bit is programmed to:
- 0, the CRT screen is turned on, and the CL-GD7541/GD7543 operates normally.
- 1, the CRT screen is turned off. In addition:
  - — The CPU uses nearly 100% of the display memory bandwidth.
  - — HSYNC and VSYNC continue normally.
  - — The BLANK# signal goes active and stays active.
  - — The refresh for the display memory continues normally.

4 — **Shift and Load 32 Data Bits :**
This bit, in conjunction with SR1[2], controls how often 32-bit graphics controller display data shifters are loaded, according to the following table:

SR1 [4]	SR1 [2]	Frequency with Which Data Shifters Are Loaded
0	0	Every character clock
0	1	Every 2nd character clock
1	X	Every 4th character clock

8.3 SR1: Clocking Mode Registe r *(cont.)*

Bit	Description
3	**Dot Cloc k Generatio n:** When this bit is programmed to: • 1, VCLK (the master clock) is divided by 2 to generate DCLK, a dot clock that is half the frequency of the master clock. This dot clock is used for low-resolution Graphics modes such as 0h, 1h, 4h, 5h, and Dh.  • 0, VCLK (the master clock) is not divided by 2. In this case, the clock that is used as the dot clock is the same frequency as the master clock. 
2	**Shift and Load 16 Data Bits :** This bit controls how often 16-bit graphics controller display data shifters are loaded. (Refer to the description of bit [4] of this register.)
1	**Reserve d**
0	**8/9 Dot Clock :** For a display that is 80 characters per horizontal scanline, this bit must be: • 0 to generate character clocks that are 8 dots wide, as required by modes that use 320 or 640 horizontal dots. • 1 to generate character clocks that are 9 dots wide, as required by modes that use 720 horizontal dots.

8.4 SR2: Plane Mask Register

I/O Port Address: 3C5

Index: 2

Bit	Description	Reset State
7	Pixel Data Bit [7] Write Enable / Reserved	0
6	Pixel Data Bit [6] Write Enable / Reserved	0
5	Pixel Data Bit [5] Write Enable / Reserved	0
4	Pixel Data Bit [4] Write Enable / Reserved	0
3	Pixel Data Bit [3] Write Enable / Bit-Map Plane 3 Enable	0
2	Pixel Data Bit [2] Write Enable / Bit-Map Plane 2 Enable	0
1	Pixel Data Bit [1] Write Enable / Bit-Map Plane 1 Enable	0
0	Pixel Data Bit [0] Write Enable / Bit-Map Plane 0 Enable	0

This register has two uses.

1) Its first use is to control the writing of up to eight pixels.

2) Its second use is to enable or disable writing to the four bit-map planes of display memory .

Bit	Descriptio n
7:0	**Pixel Data Bit Write Enable [7:0] :** • These bits can control whether individual pixel data bits [7:0] are written. • To enable an individual pixel, the corresponding Enable Writing Pixel bit must be set to 1, and *one* of the following conditions must be met: — Extended Write mode 4 or Extended Write mode 5 is selected with Graphics Controller register bits GR5[2:0]. — Write mode 1 is selected with Graphics Controller register bits GR5[2:0], and Extension register GRB[2] is set to 1. • This field is also used to write protect the BitBLT (bit block transfer) engine.
7:4	**Reserved :** These 4 bits are reserved when Extended Write modes 4 and 5 are disabled (that is, Graphics Controller register bit GR5[2] = 0), which would be the case for VGA-compatibility modes.
3:0	**Bit-Map Plane Enable [3:0] :** These 4 bits are used to control whether individual display memory bit-map planes [3:0] are written with Write modes [3:0].

8.5 SR3: Character Map Set Select Register

I/O Port Address: 3C5

Index: 3

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Secondary Character Map Set Select [0]	0
4	Primary Character Map Set Select [0]	0
3	Secondary Character Map Set Select [2]	0
2	Secondary Character Map Set Select [1]	0
1	Primary Character Map Set Select [2]	0
0	Primary Character Map Set Select [1]	0

This register is used to specify the primary and the secondary character map sets (fonts). This register applies only to text modes.

Bit **Description**

7:6 **Reserved**

5, 3:2 **Secondary Character Map Set Select:**
These 3 bits select from among the secondary character map sets, according to the following table:

SR3			Secondary Character Map Set	Address Offset (Kbytes)
[5]	[3]	[2]		
0	0	0	0	0
0	0	1	1	16
0	1	0	2	32
0	1	1	3	48
1	0	0	4	8
1	0	1	5	24
1	1	0	6	40
1	1	1	7	56

8.5 SR3: Character Map Set Selec t Registe r *(cont.)*

Bit **Description**

4, 1:0 **Primary Character Map Set Select:**
These 3 bits select from among the primary character map sets, according to the following table:

SR3			Primary Character Map Se t	Address Offse t (Kbytes)
[4]	[1]	[0]		
0	0	0	0	0
0	0	1	1	16
0	1	0	2	32
0	1	1	3	48
1	0	0	4	8
1	0	1	5	24
1	1	0	6	40
1	1	1	7	56

NOTES:

1) In text video display modes:
   1. Character Map Plane 0 stores the ASCII text character code.
   2. Character Map Plane 1 stores the attribute byte.
   3. Character Map Plane 2 stores the character map set (the font) .

2) Bit 3 of the attribute byte normally controls the intensity of the foreground color.

   This bit may be redefined to be a switch between character sets, allowing 512 displayable characters.

   This switch is enabled whenever SR4[1] is a 1 *and* there is a difference between the values of the Primary Cha r-acter Map Set Select and the values of the Secondary Character Map Set Select .

3) The format for the Character Map Plane 2 font address bits [15:0] is :

   F2 F1 F0 C7 C6 C5 C4 C3 C2 C1 C0 R4 R3 R2 R1 R0

   where:

   F[2:0] is the character map set select
   C[7:0] is the ASCII text character code
   R[4:0] is the character row (the scanline in the character cell)

8.6 SR4: Memory Mode Register

I/O Port Address: 3C5

Index: 4

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Chain-4	0
2	Odd/Even Mode	0
1	Extended (Display) Memory	0
0	Reserved	

This register is used to control miscellaneous functions in the CL-GD7541/GD7543 sequencer.

Bit	Description
7:4	**Reserved**
3	**Chain-4:** When this bit is programmed to 1: • This bit takes priority over SR4[2] (Odd/Even mode) and Graphics Controller register GR5[4] (Odd/Even Addressing mode). • Its effect is similar to SR4[2] (Odd/Even mode), except both A0 and A1 are used. — Address A0 provides display memory Plane Select Bit [0]. — Address A1 provides display memory Plane Select Bit [1]. • The Graphics Controller Read Map register (GR4) is ignored.
2	**Odd/Even Mode:** • When this bit is programmed to 0, the sequencer is in Odd/Even mode. • This bit *must* be programmed to a 0 for text modes. • The value of this bit must track Graphics Controller register GR5[4] (Odd/Even Addressing mode), and the value of this register must be opposite the value of GR5[4]. — The even CPU addresses will access display memory planes 0 and 2. — The odd CPU addresses will access display memory planes 1 and 3. • This bit may be overridden by the SR4[3] bit.
1	**Extended (Display) Memory:** When this bit is programmed to: • 0, effective memory size is 64 Kbytes, regardless of actual installed memory. (EGA modes require this to be the case.) • 1, effective memory size equals actual installed memory.
0	**Reserved**

9. CRT CONTROLLER REGISTE RS

For the following registers, '?' in the I/O port address implies 'B' for Monochrome mode and 'D' for Color mode.

9.1 CRX: CRT Controller Index Register

I/O Port Address: 3?4

Index: (n/a)

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	CRTC Index [5]	0
4	CRTC Index [4]	0
3	CRTC Index [3]	0
2	CRTC Index [2]	0
1	CRTC Index [1]	0
0	CRTC Index [0]	0

This index register is used to specify the register in the CRTC (CRT Controller) block to be accessed by the next I/O read or I/O write to Address 3?5. Registers at indices 19, 1A, 1B, 25, and 27 are described in the Extension registers in Chapter 12.

Bit	Descriptio n
7:6	**Reserve d**
5:0	**CRTC Index [5:0] :** The value resulting from these bits point to the register to be accessed in the next I/O read or I/O write to address 3?5. (Note that registers above 18 were never documented by IBM.)

9.2 CR0: Horizontal Total Register

I/O Port Address: 3?5

Index: 0

Bit	Description	Reset State
7	Horizontal Total [7]	0
6	Horizontal Total [6]	0
5	Horizontal Total [5]	0
4	Horizontal Total [4]	0
3	Horizontal Total [3]	0
2	Horizontal Total [2]	0
1	Horizontal Total [1]	0
0	Horizontal Total [0]	0

This register is used to specify the total number of character clocks per horizontal period.

Bit **Description**

7:0 **Horizontal Total:**

- This 8-bit field specifies the total number of character clocks per horizontal period as follows:
  - — The VCLK signal provides the character clock. (The character clock is derived from VCLK, according to the character width.)
  - — The character counter counts the total number of character clocks.
  - — The value in the character counter is then compared with the value in this register to provide the basic horizontal timing.
  - — All horizontal and vertical timing is eventually derived from the basic horizontal timing in this register.
- The value of the horizontal total for this register is calculated as follows:

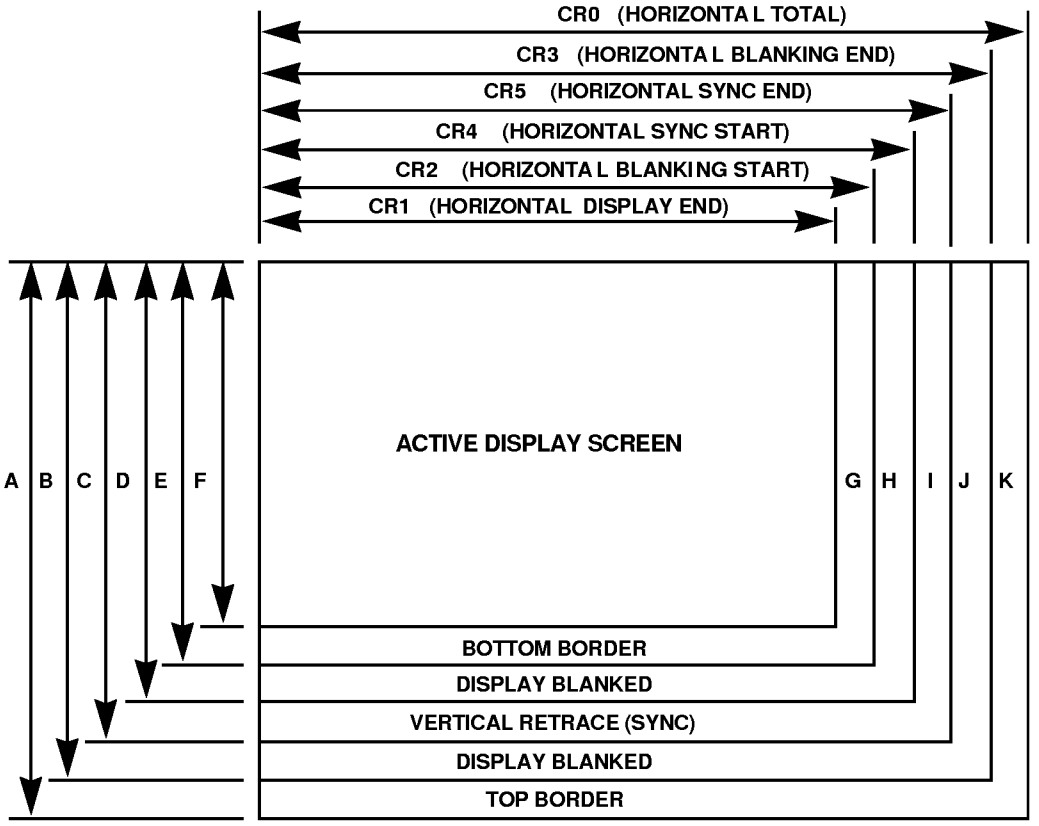
  FROM: Total number of character clocks (from character counter)
  SUBTRACT: – 5 character clocks (for standard VGA compatibility)
  TO OBTAIN: = Horizontal total

  Example: If 80 characters are desired per horizontal scanline, then a value of 75 must be loaded into this register.

- Figure 9-1 indicates the way the horizontal and vertical timing is defined.
  - — The horizontal timing is calculated in terms of character clock periods.
  - — The vertical timing is calculated in terms of horizontal periods.

Table 9-1 indicates how the various CRTC Timing registers are extended.

9.2 CR0: Horizontal Total Registe r *(cont.)*



A - CR6 (VERTICAL TOTAL)
B - CR16 (VERTICA L BLANKING END)
C - CR11 (VERTICAL SYNC END)
D - CR10 (VERTICAL SYNC START)
E - CR15 (VERTICAL BLANKING START)
F - CR12 (VERTICA L DISPLAY END)

G - RIGHT BORDER
H - DISPLAY BLANKED
I - HORIZONTAL RETRAC E (SYNC)
J - DISPLAY BLANKED
K - LEFT BORDER

Figure 9-1. CRT Controller Timing Register s

9.2 CR0: Horizontal Total Register *(cont.)*

Table 9-1 is a guide to the location of the CRT Controller Timing registers and accompanying extension and overflow bits.

- An extension bit is a bit added by Cirrus Logic to the standard VGA controller bits.
- An overflow bit is a standard VGA controller bit that results from using more than 8 bits to define a field.

Table 9-1. Summary of CRT Controller Timing Register Bits[a]

Parameter	CRT Controller Register Bit Position					
	[9]	[8]	[7]	[6]	[5]	[4:0]
H Total			CR0[7]	CR0[6]	CR0[5]	CR0[4:0]
H Display End			CR1[7]	CR1[6]	CR1[5]	CR1[4:0]
H Blanking Start			CR2[7]	CR2[6]	CR2[5]	CR2[4:0]
H Blanking End			**CR1A[5]**	**CR1A[4]**	CR5[7]	CR3[4:0]
H Sync Start			CR4[7]	CR4[6]	CR4[5]	CR4[4:0]
H Sync End						CR5[4:0]
V Total	CR7[5]	CR7[0]	CR6[7]	CR6[6]	CR6[5]	CR6[4:0]
V Sync Start	CR7[7]	CR7[2]	CR10[7]	CR10[6]	CR10[5]	CR10[4:0]
V Sync End						CR11[3:0]
V Display End	CR7[6]	CR7[1]	CR12[7]	CR12[6]	CR12[5]	CR12[4:0]
V Blanking Start	CR9[5]	CR7[3]	CR15[7]	CR15[6]	CR15[5]	CR15[4:0]
V Blanking End	**CR1A[7]**	**CR1A[6]**	CR16[7]	CR16[6]	CR16[5]	CR16[4:0]
Line Compare	CR9[6]	CR7[4]	CR18[7]	CR18[6]	CR18[5]	CR18[4:0]
Offset		**CR1B[4]**	CR13[7]	CR13[6]	CR13[5]	CR13[4:0]

[a] Bits shown in **bold** text are Cirrus Logic extensions.

9.3 CR1: Horizontal Display End Registe r

I/O Port Address: 3?5

Index: 1

Bit	Description	Reset Stat e
7	Horizontal Display End [7]	0
6	Horizontal Display End [6]	0
5	Horizontal Display End [5]	0
4	Horizontal Display End [4]	0
3	Horizontal Display End [3]	0
2	Horizontal Display End [2]	0
1	Horizontal Display End [1]	0
0	Horizontal Display End [0]	0

This register is used to specify the number of character clocks during horizontal display time.

Bit	Descriptio n
7:0	**Horizontal Display End [7:0] :** For the horizontal display time, this register specifies the number of character clocks, *minus 1*, as calculated for both text modes and graphics modes. • For text modes: CR1[7:0] = "Number of character clocks" – 1 Where number of character clocks = Number of characters • For graphics modes: CR1[7:0] = "Number of character clocks" – 1 Where number of character clocks = (Number of pixels/scanline) ÷ (Number of pixels/character clock) For a summary of CRTC Timing Registers, refer to Figure 9-1 and Table 9-1.

9.4 CR2: Horizontal Blanking Start Registe r

I/O Port Address: 3?5

Index: 2

Bit	Description	Reset Stat e
7	Horizontal Blanking Start [7]	0
6	Horizontal Blanking Start [6]	0
5	Horizontal Blanking Start [5]	0
4	Horizontal Blanking Start [4]	0
3	Horizontal Blanking Start [3]	0
2	Horizontal Blanking Start [2]	0
1	Horizontal Blanking Start [1]	0
0	Horizontal Blanking Start [0]	0

This register is used to specify the character count at which horizontal blanking starts.

Bit	Descriptio n
7:0	**Horizontal Blanking Start [7:0] :** This register specifies the character count at which horizontal blanking starts. • For text modes: Character count where horizontal blanking starts = Number of characters • For graphics modes: Character count at which horizontal blanking starts = (Number of pixels/scanline) ÷ (Number of pixels/character clock) • For both text modes and graphics modes: The value programmed into CR2 must always be larger than the value programmed into CRT Controller register CR1. For a summary of CRTC Timing registers, refer to Figure 9-1 and Table 9-1.

9.5 CR3: Horizontal Blanking End Register

I/O Port Address: 3?5

Index: 3

Bit	Description	Reset State
7	Compatible Read	0
6	Display Enable Delay [1]	0
5	Display Enable Delay [0]	0
4	Horizontal Blanking End [4]	0
3	Horizontal Blanking End [3]	0
2	Horizontal Blanking End [2]	0
1	Horizontal Blanking End [1]	0
0	Horizontal Blanking End [0]	0

This register is used to determine the horizontal blanking period width. Also, this register controls access to CRT Controller registers CR10 and CR11 and the display enable delay.

Bit **Description**

7 **Compatible Read:**
When this bit is:
- 0, CRTC registers CR10 and CR11 are write-only registers.
- 1, CRTC registers CR10 and CR11 are read/write registers.

6:5 **Display Enable Delay [1:0]:**
This 2-bit field is used to specify the number of character clocks that the display enable signal is delayed from the horizontal total. This delay is necessary to compensate for the accesses of the character code, attribute byte, font, etc.

The following table indicates programming for the display enable signal delay:

CR3		Delay for Display Enable Signal (in number of character clocks)
[6]	[5]	
0	0	No delay
0	1	1 character clock (typical setting)
1	0	2 character clocks
1	1	3 character clocks

NOTE: If the delay is programmed too low, the left-most character repeats. If the delay is programmed too high, one or more characters disappear at the left of each character row.

9.5 CR3: Horizontal Blanking End Register *(cont.)*

Bit	Description
4:0	**Horizontal Blanking End [4:0]:** • The horizontal blanking end field determines the width of the horizontal blanking period. This field consists of these 5 bits (and as needed, a sixth bit in CR5[7]). • The least-significant 5 (or 6) bits of the character counter are compared with the contents of this field. When a match occurs, the horizontal blanking period ends. • The horizontal blanking end value to be programmed into this register is calculated as follows: FROM: Horizontal blanking start (value programmed into CR2) SUBTRACT: – Horizontal blanking period (as desired) TO OBTAIN: Horizontal blanking end • The horizontal blanking period: — Must never be programmed to extend past the horizontal total. — Is limited to 63 character-clock times. • The horizontal blanking end field is extended as follows: — CR5[7] is the horizontal blanking end field bit [5], which extends this field to 6 bits. — When either Extension register CR1B[5] is 1 or Extension register CR1B[7] is 1, Extension register bits CR1A[5:4] further extend the horizontal blanking end field to 8 bits with bits [7:6]. For a summary of CRTC Timing registers, refer to Figure 9-1 and Table 9-1.

9.6 CR4: Horizontal Sync Start Registe r

I/O Port Address: 3?5

Index: 4

Bit	Description	Reset Stat e
7	Horizontal Sync Start [7]	0
6	Horizontal Sync Start [6]	0
5	Horizontal Sync Start [5]	0
4	Horizontal Sync Start [4]	0
3	Horizontal Sync Start [3]	0
2	Horizontal Sync Start [2]	0
1	Horizontal Sync Start [1]	0
0	Horizontal Sync Start [0]	0

This register specifies the time when horizontal synchronization becomes active.

Bit	Descriptio n
7:0	**Horizontal Sync Start [7:0] :** This field specifies the character count at which the horizontal synchronization signal becomes active. Adjusting the value in this field moves the display horizontally on the screen. • The horizontal sync start must be programmed to a value either equal to or greater than horizontal display end. • The time from horizontal sync start to horizontal total must be either equal to or greater than four character-clock times. For a summary of CRTC Timing registers, refer to Figure 9-1 and Table 9-1.

9.7 CR5: Horizontal Sync End Registe r

I/O Port Address: 3?5

Index: 5

Bit	Description	Reset Stat e
7	Horizontal Blanking End [5]	0
6	Horizontal Sync Delay [1]	0
5	Horizontal Sync Delay [0]	0
4	Horizontal Sync End [4]	0
3	Horizontal Sync End [3]	0
2	Horizontal Sync End [2]	0
1	Horizontal Sync End [1]	0
0	Horizontal Sync End [0]	0

This register specifies the position where the horizontal synchronization pulse ends, effectively specifying the width of the pulse. In addition, this register contains an overflow bit and a field for the horizontal synchronization delay.

Bit — **Descriptio n**

7 — **Horizontal Blanking End [5] :**
This overflow bit increases by one bit the horizontal blanking end value of CR3[4:0].

6:5 — **Horizontal Sync Delay [1:0] :**
This 2-bit field is used to specify the number of character clocks that the external horizontal synchronization pulse is delayed from the horizontal synchronization start position implied in CR4.

In some graphics modes, this horizontal synchronization delay is necessary to allow internal timing signals that are triggered from horizontal synchronization start to begin, prior to display enable.

The following table summarizes programming for the horizontal synchronization delay:

CR5		Delay for Horizontal Synchronization Pulse (in number of character clocks)
[6]	[5]	
0	0	No delay
0	1	1 character-clock dela y
1	0	2 character-clock dela y
1	1	3 character-clock dela y

9.7 CR5: Horizontal Sync End Registe r *(cont.)*

Bit	Descriptio n
4:0	**Horizontal Sync End [4:0]:** • The horizontal synchronization end field determines the width of the horizontal synchronization pulse. • The least-significant 5 bits of the character counter are compared with the contents of this field. When a match occurs, the horizontal synchronization pulse ends. • The horizontal synchronization end value to be programmed into this register is calculated as follows: FROM: Horizontal synchronization start (value programmed in CR4) SUBTRACT: – Horizontal synchronization pulse width (as desired) TO OBTAIN: = Horizontal synchronization end • The horizontal synchronization pulse: — Has a width limited to 31 character-clock times. — Must never be programmed to extend past the horizontal total of CR0. — Must always end during the horizontal blanking period. For a summary of CRTC Timing registers, refer to Figure 9-1 and Table 9-1.

9.8 CR6: Vertical Total Registe r

I/O Port Address: 3?5

Index: 6

Bit	Description	Reset Stat e
7	Vertical Total [7]	0
6	Vertical Total [6]	0
5	Vertical Total [5]	0
4	Vertical Total [4]	0
3	Vertical Total [3]	0
2	Vertical Total [2]	0
1	Vertical Total [1]	0
0	Vertical Total [0]	0

This register specifies the total number of scanlines per frame.

Bit	Descriptio n
7:0	**Vertical Total [7:0]:** • This vertical total field, a 10-bit field that consists of these 8 bits and the 2 bits in CR7[5] and CR7[0], defines the total number of scanlines per frame. • The value of the Vertical Total field to be programmed is calculated as follows: FROM: Total number of horizontal scanlines SUBTRACT: – 2 scanlines TO OBTAIN: = Vertical Total field (total number of scanlines per frame) When the value in the scanline counter equals the value of the Vertical Total field, a vertical retrace period begins. For a summary of CRTC Timing registers, refer to Figure 9-1 and Table 9-1.

9.9 CR7: Overflow Registe r

I/O Port Address: 3?5

Index: 7

Bit	Description	Reset Stat e
7	Vertical Sync Start [9]	0
6	Vertical Display End [9]	0
5	Vertical Total [9]	0
4	Line Compare [8]	0
3	Vertical Blanking Start [8]	0
2	Vertical Sync Start [8]	0
1	Vertical Display End [8]	0
0	Vertical Total [8]	0

This register contains bits that extend various vertical count fields. For a summary of CRTC Timing registers, refer to Figure 9-1 and Table 9-1.

Bit	Descriptio n
7	**Vertical Sync Start [9]:** With CR7[2], this bit extends the vertical sync start field (CR10) to 10 bits.
6	**Vertical Display End [9] :** With CR7[1], this bit extends the vertical display end field (CR12) to 10 bits.
5	**Vertical Total [9] :** With CR7[0], this bit extends the vertical total field (CR6) to 10 bits.
4	**Line Compare [8] :** With CR9[6], this bit extends the line compare field (CR18) to 10 bits. This bit can always be written.
3	**Vertical Blanking Start [8] :** With CR9[5], this bit extends the vertical blanking start field (CR15) to 10 bits.
2	**Vertical Sync Start [8] :** With CR7[7], this bit extends the vertical sync start field (CR10) to 10 bits.
1	**Vertical Display End [8] :** With CR7[6], this bit extends the vertical display end field (CR12) to 10 bits.
0	**Vertical Total [8] :** With CR7[5], this bit extends the vertical total field (CR6) to 10 bits.

9.10 CR8: Screen A Preset Row Scan Register

I/O Port Address: 3?5

Index: 8

Bit	Description	Reset State
7	Reserved	
6	Byte (Coarse) Panning [1]	0
5	Byte (Coarse) Panning [0]	0
4	Screen A Preset Row Scan [4]	0
3	Screen A Preset Row Scan [3]	0
2	Screen A Preset Row Scan [2]	0
1	Screen A Preset Row Scan [1]	0
0	Screen A Preset Row Scan [0]	0

This register specifies the row scanline at which Screen A starts. This register also allows two types of scrolling:

- Scrolling on a character row (scanline) basis (also called coarse panning).
- Scrolling on a scanline (row) basis, also called fine scroll.

In addition, this register specifies byte (coarse) panning.

Bit — **Description**

7 — **Reserved**

6:5 — **Byte (Coarse) Panning [1:0]:**
This 2-bit field controls coarse panning. (For fine panning on a pixel-by-pixel basis, refer to Attribute Controller register AR13.)

- This field can specify a coarse pan of up to 24 pixels, with 8-pixel resolution.
- Values for CR8[6:5] are interpreted as indicated in the following table:

CR8		Resulting Pan (in bytes)	Resulting Pan (in pixels)
[6]	[5]		
0	0	0	0
0	1	1	8
1	0	2	16
1	1	3	24

4:0 — **Screen A Preset Row Scan [4:0]:**
This field specifies the scanline at which the first character row begins.

- This specification provides scrolling on a scanline basis (soft scrolling).
- The contents of this field must be changed only during vertical retrace.

9.11 CR9: Character Cell Height Registe r

I/O Port Address: 3?5

Index: 9

Bit	Description	Reset Stat e
7	Scanline Double Control	0
6	Line Compare [9]	0
5	Vertical Blanking Start [9]	0
4	Character Cell Height [4]	0
3	Character Cell Height [3]	0
2	Character Cell Height [2]	0
1	Character Cell Height [1]	0
0	Character Cell Height [0]	0

This register specifies the number of scanlines in the character cell. In addition, it contains two overflow bits and one control bit.

Bit	Descriptio n
7	**Scanline Double Contro l:** When this bit is 1, every scanline is displayed twice in succession. • Scanlines double for those specifications based on scanline counter address-ing, such as Character Height, Cursor Start, Cursor End, and Cursor Underline location. • Typically, this bit is used to double a 200-scanline display to 400 scanlines. • The scanline doubling function is not available in interlaced graphics modes.
6	**Line Compare [9] :** With CR7[4], this bit extends the line compare field (CR18) to 10 bits.
5	**Vertical Blanking Start [9] :** With CR7[3], this bit extends the vertical blanking start field (CR15) to 10 bits.
4:0	**Character Cell Height [4:0] :** This field specifies the vertical size of the character cell in terms of scanlines. The value programmed into this field equals the actual size of the character cell (in scanlines) minus 1.

9.12 CRA: Text Cursor Start Register

I/O Port Address: 3?5

Index: A

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Text Cursor Disable	0
4	Text Cursor Start [4]	0
3	Text Cursor Start [3]	0
2	Text Cursor Start [2]	0
1	Text Cursor Start [1]	0
0	Text Cursor Start [0]	0

This register contains a bit that can disable the text cursor. In addition, this register specifies the scanline at which the text cursor is to start.

Bit	Description
7:6	**Reserved**
5	**Text Cursor Disable:** When this bit is: • 1, the text cursor is disabled (that is, it is removed). • 0, the text cursor functions normally.
4:0	**Text Cursor Start [4:0] :** This field specifies the scanline within the character cell at which the text cursor is to start. When the Text Cursor Start value is: • Less than or greater than the Text Cursor End value, no text cursor displays. • Equal to the Text Cursor End value, the text cursor displays on a single scan-line.

9.13 CRB: Text Cursor End Registe r

I/O Port Address: 3?5

Index: B

Bit	Description	Reset Stat e
7	Reserved	
6	Text Cursor Delay [1]	0
5	Text Cursor Delay [0]	0
4	Text Cursor End [4]	0
3	Text Cursor End [3]	0
2	Text Cursor End [2]	0
1	Text Cursor End [1]	0
0	Text Cursor End [0]	0

This register specifies the scanline at which the text cursor is to end. It also contains a field that allows the text cursor display to be delayed from the location specified in CRE and CRF.

Bit	Descriptio n
7	**Reserve d**
6:5	**Text Cursor Delay [1:0]:** This 2-bit field specifies a delay, given in character clocks, from the text cursor location specified in CRE and CRF to the actual display of the text cursor.
4:0	**Text Cursor End [4:0] :** This field specifies the scanline within the character cell at which the text cursor is to end. When the Text Cursor End value is: • Less than or equal to the character cell height, no text cursor displays. • Greater than the character cell height, the effective text cursor end value is equal to the character cell height.

9.14 CRC: Screen A Start Address High Registe r

I/O Port Address: 3?5

Index: C

Bit	Description	Reset Stat e
7	Screen A Start Address [15]	0
6	Screen A Start Address [14]	0
5	Screen A Start Address [13]	0
4	Screen A Start Address [12]	0
3	Screen A Start Address [11]	0
2	Screen A Start Address [10]	0
1	Screen A Start Address [9]	0
0	Screen A Start Address [8]	0

This register, along with CRD and Extension register bits CR1B[3:2, 0], specifies the display memory location where data to be displayed on the screen starts.

Bit	Descriptio n
7:0	**Screen A Start Address [15:8] :** The 19-bit Screen A Start Address field contains a value that specifies the starting display memory location for data to be displayed on the screen. • Bits [18:16] are in Extension register CR1B[3:2,0]. • Bits [15:8] are in this register. • Bits [7:0] are in CRT Controller register CRD.

9.15 CRD: Screen A Start Address Low Registe r

I/O Port Address: 3?5

Index: D

Bit	Description	Reset Stat e
7	Screen A Start Address [7]	0
6	Screen A Start Address [6]	0
5	Screen A Start Address [5]	0
4	Screen A Start Address [4]	0
3	Screen A Start Address [3]	0
2	Screen A Start Address [2]	0
1	Screen A Start Address [1]	0
0	Screen A Start Address [0]	0

This register, along with CRC and Extension register CR1B[3:2, 0], specify the display memory location where data to be displayed on the screen starts.

Bit	Descriptio n
7:0	**Screen A Start Address [7:0] :** The 19-bit Screen A Start Address field contains a value that specifies the starting display memory location for data to be displayed on the screen. • Bits [18:16] are in Extension register CR1B[3:2,0]. • Bits [15:8] are in CRT Controller register CRC. • Bits [7:0] are in this register.

9.16 CRE: Text Cursor Location High Registe r

I/O Port Address: 3?5

Index: E

Bit	Description	Reset Stat e
7	Text Cursor Location [15]	0
6	Text Cursor Location [14]	0
5	Text Cursor Location [13]	0
4	Text Cursor Location [12]	0
3	Text Cursor Location [11]	0
2	Text Cursor Location [10]	0
1	Text Cursor Location [9]	0
0	Text Cursor Location [8]	0

This register, along with CRF, specifies the display memory location where the text cursor is to be displayed.

Bit	Descriptio n
7:0	**Text Cursor Location [15:8] :** The Text Cursor Location is a 16-bit field that specifies the display memory location where the text cursor is to be displayed. • Bits [15:8] are in this register. • Bits [7:0] are in CRT Controller register CRF. • The value contained in this field specifies an address in display memory, not an offset from the beginning of the screen. When the value of the Screen A Start is changed without a compensating change in the Text Cursor Location field, the text cursor moves on the screen.

9.17 CRF: Text Cursor Location Low Register

I/O Port Address: 3?5

Index: F

Bit	Description	Reset State
7	Text Cursor Location [7]	0
6	Text Cursor Location [6]	0
5	Text Cursor Location [5]	0
4	Text Cursor Location [4]	0
3	Text Cursor Location [3]	0
2	Text Cursor Location [2]	0
1	Text Cursor Location [1]	0
0	Text Cursor Location [0]	0

This register, with CRE, specifies the display memory location where the text cursor is to be displayed.

Bit	Description
7:0	**Text Cursor Location [7:0] :** The Text Cursor Location is a 16-bit field that specifies the display memory location where the text cursor is to be displayed. • Bits [15:8] are in CRT Controller register CRE. • Bits [7:0] are in this register.

9.18 CR10: Vertical Sync Start Registe r

I/O Port Address: 3?5

Index: 10

Bit	Description	Reset Stat e
7	Vertical Sync Start [7]	0
6	Vertical Sync Start [6]	0
5	Vertical Sync Start [5]	0
4	Vertical Sync Start [4]	0
3	Vertical Sync Start [3]	0
2	Vertical Sync Start [2]	0
1	Vertical Sync Start [1]	0
0	Vertical Sync Start [0]	0

The Vertical Sync Start field specifies the scanline at which the Vertical Sync pulse is to become active.

Access to this register is controlled by CRT Controller register CR3[7].

- When CR3[7] is 1, this register is read/write.
- When CR3[7] is 0, this register is write-only.

Bit	Descriptio n
7:0	**Vertical Sync Start [7:0] :** The Vertical Sync field specifies the scanline at which the Vertical Sync pulse is to become active. • This register contains the least-significant 8 bits [7:0] of that field. • Bits [9:8] in CRT Controller register CR7[7,2] extend this field to 10 bits. For a summary of CRTC Timing registers, refer to Figure 9-1 and Table 9-1.

9.19 CR11: Vertical Sync End Register

I/O Port Address: 3?5

Index: 11

Bit	Description	Reset State
7	CRT Controller Registers CR0:CR7 Write Protect	0
6	Refresh Cycle Control	0
5	Vertical Interrupt Disable	0
4	Vertical Interrupt Clear	0
3	Vertical Sync End [3]	0
2	Vertical Sync End [2]	0
1	Vertical Sync End [1]	0
0	Vertical Sync End [0]	0

This register specifies the scanline at which the Vertical Sync pulse is to become inactive, thereby effectively specifying the Vertical Sync pulse width. In addition, this register contains controls for the vertical interrupt and two miscellaneous control bits, CR11[7:6].

Access to this register is controlled by CR3[7].

- When CR3[7] is 1, this register is read/write.
- When CR3[7] is 0, this register is write-only.

Bit	Description
7	**CRT Controller Registers CR0:CR7 Write Protect:** When this bit is: • 0, CR0 through CR7 can be written normally. • 1, CR0 through CR7 cannot be written, except for CR7[4], which can always be written.
6	**Refresh Cycle Control:** When this bit is: • 0, three refresh cycles execute per scanline. • 1, five refresh cycles execute per scanline.
5	**Vertical Interrupt Disable:** When this bit is: • 0, vertical interrupt is enabled and functions normally. • 1, vertical interrupt is disabled, and the INTR pin cannot go active.
4	**Vertical Interrupt Clear:** When this bit is: • 0, the Interrupt Pending Bit (FEAT[7]) clears to 0, and the INTR pin is forced inactive. • 1, it has no effect.

9.19 CR11: Vertical Sync End Register *(cont.)*

Bit	Description
3:0	**Vertical Sync End [3:0]:** • This field determines the width of the Vertical Sync pulse. • The value of this field is compared with the least-significant 4 bits of the Scan-line Counter. When a match occurs, the Vertical Sync pulse is ended. • The Vertical Sync pulse is limited to 15 scanlines. • The vertical sync end value to be programmed into this register may be calculated as follows: FROM: Vertical sync start (value programmed in CR10 and CR7[7,2]) SUBTRACT: – Vertical sync width (as desired) TO OBTAIN: = Vertical sync end • The Vertical Sync pulse must never be programmed to extend past the Vertical Total. For a summary of CRTC Timing registers, refer to Figure 9-1 and Table 9-1.

9.20 CR12: Vertical Display End Registe r

I/O Port Address: 3?5

Index: 12

Bit	Description	Reset Stat e
7	Vertical Display End [7]	0
6	Vertical Display End [6]	0
5	Vertical Display End [5]	0
4	Vertical Display End [4]	0
3	Vertical Display End [3]	0
2	Vertical Display End [2]	0
1	Vertical Display End [1]	0
0	Vertical Display End [0]	0

The Vertical Display End field is used to specify the scanline at which the display is to end.

Bit	Descriptio n
7:0	**Vertical Display End [7:0] :** The Vertical Display End field is used to specify the scanline at which the display is to end. • The least-significant 8 bits [7:0] of this field are in this register. • The most-significant 2 bits [9:8] are in CRT Controller register CR7[6,1]. For a summary of CRTC Timing registers, refer to Figure 9-1 and Table 9-1.

9.21 CR13: Offset Registe r

I/O Port Address: 3?5

Index: 13

Bit	Description	Reset Stat e
7	Offset [7]	0
6	Offset [6]	0
5	Offset [5]	0
4	Offset [4]	0
3	Offset [3]	0
2	Offset [2]	0
1	Offset [1]	0
0	Offset [0]	0

This register specifies the display 'pitch,' which is the distance in the display memory between the beginnings of adjacent character rows or scanlines.

Bit	Descriptio n
7:0	**Offset [7:0] :** This register specifies the distance in display memory between the beginnings of adjacent character rows or scanlines. This field is extended to 9 bits with Extension register CR1B[4]. Except for the first scanline, to calculate the address from which to begin fetching data, add the contents of this register CR13 to the beginning address of the previous scanline or character row. As a result, depending on the value of CRT Controller register CR17[6], the offset shifts left either zero or one bit position.

9.22 CR14: Underline Row Scanline Registe r

I/O Port Address: 3?5

Index: 14

Bit	Description	Reset Stat e
7	Reserved	0
6	Double-Word Addressing Mode for Display Memory	0
5	Count by Four	0
4	Underline Scanline [4]	0
3	Underline Scanline [3]	0
2	Underline Scanline [2]	0
1	Underline Scanline [1]	0
0	Underline Scanline [0]	0

This register is used to enable or disable access to the Extension registers.

Bit	Descriptio n
7	**Reserve d**
6	**Double-Word Addressing Mode for Display Memor y:** When this bit is: • 0, CR17[6] controls whether the CL-GD7541/GD7543 uses the byte-address mode or the word-address mode. • 1, double-word addressing mode is selected. — The CRTC Memory Address Counter is rotated left for two bit positions. — As a result, display memory address bits MA[1] and MA[0] are sourced from CRTC Address Counter bits [13] and [12], respectively.
5	**Count by Four :** When Double-Word mode is: • Disabled (CR14[6] is 0), this bit must be cleared to 0. • Enabled (CR14[6] is 1), this bit must be set to 1 to clock the Memory Address Counter with Character Clock divided by four.
4:0	**Underline Scanline [4:0] :** Within a character cell, this field specifies the scanline at which the underline occurs.

9.23 CR15: Vertical Blanking Start Registe r

I/O Port Address: 3?5

Index: 15

Bit	Description	Reset Stat e
7	Vertical Blanking Start [7]	0
6	Vertical Blanking Start [6]	0
5	Vertical Blanking Start [5]	0
4	Vertical Blanking Start [4]	0
3	Vertical Blanking Start [3]	0
2	Vertical Blanking Start [2]	0
1	Vertical Blanking Start [1]	0
0	Vertical Blanking Start [0]	0

This register specifies the scanline at which blanking is to become active.

Bit	Descriptio n
7:0	**Vertical Blanking Start [7:0] :** This 10-bit field specifies the scanline at which vertical blanking is to start. • The least-significant 8 bits [7:0] of this field are in this register. • The most-significant 2 bits [9:8] of this field are in CRT Controller registers CR9[5] and CR7[3]. For a summary of CRTC Timing registers, refer to Figure 9-1 and Table 9-1.

9.24 CR16: Vertical Blanking End Registe r

I/O Port Address: 3?5

Index: 16

Bit	Description	Reset Stat e
7	Vertical Blanking End [7]	0
6	Vertical Blanking End [6]	0
5	Vertical Blanking End [5]	0
4	Vertical Blanking End [4]	0
3	Vertical Blanking End [3]	0
2	Vertical Blanking End [2]	0
1	Vertical Blanking End [1]	0
0	Vertical Blanking End [0]	0

The Vertical Blanking End field specifies the scanline at which vertical blanking is to end.

Bit	Descriptio n
7:0	**Vertical Blanking End [7:0] :** The Vertical Blanking End field specifies the scanline at which vertical blanking is to end. When Extension register CR1B[5] is: • 0, the entire field is the 8 bits of CRT Controller register CR16[7:0]. • 1, the field is extended to 10 bits with Extension register CR1A[7:6]. The contents of the Vertical Blanking End field are compared to the scanline counter to determine when to terminate vertical blanking. If Extension register CR1B[5] is: • 0, this comparison limits the duration of vertical blanking to 255 scanlines. • 1, this comparison does not limit the duration of vertical blanking to 255 scanlines. (That is, the duration of vertical blanking may be more than 255 scanlines.) For a summary of CRTC Timing registers, refer to Figure 9-1 and Table 9-1.

9.25 CR17: Mode Control Register

I/O Port Address: 3?5

Index: 17

Bit	Description	Reset State
7	CRT Controller Timing Logic Enable	0
6	Byte/Word Address Mode	0
5	Address Rotation	0
4	Reserved	
3	Count by Two	0
2	Multiply Vertical Registers by Two	0
1	Compatibility-Mode (Hercules) Support	0
0	Compatibility-Mode (CGA) Support	0

This register contains a number of miscellaneous control bits.

Bit	Description
7	**CRT Controller Timing Logic Enable:** When this bit is: • 1, CRT Controller timing logic is enabled and functions normally. • 0, CRT Controller timing logic is disabled, forcing a reset condition.
6	**Byte/Word Address Mode:** • When this bit is 1: — The Byte-Address mode is enabled. — Before the contents of the CRTC Address Counter are sent to display memory, they are not rotated. • When this bit is 0: — The Word-Address mode is enabled. — Before the contents of the CRTC Address Counter are sent to display memory, they are rotated left one bit position.
5	**Address Rotation:** • When CR17[6] is 1, this bit is ignored. • When CR17[6] is 0 *and* this bit is: — 1, the left rotation described in CR17[6] above involves 16 bits of the CRTC Address Counter. — 0, the left rotation described in CR17[6] above involves 14 bits of the CRTC Address Counter.
4	**Reserved**

9.25 CR17: Mode Control Register *(cont.)*

Bit	Description
3	**Count by Two:** When this bit is: • 1, the CL-GD7541/GD7543 clocks the Memory Address Counter with the Character Clock, divided by two. • 0, the CL-GD7541/GD7543 clocks the Memory Address Counter with the Character Clock.
2	**Multiply Vertical Registers by Two:** When this bit is: • 1, the Scanline Counter is clocked with Horizontal Sync, divided by two. (In effect, the Vertical registers are multiplied by two.) — This division allows the number of scanlines to be doubled to 2048. — All periods become even multiples of two scanlines. • 0, the Scanline Counter is clocked with Horizontal Sync. — As a result, the number of scanlines is 1024.
1	**Compatibility-Mode (Hercules) Support:** When this bit is: • 0, Scanline Counter bit [1] is substituted for CRTC Address Counter [14]. This substitution provides for Hercules™ compatibility. • 1, the substitution described above does not occur.
0	**Compatibility-Mode (CGA) Support:** When this bit is: • 0, Scanline Counter bit [0] is substituted for CRTC Address Counter [14]. This substitution provides for CGA compatibility. • 1, the substitution described above does not occur.

9.26 CR18: Line Compare Registe r

I/O Port Address: 3?5

Index: 18

Bit	Description	Reset Stat e
7	Line Compare [7]	0
6	Line Compare [6]	0
5	Line Compare [5]	0
4	Line Compare [4]	0
3	Line Compare [3]	0
2	Line Compare [2]	0
1	Line Compare [1]	0
0	Line Compare [0]	0

The Line Compare field is used to specify where Screen A ends and Screen B starts for a vertically split screen.

Bit	Descriptio n
7:0	**Line Compare [7:0] :** The 10-bit Line Compare field is used to implement a vertically split screen by specifying where Screen A ends and Screen B starts. • This register contains the least-significant 8 bits [7:0] of this field. • The most-significant 2 bits are in CRT Controller registers CR9[6] and CR7[4]. The top portion of the split screen is called Screen A. • Screen A may start anywhere in display memory. • Screen A can be panned and scrolled on a pixel-by-pixel basis. The bottom portion of the split screen is called Screen B. • Screen B always starts at location 0 in display memory. • Screen B cannot be panned or scrolled.

9.27 CR22: Graphics Controller Data Latches Readback Registe r

I/O Port Address: 3?5

Index: 22

Bit	Description	Reset Stat e
7	Graphics Controller Data Latch n Readback [7]	0
6	Graphics Controller Data Latch n Readback [6]	0
5	Graphics Controller Data Latch n Readback [5]	0
4	Graphics Controller Data Latch n Readback [4]	0
3	Graphics Controller Data Latch n Readback [3]	0
2	Graphics Controller Data Latch n Readback [2]	0
1	Graphics Controller Data Latch n Readback [1]	0
0	Graphics Controller Data Latch n Readback [0]	0

This register address is used to read the Graphics Controller Data Latches.

Bit	Descriptio n
7:0	**Graphics Controller Data Latch n Readback [7:0] :** This read-only register is used to read back the contents of one of the four VGA graphics controller display memory data latches. • The number of the display memory data latch that is read back is selected with Graphics Controller register GR4[1:0]. • The graphics controller data latches are loaded whenever display memory is read by the CPU.

9.28 CR24: Attribute Controller Toggle Readback Register

I/O Port Address: 3?5

Index: 24

Bit	Description	Reset State
7	Attribute Controller Data-Index Toggle Readback	0
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	Reserved	
1	Reserved	
0	Reserved	

This read-only register provides access to the Attribute Controller Toggle.

Bit	Description
7	**Attribute Controller Data-Index Toggle Readback:** When this bit is: • 1, on the next access, the Attribute Controller reads or writes a data value. • 0, on the next access, the Attribute Controller reads or writes an index value.
6:0	**Reserved**

9.29 CR26: Attribute Controller Index Readback Registe r

I/O Port Address: 3?5

Index: 26

Bit	Description	Reset Stat e
7	Reserved	
6	Reserved	
5	Video Enable Status	0
4	Attribute Controller Index Readback [4]	0
3	Attribute Controller Index Readback [3]	0
2	Attribute Controller Index Readback [2]	0
1	Attribute Controller Index Readback [1]	0
0	Attribute Controller Index Readback [0]	0

This read-only register provides access to the current Attribute Controller Index.

Bit	Descriptio n
7:6	**Reserve d**
5	**Video Enable Status :** This bit provides the status of the Video Enable bit in Attribute Controller Index register ARX[5].
4:0	**Attribute Controller Index Readback [4:0] :** This field reads back the value that is in Attribute Controller Index register ARX[4:0].

10. GRAPHICS CONTROLLER REGISTER S

10.1 GRX: Graphics Controller Index Register

I/O Port Address: 3CE

Index: (n/a)

Bit	Description	Reset Stat e
7	Reserved	
6	Reserved	
5	Graphics Controller Index [5]	0
4	Graphics Controller Index [4]	0
3	Graphics Controller Index [3]	0
2	Graphics Controller Index [2]	0
1	Graphics Controller Index [1]	0
0	Graphics Controller Index [0]	0

This register is used to specify a graphics controller register.

Bit	Descriptio n
7:6	**Reserve d**
5:0	**Graphics Controller Index [5:0] :** This field specifies one of the following: • A register in the Graphics Controller group. • An Extension register that is accessed by the next I/O read or I/O write to I/O port address 3CF.

10.2 GR0: Set / Reset Register

I/O Port Address: 3CF

Index: 0

Bit	Description	Reset State
7	Write Mode 5 Background Color [7] / Reserved	0
6	Write Mode 5 Background Color [6] / Reserved	0
5	Write Mode 5 Background Color [5] / Reserved	0
4	Write Mode 5 Background Color [4] / Reserved	0
3	Write Mode 5 Background Color [3] / Display Memory Plane 3 Set/Reset	0
2	Write Mode 5 Background Color [2] / Display Memory Plane 2 Set/Reset	0
1	Write Mode 5 Background Color [1] / Display Memory Plane 1 Set/Reset	0
0	Write Mode 5 Background Color [0] / Display Memory Plane 0 Set/Reset	0

This register specifies:

- The background color, when Extended Write mode 5 is selected.
- Values to be written into the respective display memory planes, when the processor executes a Write mode 0 or Write mode 3 operation.

For an overview of the Write modes, refer to the description in Graphics Controller register GR5.

Bit	Description
7:0	**Write Mode 5 Background Color [7:0] :** When Graphics Controller register GR5[2:0] selects Extended Write mode 5, these bits [7:0] specify the background color for Extended Write mode 5.
7:4	**Reserved:** • When Graphics Controller register GR5[2:0] does not select Extended Write mode 5, these bits [7:4] are reserved. • When Extension register GRB[2] is: — 0, writes to these bits are ignored, and reads return zeroes. — 1, these bits are read/write, but bit contents are not used.
3:0	**Display Memory Plane [3:0] Set/Reset :** When Graphics Controller register GR5[2:0] does not select Extended Write mode 5, these bits [3:0] control the values written into the respective display memory planes for Write mode 3 and Write mode 0.

10.3 GR1: Set / Reset Enable Register

I/O Port Address: 3CF

Index: 1

Bit	Description	Reset State
7	Write Mode 4, 5 Foreground Color [7] / Reserved	0
6	Write Mode 4, 5 Foreground Color [6] / Reserved	0
5	Write Mode 4, 5 Foreground Color [5] / Reserved	0
4	Write Mode 4, 5 Foreground Color [4] / Reserved	0
3	Write Mode 4, 5 Foreground Color [3] / Display Memory Plane 3 Set/Reset Enable	0
2	Write Mode 4, 5 Foreground Color [2] / Display Memory Plane 2 Set/Reset Enable	0
1	Write Mode 4, 5 Foreground Color [1] / Display Memory Plane 1 Set/Reset Enable	0
0	Write Mode 4, 5 Foreground Color [0] / Display Memory Plane 0 Set/Reset Enable	0

This register:

- Defines the foreground color when Extended Write mode 4 or 5 is selected.
- Is used with Graphics Controller register GR0 to determine values to be written into the respective display memory planes when Write mode 0 is selected.

For an overview of the Write modes, refer to the description in Graphics Controller register GR5.

Bit	Description
7:0	**Write Mode 4, 5 Foreground Color [7:0]:** These bits specify the foreground color for an Extended Write mode when the mode selected is: • Extended Write mode 4 (Graphics Controller register GR5[2:0] is 100). • Extended Write mode 5 (Graphics Controller register GR5[2:0] is 101).
7:4	**Reserved:** • When Graphics Controller register GR5[2:0] selects Extended Write mode 4 or 5, these bits [7:4] are reserved. • When Extension register GRB[2] is: — 0, writes to these bits are ignored, and reads return zeroes. — 1, these bits are read/write, but bit contents are not used.
3:0	**Display Memory Plane [3:0] Set/Reset Enable:** When Write mode 0 is selected (Graphics Controller register GR5[2:0] is 000) *and* when a bit in this field is: • 1, the corresponding value in Graphics Controller register GR0[3:0] is written into the corresponding display memory plane. • 0, the corresponding value from the CPU data bus is written into the corresponding display memory plane.

10.4 GR2: Color Compare Registe r

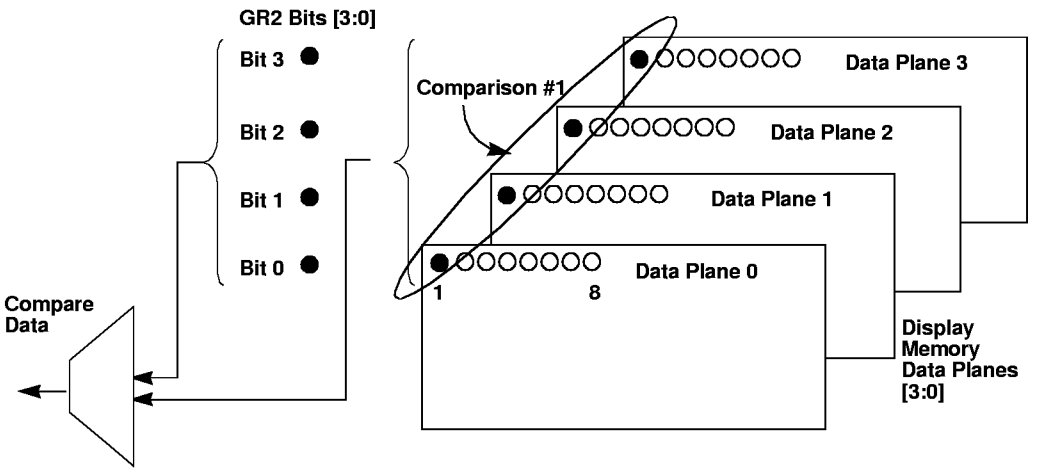
I/O Port Address: 3CF

Index: 2

Bit	Description	Reset Stat e
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Color Compare Plane [3]	0
2	Color Compare Plane [2]	0
1	Color Compare Plane [1]	0
0	Color Compare Plane [0]	0

This register specifies the color compare plane(s) for Read mode 1.

Bit	Descriptio n
7:4	**Reserve d**
3:0	**Color Compare Plane [3:0] :** This field represents a color comparison value consisting of 1 to 4 bits. • GR5[3] must be set to 1 (Read mode 1 is selected) to enable this field. • GR7[3:0] bits select display memory data planes for the comparison shown below. • For each selected display memory data plane, the color value of the corresponding bit in this field is compared to the color of the eight neighboring horizontal pixels in the corresponding display memory data plane. (For display memory data planes that are not chosen, their data is forced to match the values of the other data planes, becoming a 'don't care' in the process.) • The 8 bits from the comparison are read into the CPU.



10.5 GR3: Data Rotate Registe r

I/O Port Address: 3CF

Index: 3

Bit	Description	Reset Stat e
7	Reserved	
6	Reserved	
5	Reserved	
4	Logical Function Select [1]	0
3	Logical Function Select [0]	0
2	Data Rotate Count [2]	0
1	Data Rotate Count [1]	0
0	Data Rotate Count [0]	0

This register contains two fields that are used with Write modes 0 and 3.

Bit — **Descriptio n**

7:5 — **Reserve d**

4:3 — **Logical Function Select [1:0] :**

- This 2-bit field is used for Write mode 0 only (Graphics Controller register GR5[2:0] is 000).
- In addition, this 2-bit field selects the logical function operation that takes place between the data in the CPU data latches and the data from the CPU or Set/Reset Logic. The result of the functional operation is written into display memory.

The logical function operations are summarized in the following table:

GR3		Logical Function Operation
[4]	[3]	
0	0	None: The data in the latches are ignored.
0	1	Data in latches is logically AND'ed with data from CPU or Set/Reset Logi c
1	0	Data in latches is logically OR'ed with data from CPU or Set/Reset Logi c
1	1	Data in latches is logically XOR'ed with data from CPU or Set/Reset Logi c

2:0 — **Data Rotate Count [2:0] :**
This field allows data from the CPU bus to be rotated up to seven bit positions prior to being altered by the Set/Reset logic.

10.6 GR4: Read Map Plane Select Registe r

I/O Port Address: 3CF

Index: 4

Bit	Description	Reset Stat e
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	Reserved	
1	Display Memory Data Plane Select [1]	0
0	Display Memory Data Plane Select [0]	0

This register is used to select a display memory data plane for Read mode 0. (For an overview of the Write modes, refer to the description in GR5.)

Bit — **Descriptio n**

7:2 — **Reserve d**

1:0 — **Display Memory Data P lane Select [1:0] :**

- This field is used only when Read mode 0 is selected (Graphics Controller register GR5[3] is 1).
- This field also specifies the display memory data plane selected for a read by Read mode 0, as shown in the following table:

GR4		Display Memory Data Plane Selecte d for Read by Read Mode 0
[1]	[0]	
0	0	Display Memory Data Plane 0
0	1	Display Memory Data Plane 1
1	0	Display Memory Data Plane 2
1	1	Display Memory Data Plane 3

10.7 GR5: Mode Registe r

I/O Port Address: 3CF

Index: 5

Bit	Description	Reset Stat e
7	Reserved	
6	256-Color Mode	0
5	Graphics Data Shift Register Mode	0
4	Odd/Even Addressing Mode	0
3	Read Mode	0
2	Write Mode [2]	0
1	Write Mode [1]	0
0	Write Mode [0]	0

This register specifies the Write mode and Read mode. In addition, it controls the configuration of the graphics data shift registers.

Bit	Descriptio n
7	**Reserve d**
6	**256-Color Mod e:** When this bit is: • 1, graphics data shift registers are configured for 256-color graphics modes, and Graphics Controller register GR5[5] is ignored. • 0, graphics data shift registers are configured for 16-, 4-, or 2-color graphics modes.
5	**Graphics Data Shift Register Mod e:** When this bit is: • 0, graphics data shift registers are configured for EGA compatibility. • 1, graphics data shift registers are configured for CGA compatibility, which is used for graphics modes 4h and 5h.
4	**Odd/Eve n Addressing Mode :** • When this bit is 1, the CL-GD7541/GD7543 is configured for odd/even addressing mode. • This bit must always be programmed to the opposite value as Sequencer register SR4[2].

10.7 GR5: Mode Register *(cont.)*

Bit **Description**

3 **Read Mode:**
This bit specifies whether the CL-GD7541/GD7543 is in Read mode 0 or Read mode 1.

GR5[3]	Read Mode	CPU Read Source
0	Read mode 0	CPU reads data directly from display memory
1	Read mode 1	CPU reads data that results from the color-compare logic of GR2

Read Mode 0 :

- During Read mode 0, the CPU reads data directly from display memory.
- Read mode 0 returns an adjacent 8 bits of the display memory data plane specified in GR4[1:0].
- Read mode 0 does not use the color-compare logic of register Graphics Controller register GR2.
- A Read mode 0 operation can be forced with an I/O read of CRT Controller register CR22, the Graphics Controller Data Latches Readback register.

Read Mode 1 :

- During Read mode 1, the CPU reads data that results from the color-compare logic of Graphics Controller register GR2.
- Read mode 1 allows eight adjacent pixels (16-color modes) to be compared to a specified color value in a single operation. Each of the 8 bits returned to the CPU indicates the result of a comparison between the 4 bits of the Color Compare (Graphics Controller register GR2[3:0]) and the bits from the four display memory planes.
- When the 4 bits of the Color Compare operation match the 4 bits from the display memory data planes, a 1 is returned for the corresponding bit position.
- When any bits in the Color Don't Care Plane (Graphics Controller register GR7[3:0]) are zeroes, the value in the corresponding display memory data plane is forced to match the values of the other data planes, becoming a "don't care" in the process.

10.7 GR5: Mode Registe r *(cont.)*

Bit **Descriptio n**

2:0 **Write Mode [2:0] :**

These bits specify if the CL-GD7541/GD7543 is in Write or Extended Write mode.

- When Extension register GRB[2] is 0, GR5[2] is forced to 0.

GR5			Write Mode Selecte d	
[2]	[1]	[0]		
0	0	0	When GRB[2] is 0, GR5[2] is forced to 0.	Write mode 0
0	0	1		Write mode 1
0	1	0		Write mode 2
0	1	1		Write mode 3
1	0	0	Extended Write mode 4	
1	0	1	Extended Write mode 5	
1	1	0	Reserved	
1	1	1	Reserved	

Write Mode 0 :

- Each of the four display memory data planes is written with the CPU data rotated by the number of counts in Graphics Controller register GR3[2:0].
- When a bit in Graphics Controller register GR1[3:0] is 1:
  - — The corresponding display memory data plane is written with the contents of the corresponding bit in GR0[3:0].
  - — Under the control of GR3[4:3], the contents of CPU data latches may be logically combined with data from the set/reset logic.
- Bit planes are enabled with Sequencer register SR2[3:0].
- Bit positions are enabled with Graphics Controller register GR8.

Write Mode 1:

- Each of the four display memory data planes is written with data in CPU data latches, loaded from display memory by a previous read.
- Write mode 1 ignores Graphics Controller register GR8.

Write Mode 2:

- Display memory data planes [3:0] are written with CPU data bit values [3:0].
- Bit planes are enabled with Sequencer register SR2[3:0].
- Bit positions are enabled with Graphics Controller register GR8.
- Write mode 2 ignores the data rotator, set/reset, and function-select fields.

Write Mode 3 :

- Display memory plane data comes from corresponding bits of GR0[3:0].
- The bit-position-enable field is formed with the logical AND of Graphics Controller register GR8 and the rotated CPU data.
- Write mode 3 ignores the set/reset and function-select fields.

10.7 GR5: Mode Registe r *(cont.)*

Bit	Descriptio n
2:0(cont.)	**Extended Write Mode 4 :** • The contents of Graphics Controller register GR1[7:0] are written into up to eight adjacent pixels. • The CPU data bits are used to control whether a pixel is written. — When a CPU data bit is a 1, the corresponding pixel is written. — When a CPU data bit is a 0, the corresponding pixel is not changed. • This mode can be used for 256-color text expansion for which the background is to be preserved. • This mode can also be used for 64K-color text expansion for which the background is to be preserved. **Extended Write Mode 5:** • The contents of either Graphics Controller register GR1[7:0] or GR0[7:0] are written into each of eight adjacent pixels. • For each of the eight pixels, the choice between GR1 and GR0 is made according to the value of the corresponding bit of the CPU data, summarized in the following table.

CPU Data	GR0 / GR1	Note
0	GR0	Background
1	GR1	Foreground

• This mode is intended for 256-color text expansion, for which both the foreground and background are to be written.
• This mode can also be used for 64K-color text expansion for which both the foreground and background are to be written.

10.8 GR6: Miscellaneous Registe r

I/O Port Address: 3CF

Index: 6

Bit	Description	Reset Stat e
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Display Memory Map [1]	0
2	Display Memory Map [0]	0
1	Chain Odd Maps to Even	0
0	Graphics Mode	0

This register contains miscellaneous control bits.

Bit — **Descriptio n**

7:4 — **Reserve d**

3:2 — **Display Memory Map [1:0] :**
This field specifies the beginning address and size of the display memory in the CPU host address space. This field is summarized in the following table:

GR6 [3]	GR6 [2]	Display Memory Map Plane	Display Memor y Address in CPU Host Address Spac e	Display Memory Size (Kbytes)	Affected Mode(s)
0	0	0	A000:0 to BFFF:F	128	Extended
0	1	1	A000:0 to AFFF:F	64	EGA / VGA
1	0	2	B000:0 to BFFF:F	32	Hercules
1	1	3	B800:0 to BFFF:F	32	CGA

1 — **Chain Odd Maps to Eve n:**
- When this bit is 1, CPU Address Bit[0] is replaced with a higher-order address bit. This replacement causes the even host addresses to access Planes 0 and 2, and the odd host addresses to access Planes 1 and 3.
- This mode is useful for MDA emulation.

0 — **Graphics Mode Enabl e:**
When this bit is:
- 0, the CL-GD7541/GD7543 functions in text (alphanumeric) modes.
- 1, the CL-GD7541/GD7543 functions in graphics (all-points-addressable) modes.

10.9 GR7: Color Don't-Care Plane Registe r

I/O Port Address: 3CF

Index: 7

Bit	Description	Reset Stat e
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Color Don't-Care Plane [3]	0
2	Color Don't-Care Plane [2]	0
1	Color Don't-Care Plane [1]	0
0	Color Don't-Care Plane [0]	0

This register is used with Graphics Controller register GR2 for Read mode 1 accesses. (For an overview of the Read modes, refer to the description in Graphics Controller register GR5.)

Bit	Descriptio n
7:4	**Reserve d**
3:0	**Color Don' t-Care Plane [3:0] :** These 4 bits are used to control color compare logic for the four Color Don't-Care Planes. If a bit is: • 1, the corresponding plane is involved in color compares. • 0, the corresponding plane is not involved in color compares.

10.10 GR8: Display Memory Bit Mask Registe r

I/O Port Address: 3CF

Index: 8

Bit	Description	Reset Stat e
7	Display Memory Bit Write Enable [7]	0
6	Display Memory Bit Write Enable [6]	0
5	Display Memory Bit Write Enable [5]	0
4	Display Memory Bit Write Enable [4]	0
3	Display Memory Bit Write Enable [3]	0
2	Display Memory Bit Write Enable [2]	0
1	Display Memory Bit Write Enable [1]	0
0	Display Memory Bit Write Enable [0]	0

This register is used to control writing to display memory on a bit basis in Write modes 0, 2, and 3

Bit	Descriptio n
7:0	**Display Memory Bit Write Enable [7:0] :** Each bit in this register controls whether the corresponding bit in display memory is written in Write modes 0, 2, or 3. When a bit is: • 1, the corresponding bit in display memory is written. • 0, the corresponding bit in display memory is not written.

11. ATTRIBUTE CONTROLLER REGISTERS

11.1 ARX: Attribute Controller Index Register

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: (n/a)

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	AR11 Video Source Enable	0
4	Attribute Controller Index [4]	0
3	Attribute Controller Index [3]	0
2	Attribute Controller Index [2]	0
1	Attribute Controller Index [1]	0
0	Attribute Controller Index [0]	0

This register is used to specify the register in the Attribute Controller block that is accessed with the next I/O write to 3C0 or I/O read to 3C1.

For the Attribute Controller block, both the index and data registers are at the same port addresses, unlike other blocks, for which index and data registers are at different port addresses.

Alternate writes to ARX toggle between index and data. The CRT Controller register CR24 provides access to the Attribute Controller Toggle, which reads or writes either a data value or an index value.

Bit	Description
7:6	**Reserved**
5	**AR11 Video Source Enable:** When this bit is: • 0, the screen displays the color in Attribute Controller register AR11. • 1, the screen displays normal video.
4:0	**Attribute Controller Index [4:0]:** This field is the index to the Attribute Controller data registers. When CRT Contrdler register CR24[7] is 0, the CRT Controller register bits CR26[4:0] read back the bits in ARX[4:0].

11.2 AR0 to ARF: Attribute Controller Palette Register s

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: 0:F

Bit	Description	Reset Stat e
7	Reserved	
6	Reserved	
5	Secondary Red	0
4	Secondary Green / Intensity	0
3	Secondary Blue / Monochrome	0
2	Red	0
1	Green	0
0	Blue	0

These bits act as pointers to palette entries.

Bit	Descriptio n
7:6	**Reserve d**
5:0	**Palette Entrie s:** In 16-color text and graphics modes, the digital attribute controller palette entries in this register are chosen by the 4 bits of pixel data, and they point to palette memory entries. • The palette memory entries are normally programmed, and so the DAC outputs reflect these values. • As a result, palette memory is programmed to simulate standard EGA colors.

11.3 AR10: Attribute Controller Mode Registe r

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: 10

Bit	Description	Reset Stat e
7	AR14 Video Source Enable	0
6	Pixel Double-Clock Select	0
5	Pixel Panning Compatibility	0
4	Reserved	
3	Character Blink Enable	0
2	Line Graphics Enable	0
1	Display Type	0
0	Graphics Mode	0

This register contains some miscellaneous control bits for the Attribute Controller.

Bit	Descriptio n
7	**AR14 Video Source Enable :** • When an 8-, 16-, or 24-bit pixel mode is chosen, this bit is ignored. • When this bit is: — 1, Attribute Controller register bits AR14[1:0] are the source for CLUT address bits [5:4], which allows rapid selection of four 16-color palettes. — 0, Attribute Controller registers AR0 to ARF[5:4] are the source for CLUT address bits [5:4].
6	**Pixel Doubl e-Clock Select :** When this bit is: • 0, pixels are clocked on every cycle. • 1, pixels are clocked on every other clock cyde. Also: — Registers AR0 to ARF are bypassed. — This bit setting is used with graphics mode 13h. — The CL-GD7541/GD7543 sequencer logic operates at twice the pixel clock rate.
5	**Pixel Panning Compatibility :** When this bit is: • 0, the two parts of a split screen pan together. • 1, a line compare match in the CRTC forces the output of the AR13 Pixel Panning register to a 0 until the next VSYNC occurs. This action allows the panning of Screen A without Screen B.
4	**Reserve d**
3	**Character Blink Enabl e:** When this bit is: • 0, character blinking is disabled • 1, character blinking is enabled at the frequency rate of vertical refresh, divided by 32.

11.3 AR10: Attribute Controller Mode Register *(cont.)*

Bit — **Description**

2 — **Line Graphics Enable :**
When this bit is:
- 0, bit 9 of a 9-bit-wide character cell is the same as the background.
- 1, bit 9 of a 9-bit-wide character cell is made the same value as bit 8. This value is used for those character sets that have special characters associated with line graphics, for characters codes in the range C0 through DF.

1 — **Display Type :**
This bit is used only if the CL-GD7541/GD7543 is in alphanumeric modes. When this bit is:
- 0, the Attribute Byte contents are treated as color attributes.
- 1, the Attribute Byte contents are treated as MDA-compatible attributes.

The following table shows examples of monochrome attributes.

Bit Definitions for Attribute Byte								Hex Code of Attribute Byte	Monochrome Attribute Byte
Blink Bit	Background Bits			Intensity Bit	Foreground Bits				
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]		
0	0	0	0	0	1	1	1	07h	Normal
0	0	0	0	1	1	1	1	0Fh	Intense
0	0	0	0	0	0	0	1	01h	Underline
0	0	0	0	1	0	0	1	09h	Underline Intense
0	1	1	1	0	0	0	0	70h	Reverse
1	1	1	1	0	0	0	0	F0h	Blinking Reverse

0 — **Graphics Mode Enable:**
When this bit is:
- 0, the Attribute Controller functions in text (alphanumeric) modes.
- 1, the Attribute Controller functions in graphics (all-points-addressable) modes.

11.4 AR11: Overscan (Border) Color Registe r

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: 11

Bit	Description	Reset Stat e
7	Reserved	
6	Reserved	
5	(Border Color Bit) Secondary Red	0
4	(Border Color Bit) Secondary Green	0
3	(Border Color Bit) Secondary Blue	0
2	(Border Color Bit) Red	0
1	(Border Color Bit) Green	0
0	(Border Color Bit) Blue	0

This register points to the entry in the CLUT that defines the border color.

- As shown in Figure 9-1 at the description of CRT Controller register CR0 in Chapter 9, the border is defined as that portion of the raster between blanking and active video, on all four sides of the screen.
- Typically, the CLUT entries are programmed, and so the color defined by the bits above is the color that results.

Bit	Descriptio n
7:6	**Reserve d**
5:0	**Border Color Bits [5:0] :** Depending on if the CGA or EGA mode is in use, either four of these bits (for CGA) or six of these bits (for EGA) are used to select the CLUT entry for the border color in CGA and EGA modes.

11.5 AR12: Color Plane Enable Registe r

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: 12

Bit	Description	Reset Stat e
7	Reserved	
6	Reserved	
5	Video Status Multiplexor [1]	0
4	Video Status Multiplexor [0]	0
3	Color Plane Enable [3]	0
2	Color Plane Enable [2]	0
1	Color Plane Enable [1]	0
0	Color Plane Enable [0]	0

This register contains:

- One field that chooses the inputs for diagnostic bits in STAT[5:4].
- Another field that enables the 4 color planes in the Attribute Controller Palette registers

Bit **Descriptio n**

7:6 **Reserve d**

5:4 **Video Status Multiplexor [1:0]:**
This field chooses the inputs for the diagnostic status bits in STAT[5:4] as indicated in the following table:

AR12		STAT	
[5]	[4]	[5]	[4]
0	0	FP[2] Red	FP[0] Blue
0	1	FP[3] Secondary Blu e	FP[1] Green
1	0	FP[5] Secondary Red	FP[4] Secondary Green
1	1	FP[7]	FP[6]

11.5 AR12: Color Plane Enable Register *(cont.)*

Bit **Descriptio n**

3:0 **Color Plane Enable [3:0]:**
This field controls which display memory data plane sends data to a corresponding attribute controller color palette register, as shown in the following table:

AR12 Bit / State	Display Memor y Data Plan e	Result
AR12[3] is 0	Plane 3	Plane 3 disabled .
AR12[3] is 1		Plane 3 data selected for Color Palette register 3 .
AR12[2] is 0	Plane 2	Plane 2 disabled .
AR12[2] is 1		Plane 2 data selected for Color Palette register 2 .
AR12[1] is 0	Plane 1	Plane 1 disabled .
AR12[1] is 1		Plane 1 data selected for Color Palette register 1 .
AR12[0] is 0	Plane 0	Plane 0 disabled .
AR12[0] is 1		Plane 0 data selected for Color Palette register 0 .

11.6 AR13: Pixel Panning Registe r

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: 13

Bit	Description	Reset Stat e
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Pixel Panning [3]	0
2	Pixel Panning [2]	0
1	Pixel Panning [1]	0
0	Pixel Panning [0]	0

This register:

- Specifies the number of pixels the display data are shifted to the left
- Functions both in the graphics (all-points-addressable) and text (alphanumeric) modes.

Bit **Descriptio n**

7:4 **Reserve d**

3:0 **Pixel Panning [3:0] :**
This field controls fine panning on a pixel-by-pixel basis by specifying the number of pixels the display data are shifted to the left. The values programmed into AR13[3:0] are interpreted as indicated in the following table:

AR13				Hex Code	Shift for 9-Bit Characters	Shift for 8-Bit Characters	Shift for Video Mode 13h
[3]	[2]	[1]	[0]				
0	0	0	0	0h	1 bit left	No shift	No shift
0	0	0	1	1h	2 bits left	1 bit left	–
0	0	1	0	2h	3 bits left	2 bits left	1 bit left
0	0	1	1	3h	4 bits left	3 bits left	–
0	1	0	0	4h	5 bits left	4 bits left	2 bits left
0	1	0	1	5h	6 bits left	5 bits left	–
0	1	1	0	6h	7 bits left	6 bits left	3 bits left
0	1	1	1	7h	8 bits left	7 bits left	–
1000 to 1111				8h - Fh	No shift	1 bit right	–

11.7 AR14: Color Select Registe r

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: 14

Bit	Description	Reset Stat e
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Color Bit C [7]	0
2	Color Bit C [6]	0
1	Color Bit C [5]	0
0	Color Bit C [4]	0

This register contains two fields that are involved in the selection of addresses into the CLUT.

Bit	Descriptio n
7:4	**Reserve d**
3:2	**Color Bits C [7:6] :** • In 8-, 16-, and 24-bit pixel modes, these bits are ignored. • These 2 bits are concatenated with the 6 bits from the Attribute Controller Palette registers AR0 to ARF to form the address into the CLUT and to drive flat-panel interface pins FP[7:6].
1:0	**Color Bits C [5:4]:** • In 8-, 16-, and 24-bit pixel modes, these bits are ignored. • When AR10[7] is: — 0, these 2 bits are ignored. — 1, these 2 bits replace the corresponding 2 bits from the Attribute Controller Palette registers AR0 to ARF to form the address into the CLUT and to drive flat-panel interface pins FP[5:4].

12. EXTENSION REGISTER S

12.1 SR6: Unlock All Extension Register s

I/O Port Address: 3C5

Index: 6

Bit	Description	Reset Stat e
7	Not Used	Not applicable
6	Not Used	Not applicable
5	Not Used	Not applicable
4	Unlock All Extension Registers	1
3	Not Used	Not applicable
2	Unlock All Extension Registers	0
1	Unlock All Extension Registers	1
0	Unlock All Extension Registers	0

Bit	Descriptio n
7:5, 3	**Not Use d**
4, 2:0	**Unlock All Extension Registers (Access Value) :** All Extension registers are: • Unlocked (enabled) for read/write access when bits 4, 2:0 equal the following: — Bit 4 = 1 — Bit 2 = 0 — Bit 1 = 1 — Bit 0 = 0 • Locked (disabled) for read/write access when bits 4, 2:0 are any other value other than the ones shown above.

12.2 SR7: Extended Sequencer Mode Register

I/O Port Address: 3C5

Index: 7

Bit	Description	Reset Stat e
7	Display Memory Segment Select [3]	0
6	Display Memory Segment Select [2]	0
5	Display Memory Segment Select [1]	0
4	Display Memory Segment Select [0]	0
3	Reserved	
2	CRT Controller Character Clock Divider [1] Select	0
1	CRT Controller Character Clock Divider [0] Select	0
0	High-Resolution Packed-Pixel Mode Select	0

This register has several purposes which are described in the following bit descriptions

Bit	Descriptio n
7:4	**Display Memory Segment Select [3:0]:** When the value of this 4-bit field is programmed to: • 0000: — The CL-GD7541/GD7543 is configured for standard VGA display memory addressing, responding to memory accesses at Axxx:x, or Bxxx:x, or both, as specified by GR6[3:2]. • Other than 0000: — The CL-GD7541/GD7543 is configured for 1-Mbyte linear memory addressing. — The CL-GD7541/GD7543 responds to any memory access where CPU address bits A[23:20] match this field value. • Other than 0000 *and*: — When there is a full 1 Mbyte of display memory installed, *and* the CL-GD7541/GD7543 is configured for extended 256-color chain-4, then the 1-Mbyte address range has one-to-one mapping to the 1 Mbyte of installed display memory. — When the CL-GD7541/GD7543 is configured for unchained, ×8, or ×16 addressing, then it responds to the entire 1-Mbyte range, but address wrapping takes place. — GRB[5] is programmed to a 1, then SR7[4] becomes a don't-care bit, and the CL-GD7541/GD7543 responds to a 2-Mbyte address.
3	**Reserve d**

12.2 SR7: Extended Sequencer Mode Register *(cont.)*

Bit **Description**

2:1 **CRT Controller Character Clock Divider [1:0] Select:**
This field selects how the CRTC Character Clock is divided down, resulting in various pixel data rates, as indicated in the following table:

SR7		Resulting Pixel Data
[2]	[1]	
0	0	8 bit/pixel data with 1× VCLK (CRTC Character Clock is not divided down.) (Normal operation.)
0	1	16 bit/pixel data with 2× VCLK (CRTC Character Clock ÷ 2)
1	0	24 bit/pixel data with 3× VCLK (CRTC Character Clock ÷ 3)
1	1	16 bit/pixel data with 1× VCLK (CRTC Character Clock is not divided down.)

16-Bit/Pixel Data with 2× VCLK (SR7[2:1] is 01)
When this mode is selected:
- The DAC and the Video Shift register are clocked at the VCLK data byte rate.
- The CRTC is clocked with a character clock of 8 pixels (16 VCLKs).

The above clocking allows:
- The CRTC timing value for 640 × 480 modes and 800 × 600 modes with 16-bit pixels to be programmed in units of an 8-pixel character clock.
- CRT Controller register CR13 to be set to:
  — A0h for 640 × 480 mode
  — C8h for 800 × 600 mode
- The hardware cursor horizontal position to be set in pixel units.
- The Cursor Data Invert function to operate on 15-, 16-, or 18-bit RGB data presented to the DAC.

24-Bit/Pixel Data with 3× VCLK (SR7[2:1] is 10)
When this mode is selected:
- The DAC and the Video Shift register is clocked at the VCLK data byte rate.
- The CRTC is clocked with a character clock of 8 pixels (24 VCLKs).

The above clocking allows:
- The CRTC timing value for 640 × 480 modes with 24-bit pixels to be programmed in units of an 8-pixel character clock.
- CRT Controller register CR13 to be set to F0h.

The hardware cursor is not supported in this configuration.

12.2 SR7: Extended Sequencer Mode Register *(cont.)*

Bit	Description
2:1 *(cont.)*	**Select CRTC Character Clock Divider [1:0]** *(cont.)*: **16-Bit/Pixel Data with 1× VCLK (SR7[2:1] is 11)** When this mode is selected: • The sequencer provides 16-bit data to the palette DAC at the displayed pixel rate. This action allows 5-5-5 or 5-6-5 color modes to be selected with a 1× VCLK. • The data output on FCP[7:0] is only the low-byte of the pixel data. (In this case, the high-byte of the pixel data is not available externally.) • This mode also provides for 1024 × 768 display modes, with 5-5-5 or 5-6-5 color, and with VCLK equal to the pixel rate.
0	**High-Resolution Packed-Pixel Mode Select :** When this bit is 1: • Video Shift registers are configured so one character clock equals 8 pixels. • True packed-pixel memory addressing is enabled. • This mode may also be used with 16- and 24-bit pixel modes. (Refer to SR7[2:1].) • This mode may not be used with Graphics mode 13h, which is packed pixel, but not high resolution. (For a high-resolution Graphics mode 13h, set Attribute Controller register AR10[6] to 1.) **NOTE:** In true packed-pixel addressing, consecutive pixels are stored at consecutive addresses. In contrast, with chain-4 addressing, consecutive pixels are stored at every fourth address in display memory .

12.3 SR8: Miscellaneous Control Register 1

I/O Port Address: 3C5

Index: 8

Bit	Description	Access	Reset Stat e
7(MSB)	Not Used	-	Not applicable
6	Reserved	-	
5	FCESYNC# and FCEVIDEO# Latch	R/W	0
4	Reserved	-	
3	Reserved	-	
2	Reserved	-	
1	Reserved	-	
0(LSB)	Reserved	-	

Bit	Descriptio n
7	**Not Used**
6	**Reserve d**
5	**FCESYNC# and FCEVIDEO# Latc h:** When this bit is 1, the values on the FCESYNC# and FCEVIDEO# inputs are latched, so that the pins can be used for other functions.
4:0	**Reserve d**

12.4 SR9, SRA: Scratchpad 0 and 1 Registers

I/O Port Address: 3C5

Index: 9, A

Bit	Description	Reset Stat e
7	R/W Data [7]	0
6	R/W Data [6]	0
5	R/W Data [5]	0
4	R/W Data [4]	0
3	R/W Data [3]	0
2	R/W Data [2]	0
1	R/W Data [1]	0
0	R/W Data [0]	0

These two registers are reserved for the exclusive use of theCL-GD7541/GD7543 BIOS and must never be written by any application program. They are listed here only for completeness

Bit	Descriptio n
7:0	**Reserved:** These bits are reserved for the Cirrus Logic BIOS.

12.5 SRB, SRC, SRD, SRE: VCLK0,1,2,3 Numerator Registers

I/O Port Address: 3C5

Index: B, C, D, E

Bit	Description	Access	Reset Stat e
7	Reserved		
6	VCLK Numerator [6]	R/W	See table below
5	VCLK Numerator [5]	R/W	See table below
4	VCLK Numerator [4]	R/W	See table below
3	VCLK Numerator [3]	R/W	See table below
2	VCLK Numerator [2]	R/W	See table below
1	VCLK Numerator [1]	R/W	See table below
0	VCLK Numerator [0]	R/W	See table below

These registers are used in conjunction with Extension registers SR1B to SR1E to establish the frequency of the four possible video clocks. The video clock used is selected by MISC[3:2].

This register establishes the numerator value. For information on denominator and post-scalar values, refer to Section 12.16. For more information on clock options, refer to Appendix G.

Each video clock frequency is determined by the following equation.

$$VCLKn\ (\text{MHz}) = \frac{OSC \times NR}{DR \times [P+1]}$$

Equation 1 2-1

where:

VCLK n	=	Video clock frequency n, where n = 0, 1, 2, 3
OSC	=	Input clock frequency of 14.318 MH z
Numerator **R**egister	=	Value of register bits SRi [6:0], where i = B, C, D, E
Denominator **R**egister	=	Value of register bits SR1i [5:1], where i = B, C, D, E
Post-scalar	=	Value of register bits SR1i [0], where i = B, C, D, E

If n = 0, then i = B.
If n = 1, then i = C .
If n = 2, then i = D .
If n = 3, then i = E .

The following table shows the reset values of the registers that determine the video clock frequency. The table also shows the corresponding video clock frequency at system reset.

12.5 SRB, SRC, SRD, SRE: VCLK0,1,2,3 Numerator Register s *(cont.)*

VCLKn and Reset Frequency		VCLKn Numerator Value s			VCLKn Denominator Values			
VCLKn	VCLKn Frequency at Reset	Numerator Register and Hex Value in Register		*NR* = Value Used in Equation Numerator	Denominator Register and Hex Value in Register		*DR* = Value Used in Equation Denominator, Resulting from Post-scalar	*P* = Post-scalar Value Used in Equation Denominator
	MHz	Register (SRi)	Hex	Decimal Equivalent of Hex Value	Register (SRi)	Hex	Decimal	Decimal
VCLK0	25.180	SRB	66h	102	SR1B	3Bh	29	1
VCLK1	28.325	SRC	5Bh	91	SR1C	2Fh	23	1
VCLK2	41.165	SRD	45h	69	SR1D	30h	24	0
VCLK3	36.082	SRE	7Eh	126	SR1E	33h	25	1

Bit	Description
7	**Reserved**
6:0	**VCLK Numerator [6:0]:** These bits determine the numerator value (*N*) used to select the video clock frequency.

12.6 SRF: Display Memory Control Register

I/O Port Address: 3C5

Index: F

Bit	Description	Reset Stat e
7	Display Memory Bank Select	0
6	CPU-Write FIFO Fast-Page-Detection Mode Disable	0
5	CRT FIFO Depth Control	0
4	Display Memory Data Bus Width [1]	0
3	Display Memory Data Bus Width [0]	0
2	Display Memory RAS Timing	0
1	Reserved	
0	Display Memory Multiple-CAS# / Multiple-WE# Select	1

This register is used to control the display memory.

Bit **Descriptio n**

7 **Display Memory Bank Select :**

- This bit is used with SRF[4:3] to specify the display memory data bus width according to the number of banks of display memory used.
- When this bit is:
  - — 1, the CL-GD7541/GD7543 is configured for two banks of display memory (four 256K × 16 DRAMs).
  - — 0, the CL-GD7541/GD7543 is configured for one bank of display memory (four 512K × 8 DRAMs, or two 256K × 16 DRAMs).

6 **CPU Write FIFO Fast-Page-Detection Mode Disable :**

- To avoid CPU write buffer under-runs, this bit *must* be programmed to 1, either when loading font data for page-mode font access, or when performing multiple color-expand writes in 16-bit pixel modes.
- When this bit is:
  - — 1, CPU writes to display memory take place as random cycles.
  - — 0, consecutive CPU writes to display memory are executed as fast-page mode writes, whenever possible.

5 **CRT FIFO Depth Contro l:**

- When this bit is 0 (the default):
  - — The CRT write buffer depth is set to 8 levels (32 bits/level).
  - — This setting is typically used for standard graphics modes and for extended 16-color modes.
- When this bit is 1:
  - — The CRT write buffer depth is set to 16 levels (64 bytes).
  - — *And* an all-points-addressable graphics mode is being used, Extension register SR20[2] is enabled.
  - — This setting is typically used for any 16-bit or 24-bit pixel modes and for extended 8-bit pixel modes.
  - — This setting must never be used for any text mode.

12.6 SRF: Display Memory Control Register *(cont.)*

Bit — **Description**

4:3 **Display Memory Data Bus Width [1:0]:**
This 2-bit field is used with SRF[7] to specify the display memory data bus width according to the following table:

SRF			Display Memory Data Bus Width	Memory Organization	Total Memory
[7]	[4]	[3]			
0	0	0	–	Reserved	Reserved
0	0	1	–	Reserved	Reserved
0	1	0	32-bit	Two 256K × 16 DRAMs	1 Mbyte
				Four 512K × 8 (symmetric) DRAMs	2 Mbytes
0	1	1	–	Reserved	Reserved
1	1	0	32-bit	Four 256K × 16 DRAMs (two banks)	2 Mbytes
1	1	1	–	Reserved	Reserved

These bits have one level of buffering. At the end of each horizontal scanline refresh interval, when horizontal blanking begins, the state of each of these bits is transferred to the timing logic. This transfer avoids changing the timing logic in mid-scanline.

2 **Display Memory RAS Timing:**
This bit indicates the display memory row-address strobe timing as summarized in the following table.

SRF[2]	Timing for RAS High	Timing for RAS Low	Note
0	3 MCLK	4 MCLK	Extended RAS (default)
1	2.5 MCLK	3.5 MCLK	Standard RAS

The default is extended RAS timing, which fits all DRAMs. However, to achieve optimal performance, the timing selected must match the MCLK.

1 **Reserved**

0 **Display Memory Multiple-CAS# / Multiple-WE# Select:**
- A 0 selects multiple-WE# display memory support
- A 1 selects multiple-CAS# display memory support, which is the default

12.7 SR10: Hardware Cursor and Hardware Icon Coarse Horizontal Position

I/O Port Address: 3C5

Index: 10, 30, 50, 70, 90, B0, D0, F0

Bit	Description	Reset Stat e
7	HW Cursor and HW Icon Coarse Horizontal Position [10]	0
6	HW Cursor and HW Icon Coarse Horizontal Position [9]	0
5	HW Cursor and HW Icon Coarse Horizontal Position [8]	0
4	HW Cursor and HW Icon Coarse Horizontal Position [7]	0
3	HW Cursor and HW Icon Coarse Horizontal Position [6]	0
2	HW Cursor and HW Icon Coarse Horizontal Position [5]	0
1	HW Cursor and HW Icon Coarse Horizontal Position [4]	0
0	HW Cursor and HW Icon Coarse Horizontal Position [3]	0

This register, and bits SRX[7:5] of the index that is used to access it, is used to define in character clocks the coarse horizontal (X) pixel offset of the graphics hardware cursor and icon. For more information on the hardware cursor and icon, refer to Appendix B and Appendix C.

For all 8-bit text modes and non-expanded graphics modes and text modes which do not require the fourth expansion bit, the entire 12-bit cursor or icon horizontal position can be written in a sh-gle 16-bit I/O write as follows:

- Extension register bits SR2A[6] and SR2E[0], which are cleared to 0, are ignored.
- The offset must be placed in AX[15:5].
- AX[4:0] must be 10000.
- DX must be 3C4h.

When 10, 30, 50...F0 is written to 3C4 without writing to 3C5 (a byte write), then a read of 3C4 returns the previously stored three bits of the cursor or icon position.

NOTE: Changes programmed in register SR10 do not take effect until register SR11 has been written .

Bit	Descriptio n
7:0	**Hardware Cursor and Hardware Icon Coarse Horizontal Position [10:3] :** Extension register SR12[3] selects whether the value in this register refers to the hardware cursor or the hardware icon. Cursor 12-bit horizontal position • When Extension register SR12[3] is 0, the hardware cursor is selected. • The most-significant 8 coarse horizontal position bits are in Extension register SR10[7:0]. • The least-significant 3 fine horizontal position bits, defined in dot clocks, are in Extension register SRX[7:5]. • Extension register SR2E[0] extends the cursor fine horizontal position by one most-significant bit for horizontally expanded graphics modes. This extra bit is valid only with a 10-dot character clock. • For text modes and Graphics mode 13h, the hardware cursor is not available.

12.7 SR10: Hardware Cursor and Hardware Icon Coarse Horizontal Position *(cont.)*

Bit	Description
7:0*(cont.)*	**HW Cursor and HW Icon Coarse Horizontal Position [10:3]** *(cont.)*:

Icon 12-bit Horizontal Position

- When Extension register SR12[3] is 1, the hardware icon is selected.
- SR10[7:0] form the upper-eight bits of the 11-bit icon horizontal offset.
- SRX[7:5] form the lower-three bits of the 11-bit icon horizontal offset.
- SR2A[6] is the fourth bit of a dot-clock-level delay in expanded-graphics modes and in text modes with 9-dot or 10-dot fonts.
- The icon is supported in all modes, except interlaced, 24 bpp with 3× clock, and 16 bpp with 2× clock. (The latter does not support horizontal doubling.)

To program the horizontal position of the hardware icon,

- Place the icon hot point (top left) at pixel n (with 0 as the first pixel).
- Program the coarse horizontal position as: Integer [(n + (k – 1)) ÷ k] (k = the number of dots in a character clock.)
- Program the fine horizontal position as: Remainder [(n + (k – 1)) ÷ k]

For example, to place the icon

- At pixel 10, which is 11 pixels from the left (n = 10),
- With an 8-dot character clock, as in graphics mode 12 (k = 8),

Then program

- The coarse position = Integer [(10 + (8 – 1)) ÷ 8] = 2h
- The fine position = Remainder [(10 + (8 – 1)) ÷ 8] = 1h

An example of programming for an 8-dot character clock is in the table below.

Pixel Position	Horizontal Position Programmed	
	Coarse	Fine
0	0	7
1	1	0
2	1	1
3	1	2
4	1	3
5	1	4
6	1	5
7	1	6
8	1	7
9	2	0
10	2	1

There are only three cases of character clock width.

- 10 dots — used for text and graphics expansion on 800 × 600 LCD
- 9 dots — used for text on 800 × 600 LCDs, when 720 dots are displayed
- 8 dots — used in all other cases

12.8 SR11: Hardware Cursor and Hardware Icon Coarse Vertical Position

I/O Port Address: 3C5

Index: 11, 31, 51, 71, 91, B1, D1, F1

Bit	Description	Reset Stat e
7	HW Cursor and HW Icon Coarse Vertical Position [10]	0
6	HW Cursor and HW Icon Coarse Vertical Position [9]	0
5	HW Cursor and HW Icon Coarse Vertical Position [8]	0
4	HW Cursor and HW Icon Coarse Vertical Position [7]	0
3	HW Cursor and HW Icon Coarse Vertical Position [6]	0
2	HW Cursor and HW Icon Coarse Vertical Position [5]	0
1	HW Cursor and HW Icon Coarse Vertical Position [4]	0
0	HW Cursor and HW Icon Coarse Vertical Position [3]	0

This register, and bits SRX[7:5] of the index that is used to access it, is used to define in scanlines the coarse vertical (Y) scanline offset of the graphics hardware cursor and icon. For more information on the hardware cursor and icon, refer to Appendix B and Appendix C.

The entire 11-bit cursor or icon vertical position can be written in a single 16-bit I/O write as follows:

- The offset must be placed in AX[15:5].
- AX[4:0] must be 10001.
- DX must be 03C4.

When 10, 30, 50...F1 is written to 3C4 without writing to 3C5 (a byte write), then a read of 3C4 returns the previously stored three bits of the cursor or icon vertical position.

Bit	Descriptio n
7:0	**Hardware C ursor and Hardware Icon Coarse Vertical Position [10:3] :** Extension register SR12[3] selects whether the value in this register refers to the hardware cursor or the hardware icon. Cursor and icon 11-bit vertical position: • When SR12[3] is: — 0, the hardware cursor is selected. — 1, the hardware icon is selected. • SR11[7:0] are the upper 8 coarse vertical position bits. • SRX[7:5] are the lower 3 fine vertical position bits, defined in scanlines.

12.9 SR12: Video Data Path Control Register

I/O Port Address: 3C5

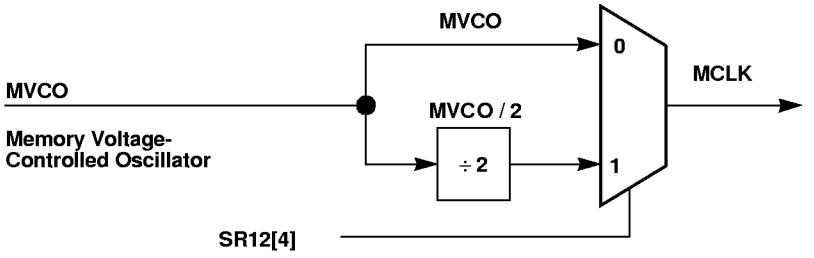
Index: 12

Bit	Description	Reset State
7	Overscan Color Protect	0
6	Tristate All Display Memory Pins	0
5	VCLK = (VCO ÷ 4)	0
4	MCLK = (MVCO ÷ 2)	0
3	Hardware Cursor and Hardware Icon Position Modification	0
2	Hardware Cursor-Size Select	0
1	CPU Access to DAC Extended Colors	0
0	Hardware Cursor Enable	0

This register is used to enable or disable the CL-GD7541/GD7543 4-bit packed-pixel addressing.

Bit	Description
7	**Overscan Color Protect:** When this bit is: • 1, the overscan color comes from Extension register HDR (the hidden DAC register, the 16-cell RAMDAC RAM extension). As a result, the border color is locked to a value dictated by environmental requirements, and it cannot be changed by the application. • 0, the overscan color comes from Attribute Controller register AR11[5:0].
6	**Tristate All Display Memory Pins:** When this bit is: • 0, all display memory pins operate normally. • 1, all display memory pins are forced to a tristate high-impedance off state. The display memory pins can then be multiplexed for use with another graphics controller.
5	**VCLK = (VCO , 4):** When this bit is 1, the video clock (VCLK) signal is derived from the voltage-controlled oscillator (VCO) frequency divided by four. • This bit must be used to get VCLK frequencies of 20 MHz or less. For example, to get 20 MHz: — Program VCO for 80 MHz. — Set SR12[5] to 1, which divides the VCO signal by four. — As a result, VCLK = 20 MHz. • This bit is useful in 5 V core-VDD systems where at low frequencies, the VCO frequency range is not good enough. (Note that bits SR1B[0], SR1C[0], SR1D[0], and SR1E[0] divide the VCO signal by 2 to produce the VCLK signal). While the VCO is within its operating range, as appropriate for the desired VCLK frequency, divide by 2 or by 4.

12.9 SR12: Video Data Path Control Registe r *(cont.)*

Bit	Descriptio n
4	**MCLK = (MCLK , 2):** • This bit is used to get MCLK (memory clock signal) frequencies outside the memory VCO frequency range for a given Core VDD value and frequency. • When this bit is: — 0, MCLK is the same as the MVCO (memory voltage-controlled oscillator) signal. — 1, MCLK is derived by dividing by two the original memory clock signal from MVCO. 
3	**Hardware Cursor and Hardware Icon Position Modification:** This bit selects whether the CPU can modify the position (both horizontal and vertical) of either the hardware cursor or the hardware icon. The same registers are used to modify both hardware cursor and hardware icon position. • When this bit is 0, the CPU can modify the hardware cursor position. • When this bit is 1, the CPU can modify the hardware icon position. • This bit does not affect Extension register bits SR2A[6] or SR2E[0], which are always accessible by the CPU.
2	**Hardware Cursor -Size Select :** This register bit must be programmed the same as SR21[4]. When this bit is: • 0, the 32 × 32-pixel hardware cursor is selected. • 1, the 64 × 64-pixel hardware cursor is selected.
1	**CPU Access to DAC Extended Colors:** When this bit is: • 0, the CPU accesses the standard VGA 256 × 18 CLUT. • 1, the CPU accesses the DAC extended colors, which are 16 additional 18-bit wide RAMDAC RAM locations. — Some locations have a specific purpose, such as hardware cursor colors (2 locations), hardware icon colors (4 locations), and border color (1 location). — Other locations are not used, or they can be used as scratchpad registers by the BIOS and drivers.

12.9 SR12: Video Data Path Control Register *(cont.)*

Bit — **Description**

1 *(cont.)* **CPU Access to DAC Extended Colors** *(cont.)*:
The address map for the DAC extended colors is given in the following table:

I/O Address	Physical RAM Location	Function
X0h	256	Hardware cursor background color
XFh	257	Hardware cursor foreground color
X2h	258	Fix color of overscan (the border)
X3h	259	Hardware icon color #0. (This function is not used, if in 3-colors-and-transparent mode.)
X4h	260	Hardware icon color #1
X5h	261	Hardware icon color #2
X6h	262	Hardware icon color #3
XB, XC, XD, XE	269, 270	Used by Video BIOS

0 **Hardware Cursor Enable:**
When this bit is 1, the graphics hardware cursor is enabled.

12.10 SR13: Hardware Cursor Pattern Address Offset Register

I/O Port Address: 3C5

Index: 13

Bit	Description	Reset Stat e
7	Not Used	Not applicable
6	Not Used	Not applicable
5	Reserved	
4	Hardware Cursor Pattern Select [4]	0
3	Hardware Cursor Pattern Select [3]	0
2	Hardware Cursor Pattern Select [2]	0
1	Hardware Cursor Pattern Select [1] / Reserved	0
0	Hardware Cursor Pattern Select [0] / Reserved	0

This register is used to select one of the following:

- One of the 32 possible cursor patterns for the 32 × 32 hardware cursor.
- One of the 8 possible cursor patterns for the 64 × 64 hardware cursor.

For a complete programming guide for the hardware cursor, refer to Appendix B.

Bit	Descriptio n
7:6	**Not Use d**
5	**Reserve d**
4:0	**Hardware C ursor Pattern Select (32 × 32 Cursor) :** When SR12[2] is 0: • This 5-bit field can select 1 of 32 cursor patterns for the 32 × 32 cursor. • The patterns are stored in 8 Kbytes of the top 32 Kbytes of display memory.
4:2	**Hardware C ursor Pattern Select (64 × 64 Cursor) :** When SR12[2] is 1: • This 3-bit field can select 1 of 8 cursor patterns for the 64 × 64 cursor. • The patterns are stored in 8 Kbytes of the top 32 Kbytes of display memory.
1:0	**Reserved :** This bit is reserved when SR12[2] is 1.

12.11 SR14, SR15: Scratchpad 2, 3 Registers

I/O Port Address: 3C5

Index:14, 15

Bit	Description	Reset Stat e
7	R/W Data [7]	0
6	R/W Data [6]	0
5	R/W Data [5]	0
4	R/W Data [4]	0
3	R/W Data [3]	0
2	R/W Data [2]	0
1	R/W Data [1]	0
0	R/W Data [0]	0

These two registers are reserved for the exclusive use of the CL-GD7541/GD7543 BIOS and must never be written by any application program. They are listed here only for completeness

Bit	Descriptio n
7:0	**Reserved:** These bits are reserved for the Cirrus Logic BIOS.

12.12 SR16: Performance Tuning Register

I/O Port Address: 3C5

Index:16

Bit	Description	Reset Stat e
7	Extra Wait State for Fast VESA VL-Bus	1
6	RDY# Delay for I/O	1
5	RDY# Delay for Memory Write [1]	1
4	RDY# Delay for Memory Write [0]	1
3	FIFO Demand Threshold [3]	0
2	FIFO Demand Threshold [2]	0
1	FIFO Demand Threshold [1]	0
0	FIFO Demand Threshold [0]	0

This register is used to control the delay from ADS# to RDY# and to control the threshold at which the CRT FIFO is refilled. This register must never be written by an application program. It is listed here for completeness only.

Bit **Descriptio n**

7 **Extra Wait State for Fast VESA VL-Bus:**

- When this bit is 1, and when the CL-GD7541/GD7543 is configured for the VESA VL-Bus, one extra wait state is added to both I/O and memory accesses.
- This bit must be 1 if the bus clock is fast, compared to the memory clock.
- In conjunction with the state of SR16[6], this bit controls the CPU1X clock delay from ADS# to RDY# for I/O cycles.
- For further explanation, refer to the tables in SR16[6] and SR16[5:4]

6 **RDY# Delay for I/O :**

- This field applies only when the CL-GD7541/GD7543 is configured for local bus.
- In conjunction with the state of SR16[7], this bit controls the CPU1X clock delay from ADS# to RDY# for read/write I/O cycles.
- The following table summarizes the values:

SR16		CPU1X Clock Dela y (in wait states)
[7]	[6]	
0	0	1 wait state
0	1	2 wait states
1	0	2 wait states
1	1	3 wait states (default)

12.12 SR16: Performance Tuning Register *(cont.)*

Bit | **Description**

5:4 **RDY# Delay for Memory Write [1:0] :**

- This field is used to control the delay from ADS# to RDY# for memory write cycles.
- This field applies only when the CL-GD7541/GD7543 is configured for local bus.
- The table below summarizes values that may be programmed into this field. The value programmed must satisfy the following inequality:
  [(wait states minus 1) × CPU Clock Period] ≥ [(3 × MCLK Period) + 2 ns]

SR16			CPU1X Clock Delay (in wait states)
[7]	[5]	[4]	
0	0	0	2 wait states
0	0	1	3 wait states
0	1	0	4 wait states
0	1	1	5 wait states
1	0	0	3 wait states
1	0	1	4 wait states
1	1	0	5 wait states
1	1	1	6 wait states (default)

3:0 **FIFO Demand Threshold [3:0] :**

- The value written to this field selects the level at which the sequencer begins cycles to refill the CRT FIFO (and thereby hold off CPU cycles).
  - — The greater the value written to this field, the higher the priority of CRT FIFO access over CPU cycles.
  - — An exception is the value '0000', which gives the highest priority to the CRT FIFO access.
- For each Graphics mode and MCLK frequency, this field has an optimum value that uses the display memory bandwidth most efficiently.

12.13 SR18: Signature Generator Control Register

I/O Port Address: 3C5

Index:18

Bit	Description	Reset State
7	LCD Signature Generator Enable	0
6	Reserved	
5	Reserved	
4	Pixel Data Bus Bit Select [2]	0
3	Pixel Data Bus Bit Select [1]	0
2	Pixel Data Bus Bit Select [0]	0
1	Signature Generator Reset	0
0	Signature Generator Enable / Status	0

This register is used to control and monitor the status of the CL-GD7541/GD7543 signature generator, which is used for board-level testing of the video sub-system. For a complete description of the signature generator, refer to Appendix I.

Bit **Description**

7 **LCD Signature Generator Enable:**
When this bit is 1, the LCD signature generator is enabled.

6:5 **Reserved**

4:2 **Pixel Data Bus Bit Select [2:0] :**
This field is used to select the Feature Connector Pixel Data Bus bit that is used as the input for the signature generator according to the following table:

SR18			Feature Connector Pixel Data Bus Bit
[4]	[3]	[2]	
0	0	0	FCP[0]
0	0	1	FCP[1]
0	1	0	FCP[2]
0	1	1	FCP[3]
1	0	0	FCP[4]
1	0	1	FCP[5]
1	1	0	FCP[6]
1	1	1	FCP[7]

12.13 SR18: Signature Generator Control Register *(cont.)*

Bit	Description
1	**Signature Generator Reset:** When this bit is: • 1, the signature generator is reset to an initial, defined condition. • 0, the signature generator is allowed to run under the control of SR18[0].
0	**Signature Generator Enable / Status:** • When this bit is 1, the signature generator is enabled and begins operation on the next VSYNC. From the Feature Connector Pixel Bus bit chosen by SR18[4:2], the signature generator accumulates a signature for one video frame and then stops, forcing this bit to 0. • By monitoring the status of this bit, the program can determine when the signature is complete.

12.14 SR19: Signature Generator Result Low Register

I/O Port Address: 3C5

Index: 19

Bit	Description	Reset State
7	Signature Generator Result [7]	0
6	Signature Generator Result [6]	0
5	Signature Generator Result [5]	0
4	Signature Generator Result [4]	0
3	Signature Generator Result [3]	0
2	Signature Generator Result [2]	0
1	Signature Generator Result [1]	0
0	Signature Generator Result [0]	1

For a complete description of the signature generator refer to Appendix I.

Bit	Description
7:0	**Signature Generator Result [7:0]**: This register is used to read the low-order byte of the signature generator result

12.15 SR1A: Signature Generator Result High Register

I/O Port Address: 3C5

Index: 1A

Bit	Description	Reset State
7	Signature Generator Result [15]	0
6	Signature Generator Result [14]	0
5	Signature Generator Result [13]	0
4	Signature Generator Result [12]	0
3	Signature Generator Result [11]	0
2	Signature Generator Result [10]	0
1	Signature Generator Result [9]	0
0	Signature Generator Result [8]	0

For a complete description of the signature generator refer to Appendix I.

Bit	Description
7:0	**Signature Generator Result [15:8]**: This register is used to read the high-order byte of the signature generator result

12.16 SR1B,SR1C,SR1D,SR1E: Denominator/Post-scalar for VCLK 0,1,2,3

I/O Port Address: 3C5

Index: 1B, 1C, 1D, 1E

Bit	Description	Access	Reset State
7	Reserved		
6	Reserved		
5	VCLK Denominator [4]	R/W	See table below
4	VCLK Denominator [3]	R/W	See table below
3	VCLK Denominator [2]	R/W	See table below
2	VCLK Denominator [1]	R/W	See table below
1	VCLK Denominator [0]	R/W	See table below
0	VCLK Post-Scalar	R/W	See table below

These registers are used in conjunction with Extension registers SRB to SRE to establish the frequency of the four possible video clocks. The video clock used is selected by MISC[3:2].

This register establishes the denominator and post-scalar values. For information on the numerator, refer to Section 12.5. For more information on clock options, refer to Appendix G.

Each video clock frequency is determined by the following equation.

$$VCLKn\ (\text{MHz}) = \frac{OSC \times NR}{DR \times [P+1]}$$

Equation 12-2

where:

VCLK n	=	Video clock frequency n, where n = 0, 1, 2, 3
OSC	=	Input clock frequency of 14.318 MHz
Numerator **R**egister	=	Value of register bits SRi [6:0], where i = B, C, D, E
Denominator **R**egister	=	Value of register bits SR1i [5:1], where i = B, C, D, E
Post-scalar	=	Value of register bits SR1i [0], where i = B, C, D, E

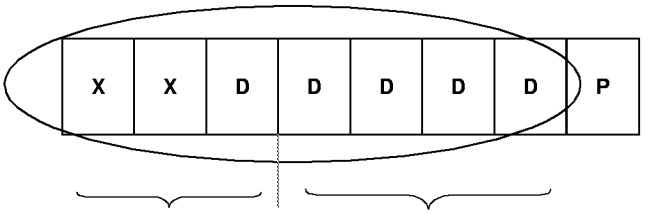
If n = 0, then i = B.
If n = 1, then i = C.
If n = 2, then i = D.
If n = 3, then i = E.

The following table shows the reset values of the registers that determine the video clock frequency. The table also shows the corresponding video clock frequency at system reset.

12.16 SR1B, SR1C, SR1D, SR1E: Denominator/Post-scalar for VCLK 0,1,2, 3 *(cont.)*

VCLKn Frequency		VCLKn Numerator Values			VCLKn Denominator Values			
VCLKn	VCLKn Frequency at Reset	Numerator Register and Hex Value in Register		*NR* = Value Used in Equation Numerator	Denominator Register and Hex Value in Register		*DR* = Value Used in Equation Denominator, Resulting from Post-scalar	*P* = Post-Scalar Value Used in Equation Denominator
	MHz	Register (SRi)	Hex	Decimal Equivalent of Hex Value	Register (SRi)	Hex	Decimal	Decimal
VCLK0	25.180	SRB	66h	102	SR1B	3Bh	29	1
VCLK1	28.325	SRC	5Bh	91	SR1C	2Fh	23	1
VCLK2	41.165	SRD	45h	69	SR1D	30h	24	0
VCLK3	36.082	SRE	7Eh	126	SR1E	33h	25	1

Bit	Description
7:6	**Reserved**
5:1	**VCLK Denominator [4:0]:** These bits determine the denominator value (*D*) used to determined the video clock frequency. For the equation, the post-scalar bit (*P*) is ignored, which has the effect of shifting all bits in the register to the right.
0	**VCLK Post-scalar:** This bit determines the post-scalar value (*P*) used to determine the video clock frequency. This bit defines a divide-by-one or divide-by-two operator in the denominator. (If the post-scalar is 1, then the voltage-controlled oscillator is running at two times OSC, the input clock frequency.)



UPPER VALUE = VALUES IN X XD LOWER VALUE = VALUES IN DDDD

The circled area contains the value that is extracted, converted to decimal, and substituted into the equation.

12.17 SR1F: MCLK Frequency and VCLK Source Select Register

I/O Port Address: 3C5

Index: 1F

Bit	Description	Reset State
7	Not Used	Not applicable
6	VCLK Source Select	0
5	MCLK Frequency [5]	(Refer to MCLK Table below)
4	MCLK Frequency [4]	(Refer to MCLK Table below)
3	MCLK Frequency [3]	(Refer to MCLK Table below)
2	MCLK Frequency [2]	(Refer to MCLK Table below)
1	MCLK Frequency [1]	(Refer to MCLK Table below)
0	MCLK Frequency [0]	(Refer to MCLK Table below)

This register is used to program the MCLK frequency. This register must never be programmed by an applications program. It is listed here only for completeness.

Bit **Description**

7 **Not Used**

6 **VCLK Source Select :**
When this bit is:
- 0, the VCLK synthesizer operates normally.
- 1, VCLK is derived from MCLK as follows:

SR1F[6]	SR1E[0]	VCLK Source
0	X	VLCK (Normal Operation)
1	0	VCLK = MCLK
1	1	VCLK = (MCLK ÷ 2)

5:0 **MCLK Frequency [5:0] :**
- To directly program the MCLK frequency, use the following equation: SR1F[5:0] × [Reference Frequency ÷ 8] = Desired MCLK.
- For DRAM requirements for MCLK frequencies, refer to Appendix F..
- This field may be programmed with values from 21 to 38 (decimal).
- The following table assumes a reference frequency of 14.318 MHz.

SR1F[5:0] in Decimal and Hex	[Reference Frequency ÷ 8] =	Desired MCLK Frequency
21 (15h)	1.79	37.585 MHz
23 (17h)		41.165 MHz
24 (18h, the default, at-reset value)		**42.955 MHz**
25 (19h)		44.744 MHz
26 (1Ah)		46.534 MHz
28		50.114 MHz

12.18 SR20: Miscellaneous Control Register 2

I/O Port Address: 3C5

Index: 20

Bit	Description	Reset State
7(MSB)	Display Memory Data Latch Select on Next CAS# Rising Edge	0
6	RAS# Cycle Time Select	0
5	LCD Data and Control Pins Tristated (CL-GD7541 Only)	0
4	Dynamic Frame-Buffer Sharing Pull-up Readback (CL-GD7541 Only)	0
3	LCD Power-Management Pins Tristated (CL-GD7541 Only)	0
2	CRT FIFO Request Threshold (CL-GD7541 Only)	0
1	Display Memory Interface-Input Threshold Select	0
0(LSB)	CPU Bus Interface-Input Threshold Select	0

This register is reserved exclusively for the CL-GD7541/GD7543 BIOS and must never be written by an application program. It is listed here only for completeness.

Bit **Description**

7 **Display Memory Data Latch Select on Next CAS# Rising Edge :**
When this bit is:
- 0, display memory data bits are latched on the CAS# trailing edge.
- 1, display memory data bits are latched on the next CAS# rising edge. (This bit should be asserted with most EDO/Hyper-Page-Mode DRAMs.)

6 **RAS# Cycle Time Select :**
This bit works in conjunction with Extension register SRF[2] to determine the length of the RAS# cycle time, as shown in the following table:

SR20[6]	SRF[2]	Length of RAS# Cycle	Type of RAS# Cycle
0	0	7 MCLKs	4 low and 3 high
0	1	6 MCLKs	3.5 low and 2.5 high
1	0	9 MCLKs	5 low and 4 high
1	1	8 MCLKs (CL-GD7541 only)	4.5 low and 3.5 high

12.18 SR20: Miscellaneous Control Register 2 *(cont.)*

Bit	Descriptio n
5	**LCD Data and Control Pins Tristated (CL-GD754 1 Only) :** When this bit is: • 0, LCD data and control pins operate normally. (This condition is the default.) • 1, LCD data and control pins are tristated. — The following LCD data and control pins are tristated for all LCD panels: SUD[7:0], SLD[7:0], FP[3]/MOD, FP2, FPVDCLK, LLCLK, LFS, and FPDE — The following LCD data and control pins are tristated only if a 24-bit TFT panel is selected (that is, Extension register bits R9X[1:0] are set to '11'): FP[0], FP[1], FP[8], FP[9], FP[16], and FP[17]. — The following LCD panel power-management pins are not affected by SR20[5]: FPVCC, FPBL, and FPVEE. Although these pins are panel-related, they are instead controlled by SR20[3].
4	**Dynamic Frame-Buffer Sharing Pull-up Readback (CL-GD754 1 Only) :** When the MD[24] pin: • Does not have a pull-up resistor, this bit is a 0, and the CL-GD7541 is not configured for dynamic frame-buffer sharing. In this case, the state of the signals on the SW1 and SW2 pins are read back into SR24[2:0]. • Has a pull-up resistor, this bit is a 1, and the CL-GD7541 is configured for dynamic frame-buffer sharing as follows: — The SW1 pin becomes an active-low pin, MGNTO#. — The SW2 pin becomes an active-high pin, MRQIN. — The function of the panel switches SW1 and SW2 moves to external pull-ups on MD[26] and MD[27], in which case for each pin a pull-up results in a '1' on the pin. (The pull-down, which results in a '0' on each pin, is internal to the CL-GD7541.) — Independent of the value of Extension register SR22[6], the state of panel switches SW1 and SW2 read back into the same register bits, SR24[2:0]. — The SW0 / MCLK / XMCLK pin is configured as an MCLK output that is used by the controller that shares the frame buffer with the CL-GD7541 VGA controller.
3	**LCD Power-Management Pins Tristated (CL-GD754 1 Only) :** This bit affects the CL-GD7541 LCD power pins FPVCC, FPBL, and FPVEE. When this bit is: • 0, the above-mentioned LCD power pins operate normally and are driving. (This condition is the default.) • 1, the above-mentioned LCD power pins are tristated.

12.18 SR20: Miscellaneous Control Register 2 *(cont.)*

Bit	Description
2	**CRT FIFO Request Threshold (CL-GD7541 Only):** This bit affects only the CL-GD7541. It takes effect only in graphics (all-points-addressable) mode *and* when Extension register SRF[5] is 1. When this bit is: • 0, the CRT FIFO asserts a request for new data as soon as any data bits are transferred out of the CRT FIFO. • 1, the CRT FIFO asserts a request for new data only after the CRT FIFO has emptied half of its data.
1	**Display Memory Interface-Input Threshold Select:** When this bit is: • 0, display memory interface-input thresholds are at TTL levels. • 1, display memory interface-input thresholds are at CMOS levels.
0	**CPU Bus Interface-Input Threshold Select:** When this bit is: • 0, CPU bus interface-input thresholds are at TTL levels. • 1, CPU bus interface-input thresholds are at CMOS levels.

12.19 SR21: Dual-Scan Color Control Registe r

I/O Port Address: 3C5

Index: 21

Bit	Description	Reset Stat e
7(MSB)	Refresh-Per-Line Select	0
6	Dual-Scan STN Color Select	0
5	Frame Buffer Cycle Stop	0
4	Hardware Cursor-Size Select	0
3	Inverted VCO Output Used as VCLK	0
2	Reserved	
1	Reserved	
0(LSB)	Reserved	

The SR21[7] and [4] bits are available for programming the CL-GD7541/GD7543. However, in contrast, the SR21[5,2:0] bits are reserved for manufacturing testing and must never be written by an application program.

Bit	Descriptio n
7	**Refresh-Per-Line Select:** • When this bit is 1, one refresh cycle per scanline is selected. • When this bit is 0, CRT Controller register CR11[6] selects either three or five refresh cycles per scanline. (This default state of this bit is 0.)
6	**Dual-Scan STN Color Selec t**: • Extension register bits CR2C[7:6] must be set to 10 to select STN color LCDs. • When CR2C[7:6] is 10 *and* this bit is: — 1, dual-scan STN color mode is selected. — 0, single-scan STN color mode is selected.
5	**Frame Buffer Cycle Stop :** When this bit is 1, at the end of a RAS# cycle, any requests for a frame buffer are stopped. This bit is for test purposes only.
4	**Hardware Cursor-Size Selec t**: • Extension register SR12[2] must be programmed the same as this bit. • When SR12[0] is 1 *and* this bit is: — 1, the 64 × 64-pixel hardware cursor is selected. — 0, the 32 × 32-pixel hardware cursor is selected. • For hardware cursor pattern choices, refer to SR13[4:0].
3	**Inverted VCO Output Used as VCLK :** • When this bit is 1, VCLK is the inverse of the output from the VCO. • When this bit is 0, VCLK is the same as the output from the VCO. This bit setting allows the CL-GD7541/GD7543 to take advantage of the VCO duty cycle skew to maximize high-frequency operations.
2:0	**Reserved :** These bits are for test purposes only.

12.20 SR22: Hardware Configuration Read Register 1

I/O Port Address: 3C5

Index: 22

Bit	Description	Access	Reset State
7	PCI Minimum Grant	R	= MD[23]
6	DFBS Readback (CL-GD7541 Only)	R	= MD[22]
5	Sleep Mode Address Select	R	= MD[21]
4	Reserved		
3	External Clock Select	R	= MD[19]
2	VESA VL-Bus > 33 MHz Select	R	= MD[18]
1	Reserved		
0	PCI 32-Bit Bus Select	R	= MD[16]

This register contains a read-only field that allows the BIOS to determine configuration information for bus type, sleep address, and external clock by reading the level on the indicated MD pins during the low-to-high transition of the system reset pulse.

- All these MD pins have pull-down resistors internally, and so the default readings are all 0.
- An external 60k-Ω pull-up resistor is needed to establish a high (1) on these pins.

Bus-select bits SR22[7,2,0] are mutually exclusive. Only *one* can be high at any time.

- If there are no external pull-ups on SR22 bus-select bits 7, 2, and 0, the CL-GD7541/GD7543 is configured for VESA VL-Bus operation ≤ 33 MHz.
- If there are no external pull-ups on *any* of the SR22 bus-select bits, the CL-GD7541/GD7543 is configured for VESA VL-Bus operation ≤ 33 MHz. In addition, the CL-GD7541/GD7543 is configured with internal clock synthesizers and a sleep address of 3C3h.

Bit	Description
7	**PCI Minimum Grant:** • An external pull-up on MD[23] / PCI-MGPU reads back a 1. In this case: — The PCI burst cycle to the CL-GD7541/GD7543 must be a minimum of 16 CPU clock cycles. — PCI Configuration register 3Ch, Offset 2 reads back a 1, allowing the PCI core logic to detect the presence of the pull-up resistor. — The CL-GD7541/GD7543 expects a default minimum grant value of 8 bus clocks. — A pull-up must not be used on MD[16] / PCIPU, as only one PCI bus external configuration pull-up must be used (either PCI-MGPU or PCIPU). • No external pull-up on MD[23] / PCI-MGPU reads back a 0. In this case: — The PCI burst cycle to the CL-GD7541/GD7543 is 8 CPU clock cycles. — PCI Configuration register 3Ch, offset 2 reads back a 0. • Normally, no pull-up is required on MD[23] / PCI-MGPU.

12.20 SR22: Hardware Configuration Read Register 1 *(cont.)*

Bit	Descripti on
6	**DFBS Readbac k (CL-GD754 1 Only):** • An external pull-up on MD[22] / DFBSPU reads back a 1, which configures the CL-GD7541 for dynamic frame-buffer sharing as follows: — The SW0 pin outputs the value of MCLK, as controlled by Extension register SR12[4]. — The SW1 pin becomes an active-low pin, Memory Grant (MGNT0#). — The SW2 pin becomes an active-high pin, Memory Request Input (MRQIN). — The MD[26] pin becomes SW1PU, and MD[27] pin becomes SW2PU. The pins read back the data on the same registers as for SW1 (SR24[1]) and SW2 (SR24[2]). • No external pull-up on MD[22] / DFBSPU reads back a 0, so that the switch pins SW2:0 are used as they are normally.
5	**Sleep Mode Address Select :** • An external pull-up on MD[21] / S46PU reads back a 1, which selects I/O address 46E8h as the sleep mode address. • No external pull-up on MD[21] / S46PU reads back a 0, indicating the selection of sleep mode address 3C3h, the default.
4	**Reserve d**
3	**External Clock Select :** • An external pull-up on MD[19] / XCLKPU reads back a 1, powering down the internal clock for MCLK and VCLK, and enabling the external XMCLK and XVCLK clock inputs. (This external pull-up is used for manufacturing test and for logic simulations by Cirrus Logic.) • No external pull-up on MD[19] / XCLKPU reads back a 0, so that the internal clock MCLK and VCLK are used by default.
2	**VESA VL-Bus > 33 MHz Select:** • An external pull-up on MD[18] / FVLPU reads back a 1, selecting a fast VESA VL-Bus operation at > 33 MHz. • No external pull-up on MD[18] / FVLPU reads back a 0, selecting a VESA VL-Bus operation ≤ 33 MHz.
1	**Reserve d**
0	**PCI 32-bit Bus Select :** • An external pull-up on MD[16] / PCIPU reads back a 1, configuring the CL-GD7541/GD7543 for 32-bit PCI bus operation. • No external pull-up on MD[16] / PCIPU reads back a 0, configuring the CL-GD7541/GD7543 for VESA VL-Bus operation ≤ 33 MHz.

12.21 SR23: Software Configuration Register 1

I/O Port Address: 3C5

Index:23

Bit	Description	Reset State
7	FCVCLK Enable	0
6	ACTI / FCEVIDEO# / SBYI Select	0
5	BLI / SUSPI Select	0
4	VCLK Output Enable	0
3	Extended-Data-Out / Hyper-Page-Mode DRAM Select	0
2	MCLK VCO Output Select	0
1	Zero Wait State for Test Mode	0
0	SW0 / MCLK / XMCLK Select	0

This register contains a read-only field that allows for miscellaneous configurations.

Bit — **Description**

7 — **FCVCLK Enable:**
A 1 in this bit enables the FCVCLK input to drive either the RAMDAC or the video clock (VCLK), depending on the state of External/General register MISC[3]. When SR23[7] is 1 *and*:
- MISC[3] is 0, FCVCLK is sent only to the RAMDAC, enabling only that part of the CL-GD7541/GD7543.
- MISC[3] is 1, FCVCLK is used to drive VCLK, which clocks the entire CL-GD7541/GD7543.
- There is a high on the TVON pin, the TVON high signal forces MISC[3] to 1. In this case also, FCVCLK is used to drive VCLK, which clocks the entire CL-GD7541/GD7543.

6 — **ACTI / FCEVIDEO# / SBYI Select:**
When SR24[7] is 0 *and* this bit is:
- 0, the ACTI / FCEVIDEO# / SBYI pin is configured as SBYI, the hardware-controlled Standby input.
- 1, the ACTI / FCEVIDEO# / SBYI pin is configured as ACTI, the Activity sense input for resetting the power-down timers.

When SR24[7] is 1:
- The ACTI / FCEVIDEO# / SBYI pin is always configured as FCEVIDEO#, the Feature Connector Video Port, regardless of the SR23[6] value.

5 — **BLI / SUSPI Select :**
When this bit is:
- 0, the BLI / SUSPI pin is configured for SUSPI, the hardware-controlled Suspend input.
- 1, *and* SR24[7] is 0, the BLI / SUSPI pin is configured for BLI, the Backlight Input control.

12.21 SR23: Software Configuration Register 1 *(cont.)*

Bit **Descriptio n**

4 **VCLK Output Enable :**
When this bit is:
- 0 (the default), the VCLK output is low.
- 1, the internal VCLK is available for testing on the VCLK / FCDCLK pin, independent of SR22[3] (the external/internal clock selection).

NOTE : When SR24[7] = 1, internal VCLK is also available on the FCDCLK output

3 **Extended -Data-Out / Hyper-Page-Mode DRAM Select :**
Before any access can be made to video memory, this bit *must* be set properly according to the type of DRAM that is installed in the system. Set this bit to:
- 0 when standard DRAMs are installed and standard DRAM timing is required
- 1 when either EDO (Extended-Data-Out) DRAMs or Hyper-Page-Mode DRAMs have been installed in the system, and EDO DRAM timing is required

2 **MCLK VCO Output Select :**
This bit can be used to test the clock synthesizer. When the SW0 / MCLK / XMCLK pin is configured for MCLK (SR22[3] is 0 *and* SR23[0] is 1), *and* this bit is:
- 0, the MCLK output is the value programmed into SR12[4], which selects one of two values – either MCLK VCO (that is, MVCO) or the quantity MVCO ÷ 2.
- 1, the MCLK output is MVCO (and not MVCO ÷ 2).

SR22[3]	SR23		SW0 / MCLK / XMCLK Pin Statu s
	[0]	[2]	
0	0	Don't care	SW0 Input
0	1	0	MCLK Output is either MVCO or (MVCO ÷ 2)
0	1	1	MCLK Output is MVCO
1	Don't care	Don't care	XMCLK Input

1 **Zero Wait State for Test Mod e:**
- When this bit is 0 (the default), there is one wait state.
- When this bit is 1, zero wait states are enabled for test purposes only.

0 **SW0 / MCLK / XMCLK Selec t:**
This bit works in conjunction with SR22[3] to determine the configuration of the SW0 / MCLK / XMCLK pin as shown in the following table:

SR22[3]	SR23[0]	SW0 / MCLK/ XMCLK Pin Statu s
0	0	SW0 Input
0	1	MCLK Output
1	Don't care	XMCLK Input

12.22 SR24: LCD-Type Switches and Feature Connector Enable

I/O Port Address: 3C5

Index:24

Bit	Description	Reset State
7	Feature Connector Video Port Enable	= MD[25]
6	FCVCLK Invert Enable	0
5	Fast 16-Bit CPU Bus Access Enable	0
4	FCDCLK Output Select	0
3	All External Pull-Ups Read under Software Control	Pull-up Values
2	SW2 Pin Read	Switch Value
1	SW1 Pin Read	Switch Value
0	SW0 Pin Read	Switch Value

Bit	Description
7	**Feature Connector Video Port Enable:** • An external pull-up resistor on MD25 / FCPU configures all appropriate pins for the Feature Connector Video Port. (Refer to pin descriptions in Chapter 2.) • When no pull-up is used, the above-mentioned pins revert to their other functions or are disabled (that is, inputs are ignored and outputs are high impedance).
6	**FCVCLK Invert Enable (CL-GD7543 Only):** When this bit is 1, it enables the polarity of the FCVCLK signal to be inverted.
5	**Fast 16-Bit CPU Bus Access Enable:** When this bit is: • 0, the RDY# / TRDY# output is delayed for 16-bit accesses by one bus-clock cycle to minimize bus contention problems. • 1, the clock delay is removed, which allows faster bus access. This bit works with both the VESA VL-Bus and the PCI bus.
4	**FCDCLK Output Select:** This bit is used to select the clock signal for the FCDCLK pin. When this bit is: • 1, — The selection is the VCLK VCO output clock. — Then even if Extension register SR23[7] is 1, the internal VCLK clock synthesizer outputs the internal clock to the VCLK output pin. This configuration is used with the Feature Connector for Video Overlay. • 0, the selection is for the DCLK dot clock that Sequencer register SR1[3] does *not* derive by dividing VCLK by 2.

12.22 SR24: LCD-Type Switches and Feature Connector Enable *(cont.)*

Bit	Description
3	**All External Pull-Ups Read Under Software Control:** • When hardware control is used, the state of all external pull-ups on the memory data pins (MD31:0) are read and latched by the CL-GD7541/GD7543 during hardware reset only. • When software control is used, any 1-to-0 transition of this bit allows the state of all external pull-ups on the memory data pins to be read and latched by the CL-GD7541/GD7543 at any time, not just at hardware reset. Software control is used when: — Power is turned off to all parts of the CL-GD7541/GD7543. — The system reset pulse is too short to read the switches that have large pull-up or pull-down resistance.
2:0	**SW2 to SW0 Pin Read:** These read-only bits reflect the inverse of the active level of switch inputs SW2 to SW0 respectively. • During normal operation, switch inputs SW2 to SW0 are directly read continuously on the I/O bus, and so they are not latched at hardware reset. As a result, they do not need a software read for a save or restore operation. They are not affected by SR24[3]. • These bits are normally for BIOS use.

12.23 SR25: Timer-Software Reset and Hardware Configuration 2

I/O Port Address: 3C5

Index:25

Bit	Description	Reset State
7	Dynamic Frame-Buffer Sharing Enable (CL-GD7541 Only)	0
6	External RAMDAC Address / Chip Select	0
5	1-Bit/Pixel Packed-Pixel Mode Enable	0
4	External XVCLK Input Enable	0
3	4-Bit/Pixel Packed-Pixel Mode Enable	0
2	Effect of CR1B[1] on CRT Address Disable (CL-GD7543 Only)	0
1	Standby Mode Timer Reset by I/O Read to Keyboard	0
0	Backlight Timer Reset by I/O Read to Keyboard	0

Bit **Description**

7 **Dynamic Frame-Buffer Sharing (DFBS) Enable (CL-GD7541 Only):**
When this bit is:
- 0, even if the signal on the DFBSPU pin is high *and* Extension register SR22[6] is 1, the DFBS function is disabled, and the MRQIN signal has no effect on memory arbitration.
- 1, *and* the system is configured for DFBS, then this bit enables the DFBS function for those software applications that use it.

6 **External RAMDAC Address / Chip Select:**
- When this bit is 0, the TVON pin is controlled by Extension register CR30[3].
- When this bit is 1,
  - — The TVON output becomes the external RAMDAC Chip Select. At system reset, both the TVON and RAMDAC Select functions are inactive-low. As a result, no matter how the chip comes up, external RAMDAC is not affected.
  - — It disables the internal DAC and RAMDAC RAM I/O readback. The RAM continues to be updated by RAMDAC writes, but it does not respond to any RAMDAC read except 3C7.
  - — In VESA VL-Bus mode, the CL-GD7541/GD7543 does not assert LDEV# and RDY.
  - — In PCI bus mode, the CL-GD7541/GD7543 does not support external RAMDAC related to I/O select or shadowing.
- This bit must be set to 1, *before* TV-OUT feature is enabled CR30[3] is 1), to ensure that the TVON pin becomes the external RAMDAC Chip Select

5 **1-Bit/Pixel Packed-Pixel Mode Enable:**
When this bit is 1, the 1-bit-per-pixel packed-pixel mode is enabled.

4 **External XVCLK Input Enable:**
When this bit is 1 and when SR22[3] is 0, an external 14.318-MHz input must be connected to the OSC / XVCLK input pin. (However, in this case MCLK does not use this input. Instead, it still uses the internal MVCO source.)
- On VCLK generation, this bit is OR'ed with SR22[3].
- This bit is to be used for NTSC-Out.

12.23 SR25: Timer-Software Reset and Hardware Configuration 2 *(cont.)*

Bit | **Descripti on**

3 — **4-Bit/Pixel Packed-Pixel Mode Enable :**
When this bit is 1, a 4-bit-per-pixel packed-pixel mode is enabled.

2 — **Effect of CR1B[1] on CRT Addres s Disable (CL-GD754 3 Only):**
For CRT addresses, this bit overrides Extension register CR1B[1], which has the effect of limiting the CRT and CPU addresses.

- When this bit is 0:
  - — The CRT display can access only the display memory for standard VGA modes. In contrast, the CPU can access the entire display memory.
  - — *And* CR1B[1] is 1, this bit setting is used to update hardware icon and hardware cursor mapping in standard VGA modes.
- When this bit is 1:
  - — Both the CRT display and the CPU can access the entire display memory.
  - — This bit setting is used with extended graphics modes that require more display memory than the display memory for standard VGA modes.
  - — Display memory for standard VGA modes must be reduced in size in order to wrap around (an effect used by many applications for fast scrolling).
  - — The table below gives the bit settings that result in extended memory access for the CPU and CRT.

SR25[2]	CR1B[1]	CPU Memory Accesse s	CRT Memory Accesse s
0	0	Access limited to VG A	Access limited to VG A
0	1	Extended memory acces s	Access limited to VG A
1	0	Access limited to VG A	Access limited to VG A
1	1	Extended memory acces s	Extended memory acces s

1 — **Standby Mode Timer Reset by I/O Read to Keyboard :**
This bit is used to reset the internal Standby mode timer, when there is an I/O read to the keyboard controller (port 60h).

0 — **Backlight Timer Reset by I/O Read to Keyboard :**
This bit is used to reset the internal backlight timer, when there is an I/O read to the keyboard controller (port 60h).

12.24 SR26: Shader Signature Low Registe r

I/O Port Address: 3C5

Index:26

Bit	Description	Reset Stat e
7	Shader Signature [7]	0
6	Shader Signature [6]	0
5	Shader Signature [5]	0
4	Shader Signature [4]	0
3	Shader Signature [3]	0
2	Shader Signature [2]	0
1	Shader Signature [1]	0
0	Shader Signature [0]	0

The Shader Signature field is used for factory testing only. Application programsmust not use the Shader Signature registers, which are listed here only for completeness.

Bit	Descriptio n
7:0	**Shader Signature [7:0] :** This register contains the least-significant byte for the Shader Signature. For the most-significant byte, refer to SR27. The Shader Signature field is used to test the CL-GD7541/GD7543 shader logic.

12.25 SR27: Shader Signature High Registe r

I/O Port Address: 3C5

Index: 27

Bit	Description	Reset Stat e
7	Shader Signature [15]	0
6	Shader Signature [14]	0
5	Shader Signature [13]	0
4	Shader Signature [12]	0
3	Shader Signature [11]	0
2	Shader Signature [10]	0
1	Shader Signature [9]	0
0	Shader Signature [8]	0

The Shader Signature field is used for factory testing only. Application programsmust not use the Shader Signature registers, which are listed here only for completeness.

Bit	Descriptio n
7:0	**Shader Signature [15:8] :** This register contains the most-significant byte for the Shader Signature. For the most-significant byte, refer to SR26. The Shader Signature field is used to test the CL-GD7541/GD7543 shader logic.

12.26 SR28 and SR29 Scratchpad Registers 5 and 6

I/O Port Address: 3C5

Index: 28 and 29

Bit	Description	Reset Stat e
7	R/W[7]	
6	R/W[6]	
5	R/W[5]	
4	R/W[4]	
3	R/W[3]	
2	R/W[2]	
1	R/W[1]	
0	R/W[0]	

These two registers are reserved for the exclusive use of the CL-GD7541/GD7543 BIOS. They must never be written by any application program.

There are a total of thirteen 18-bit scratchpad registers available in the RAMDAC RAM. They are accessed as any RAMDAC RAM register, in groups of three I/O accesses. These registers are listed here only for completeness.

Bit	Descriptio n
7:0	**Reserved :** These bits are reserved for the use of CL-GD7541/GD7543 BIOS.

12.27 SR2A: Hardware Icon #0 Control Registe r

I/O Port Address: 3C5

Index:2A

Bit	Description	Reset Stat e
7	Reserved	
6	Hardware Icon Fine Horizontal Position [3]	0
5	Hardware Icon #0 Display Memory Map Selection	0
4	Hardware Icon #0 Vertical Scanline Doubling	0
3	Hardware Icon #0 Horizontal Pixel Doubling	0
2	Hardware Icon #0 Blink Enable	0
1	Hardware Icon #0 Display Mode Select	0
0	Hardware Icon #0 Display Enable	0

Bit **Descriptio n**

7 **Reserve d**

6 **Hardware Icon Fine Horizontal Position [3]:**
This bit is the most-significant bit of a 4-bit word that is used with 9-dot and 10-dot fonts (character clocks), when in text or horizontally expanded graphics modes.
- The least-significant bits [2:0] are in Sequencer register SRX[7:5].
- The coarse horizontal position is in Extension register SR10.

NOTE: When horizontal expansion from 640 to 800 is enabled, the hardware icon must be positioned within 10 dots.

5 **Hardware Icon #0 Display Memory Map Selection:**
- When this bit is 0, display memory map 0 is selected for Icon #0.
- When this bit is 1, display memory map 1 is selected for Icon #0.

4 **Hardware Icon #0 Vertical Scanline Doubling:**
When this bit is 1:
- Icon #0 displays 128 scanlines, but each scanline is replicated vertically.
- Icon #0 extends down and forces all other icons down.

3 **Hardware Icon #0 Horizontal Pixel Doubling:**
When this bit is 1:
- Icon #0 displays 128 pixels, but each pixel is replicated horizontally.
- Icon #0 expands to the right on the display.

2 **Hardware Icon #0 Blink Enable :**
- When this bit is 1, icon #0 blinks at one-half the text-cursor blink rate.
- When this bit is 0, icon #0 is steady state.

1 **Hardware Icon #0 Display Mode Select:**
The hardware icon is always 2 bits/pixel and is controlled by these two bits.
- When this bit is 0, the 4-color display mode for icon #0 is selected.
- When this bit is 1, the 3-colors-and-transparent display mode is selected.

0 **Hardware Icon #0 Display Enable:**
When this bit is 1, icon #0 is enabled to display.

12.28 SR2B: Hardware Icon #1 Control Registe r

I/O Port Address: 3C5

Index:2B

Bit	Description	Reset Stat e
7	FPVDCLK and LLCLK High Drive	0
6	Monitor Sense Assist Bit	0
5	Hardware Icon #1 Display Memory Map Selection	0
4	Hardware Icon #1 Vertical Scanline Doubling	0
3	Hardware Icon #1 Horizontal Pixel Doubling	0
2	Hardware Icon #1 Blink Enable	0
1	Hardware Icon #1 Display Mode Select	0
0	Hardware Icon #1 Display Enable	0

Bit	Descriptio n
7	**FPVDCLK and LLCLK High Drive :** When this bit is 1, FPVDCLK and LLCLK have double the normal output drive to support high-load LCDs.
6	**Monitor Sense Assist Bit :** When this bit is 1: • The internal BLANK# signal to the DAC is disabled, thus allowing border color during the entire non-display time. • *And* Attribute Controller register ARX[5] is 0, this bit can be used to force a monitor display for accurate monitor sense, independent of the following: — CPU speed — CPU interrupts — The Graphics mode
5	**Hardware Icon #1 Display Memory Map Selection:** When this bit is: • 0, display memory map 0 for is selected for icon #1. • 1, display memory map 1 for is selected for icon #1.
4	**Hardware Icon #1 Vertical Scanline Doubling:** When this bit is 1: • Icon #1 displays 128 scanlines, but each scanline is replicated vertically. • Icon #1 extends down and forces all other icons down.
3	**Hardware Icon #1 Horizontal Pixel Doubling:** When this bit is 1: • Icon #1 displays 128 pixels, but each pixel is replicated horizontally. • Icon #1 expands to the right on the display.

12.28 SR2B: Hardware Icon #1 Control Registe r *(cont.)*

Bit	Descriptio n
2	**Hardware Icon #1 Blink Enable:** When this bit is: • 1, the icon blinks at one-half the text-cursor blink rate. • 0, the icon is steady state.
1	**Hardware Icon #1 Display Mode Select:** The hardware icon is always 2 bits/pixel and is controlled by these two bits. When this bit is: • 0, the 4-color display mode for icon #1 is selected. • 1, the 3-colors-and-transparent display mode is selected.
0	**Hardware Icon #1 Display Enable:** When this bit is 1, icon #1 is enabled to display.

12.29 SR2C: Hardware Icon #2 Control and Miscellaneous PCI Registe r

I/O Port Address: 3C5

Index:2C

Bit	Description	Reset Stat e
7	PCI Base Register 14h Enable [31:24]	0
6	PCI Base Register 14h Byte Swap [31:24]	0
5	Hardware Icon #2 Display Memory Map Selection	0
4	Hardware Icon #2 Vertical Scanline Doubling	0
3	Hardware Icon #2 Horizontal Pixel Doubling	0
2	Hardware Icon #2 Blink Enable	0
1	Hardware Icon #2 Display Mode Select	0
0	Hardware Icon #2 Display Enable	0

Bit	Descriptio n
7	**PCI Base Register 14h Enable :** • When this bit is 1, and the CL-GD7541/GD7543 is in PCI bus mode, Base register 14h [31:24] is decoded as a valid address range. • When this bit is 0, this address range is ignored.
6	**PCI Base Register 14h Byte Swap:** When this bit is 1 and the CL-GD7541/GD7543 is in PCI bus mode: • Byte swapping is enabled for the Base register 14h[31:24] address range. • Byte[0] is swapped with byte[1], and byte[2] is swapped with byte[3].
5	**Hardware Icon #2 Display Memory Map Selection:** • When this bit is 0, display memory map 0 is selected for icon #2 • When this bit is 1, display memory map 1 is selected for icon #2
4	**Hardware Icon #2 Vertical Scanline Doubling:** When this bit is 1: • Icon #2 displays 128 scanlines, but each scanline is replicated vertically. • Icon #2 extends down and forces all other icons down.
3	**Hardware Icon #2 Horizontal Pixel Doubling:** When this bit is 1: • Icon #2 displays 128 pixels, but each pixel is replicated horizontally. • Icon #2 expands to the right on the display.
2	**Hardware Icon #2 Blink Enable :** • When this bit is 1, icon #2 blinks at one-half the text-cursor blink rate. • When this bit is 0, icon #2 is steady state.
1	**Hardware Icon #2 Display Mode Select :** The hardware icon is always 2 bits/pixel and is controlled by these two bits. • When this bit is 0, the 4-color display mode for icon #2 is selected. • When this bit is 1, the 3-colors-and-transparent display mode is selected.
0	**Hardware Icon #2 Display Enable:** When this bit is 1, icon #2 is enabled to display.

12.30 SR2D: Hardware Icon #3 Control and HIMEM Select Registe r

I/O Port Address: 3C5

Index:2D

Bit	Description	Reset Stat e
7	HIMEM[1] Reference Bit	0
6	HIMEM[0] Reference Bit	0
5	Hardware Icon #3 Display Memory Map Selection	0
4	Hardware Icon #3 Vertical Scanline Doubling	0
3	Hardware Icon #3 Horizontal Pixel Doubling	0
2	Hardware Icon #3 Blink Enable	0
1	Hardware Icon #3 Display Mode Select	0
0	Hardware Icon #3 Display Enable	0

Bit	Descriptio n
7:6	**HIMEM[1:0] Reference Bits :** These bits are extensions of display memory segment select bits in Extension register SR7[7:4]. The CL-GD7541/GD7543 compares the value in these bits with the levels on the HIMEM[1:0] pins to define the valid upper-address space. • In VESA VL-Bus operations, when CPU bus address bits HIMEM[1:0] = SR2D[7:6] and CPU bus address bits A[23:20] = SR7[7:4], then the CL-GD7541/GD7543 identifies the upper address as its CPU address-mapped area. • In PCI bus operations, when these two bits are non-zero, the chip is in linear memory mode. When SR2D[7:6] or SR7[7:4] are not zero, the PCI memory map is defined by Base registers 10 or 14 (upper bytes). • For segmented addressing mode, these bits must be 0.
5	**Hardware Icon #3 Display Memory Map Selection:** • When this bit is 0, display memory map 0 is selected for icon #3. • When this bit is 1, display memory map 1 is selected for icon #3.
4	**Hardware Icon #3 Vertical Scanline Doubling:** When this bit is 1: • Icon #3 displays 128 scanlines, but each scanline is replicated vertically. • Icon #3 extends down and forces all other icons down.
3	**Hardware Icon #3 Horizontal Pixel Doubling:** When this bit is 1: • Icon #3 displays 128 pixels, but each pixel is replicated horizontally. • Icon #3 expands to the right on the display.
2	**Hardware Icon #3 Blink Enable :** When this bit is: • 1, icon #3 blinks at one-half the text-cursor blink rate. • 0, icon #3 is steady state.

12.30 SR2D: Hardware Icon #3 Control and HIMEM Select Register *(cont.)*

Bit	Description
1	**Hardware Icon #3 Display Mode Select:** The hardware icon is always 2 bits/pixel and is controlled by these two bits. When this bit is: • 0, the 4-color display mode for hardware icon #3 is selected. • 1, the 3-colors-and-transparent display mode is selected.
0	**Hardware Icon #3 Display Enable:** When this bit is 1, hardware icon #3 is enabled to display.

12.31 SR2E: Hardware Cursor Horizontal Position Extension Register

I/O Port Address: 3C5

Index:2E

Bit	Description	Reset State
7	Early OVRW# Signal Delay [2]	0
6	Early OVRW# Signal Delay [1]	0
5	Early OVRW# Signal Delay [0]	0
4	Display Memory-Write Cycle Delay [1]	0
3	Display Memory-Write Cycle Delay [0]	0
2	Hardware Icon #0 Address Map Select [1]	0
1	Hardware Icon #0 Address Map Select [0]	0
0	Hardware Cursor Fine Horizontal Position [3]	0

Bit **Description**

7:5 **Early OVRW# Signal Delay [2:0] :**

These 3 bits define the time interval between the Video Overlay Window output from the CL-GD7541/GD7543 and the data input from the external TV decoder.

- This time interval is used for a time differential adjustment that is intended to compensate for the Feature Connector system delay:
  - — *From* the time the OVRW# output is generated
  - — *To* the time Feature Connector data is presented to the CL-GD7541/GD7543.
- The FCEVIDEO# input must be externally synchronized from the OVRW# output to the data input.
- The table that follows shows early clock cycles for either 1× or 2× DCLKs.
  - — The programmed number of early clock cycles defines the delay between the assertion and de-assertion of OVRW# and the corresponding start and end of the Video Overlay Window.
  - — The 1× DCLKs are typically 25-MHz clocks that are used in clocking Graphics mode 1 for 16-bit pixels.
  - — The 2× DCLKs are typically 50-MHz clocks that are used in clocking Graphics mode 2 for 16-bit pixels.

SR2E			Total Early Clock Cycles	
[7]	[6]	[5]	1× DCLK	2× DCLK
0	0	0	0	3
0	0	1	Don't use	4
0	1	0	Don't use	5
0	1	1	0	6
1	0	0	1	7
1	0	1	2	8
1	1	0	Don't use	2
1	1	1	Don't use	1

12.31 SR2E: Hardware Cursor Horizontal Position Extension Register *(cont.)*

Bit **Description**

4:3 **Display Memory Write Cycle Delay [1:0] :**
These two bits are used to delay the start of a write cycle for display memory in units of MCLKs, as explained in the table below:

SR2E		Delay Start of Display Memory Write Cycle By :	Conditions Under Which to Use :
[4]	[3]		
0	0	3 MCLKs	Use for worst-case timing conditions .
0	1	2 MCLKs	Optimize the 33-MHz PCI bus. Optimize the 50-MHz VESA VL-Bus.
1	0	1 MCLK	Optimize the 33-MHz VESA VL-Bus.
1	1	0 MCLKs	Optimize the 20-MHz VESA VL-Bus.

2:1 **Hardware Icon #0 Address Map Select [1:0] :**
- When this field is zero, each icon has two memory maps assigned to it.
- When this field is non-zero, only icon #0 can be used.
  - — Hardware icon #0 can have up to eight memory maps.
  - — The other hardware icons #1:#3 must be disabled.
  - — The number in SR2E[2:1] points to the pair of two icon maps selected by SR2A[5], but in this case, all maps go to icon #0 for display.
  - — In this order of significance, SR2E[2:1] and SR2A[5] select the eight memory maps for icon #0.

0 **Hardware Cursor Fine Horizontal Position [3]:**
This bit is the most-significant bit of a 4-bit word that is used with 10-dot fonts (character clocks), when in horizontally expanded graphics modes.
- The least-significant bits [2:0] are in Sequencer register SRX[7:5].
- When Extension register SR12[3] is 0, the CPU can modify the hardware cursor horizontal position.
- In non-expanded graphics modes, this bit is always 0.
- The coarse horizontal position is in Extension register SR10.

NOTE: When enabling a horizontal expansion from 640 to 800, the hardware cursor must be positioned within 10 dots.

12.32 SR2F: Half-Frame-Accelerator FIFO Threshold

I/O Port Address: 3C5

Index:2F

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Half-Frame Accelerator FIFO Threshold [3]	0
2	Half-Frame Accelerator FIFO Threshold [2]	0
1	Half-Frame Accelerator FIFO Threshold [1]	0
0	Half-Frame Accelerator FIFO Threshold [0]	0

NOTE: These register bits affect only dual-scan panels.

Bit	Description
7:4	**Reserved**
3:0	**Half-Frame Accelerator FIFO Threshold [3:0]:** The half-frame accelerator FIFO is 16 data stages deep and 32 bits wide. Before a new request can be made for a refill of the half-frame-accelerator read FIFO, SRF[3:0] controls how many 32-bit data stages are empty in the half-frame-accelerator read FIFO. (At the same time that the half-frame-accelerator read FIFO is emptied, it is refilled.) **NOTE:** A color LCD has a higher FIFO threshold than a monochrome LCD. (To minimize CRT-FIFO latency, in 16-bit and 24-bit per pixel modes, program a low threshold of 3h for a monochrome LCD. Program 6h for a dual-scan color STN LCD.) Example: If SR2F[3:0] = 4, after only four half-frame-accelerator FIFO stages are empty, a new request, programmed in hex, is made for new half-frame-accelerator cycles. For this example, program a FIFO threshold that is: • Low (2h to 4h) for 2 to 4 data stages for dual-scan monochrome STN panels. • Higher (4h to 7h) for 4 to 7 data stages for dual-scan color STN panels. • Less than Ah for all other cases.

12.33 GR9: Offset Register 0

I/O Port Address: 3CF

Index:9

Bit	Description	Reset Stat e
7	Offset 0 [7]	0
6	Offset 0 [6]	0
5	Offset 0 [5]	0
4	Offset 0 [4]	0
3	Offset 0 [3]	0
2	Offset 0 [2]	0
1	Offset 0 [1]	0
0	Offset 0 [0]	0

This register is used to access up to 2 Mbytes of display memory with up to 16-Kbyte granularity.

Bit **Descriptio n**

7:0 **Offset Register 0 [7:0] :**

- This Offset register is used when one of the following conditions is true:
  - — GRB[0] is 0
  - — GRB[0] is 1 *and* CPU address bit A[15] is 0
- When one of the above conditions is true *and* GRB[5] is 0:
  - — The register's offset value is added to the contents of XA (bus addresses A[19:12]) to provide XMA, an address into display memory.
  - — Access is for 1 Mbyte of display memory with 4-Kbyte granularity.
- When one of the above conditions is true *and* GRB[5] is 1:
  - — The register's offset value is added to the contents of XA (bus addresses A[20:14]) to provide XMA, an address into display memory.
  - — Access is for up to 2 Mbytes of display memory with 16-Kbyte granularity.

XMA. XMA is the display memory address, prior to modification by address wrap controls.

XMA = (Bus Address XA) + (value from Offset register GR9 or GRA).

XA. XA is the address on the bus, with bits [16] and [15] possibly forced to a 0 as indicated in the following table.

12.33 GR9: Offset Register 0 *(cont.)*

Bit **Descriptio n**

7:0 *(cont.)* **Offset Register 0 [7:0]** *(cont.)*:

Configuratio n		Bus Address X A		
If Display Memory is :	**And Register Setting :**	**[16]**	**[15]**	**[14:0]**
128 Kbytes	GR6[3:2] is 00	A[16]	A[15]	A[14:0]
64 Kbytes	GR6[3:2] is 01 *and* GRB[0] is 0 (Offset 1 disabled)	0	A[15]	A[14:0]
64 Kbytes	GR6[3:2] is 01 *or* GRB[0] is 1 (Offset 1 enabled)	0	0	A[14:0]

The XA bus address is summed with the contents of an Offset register with one of three relative alignments, according to the configuration indicated in the three tables that follow:

Bus Address (XA)	0	0	0	XA[16]	XA[15]	A[14]	A[13]	A[12]
+ Offset Value	Offset[7]	Offset[6]	Offset[5]	Offset[4]	Offset[3]	Offset[2]	Offset[1]	Offset[0]
= Display Memory Address (XMA)	XMA[19]	XMA[18]	XMA[17]	XMA[16]	XMA[15]	XMA[14]	XMA[13]	XMA[12]

Bus Address	0	0	0	0	XA[16]	XA[15]	A[14]	A[13]	A[12]
+ Offset Value	Offset[6]	Offset[5]	Offset[4]	Offset[3]	Offset[2]	Offset[1]	Offset[0]	0	0
= Display Memory Address	XMA[20]	XMA[19]	XMA[18]	XMA[17]	XMA[16]	XMA[15]	XMA[14]	XMA[13]	XMA[12]

Bus Address	LA[20]	LA[19]	LA[18]	LA[17]	A[16]	A[15]	A[14]	A[13]	A[12]
+ Offset Value	Offset[6]	Offset[5]	Offset[4]	Offset[3]	Offset[2]	Offset[1]	Offset[0]	0	0
= Display Memory Address	XMA[20]	XMA[19]	XMA[18]	XMA[17]	XMA[16]	XMA[15]	XMA[14]	XMA[13]	XMA[12]

12.34 GRA: Offset Register 1

I/O Port Address: 3CF

Index: A

Bit	Description	Reset State
7	Offset 1 [7]	0
6	Offset 1 [6]	0
5	Offset 1 [5]	0
4	Offset 1 [4]	0
3	Offset 1 [3]	0
2	Offset 1 [2]	0
1	Offset 1 [1]	0
0	Offset 1 [0]	0

This register is used to provide access for up to 2 Mbytes of display memory with 16-Kbyte granularity.

Bit	Description
7:0	**Offset 1 [7:0] :** • When Extension register GRB[0] is 0, this register is disabled. • When Extension register GRB[0] is 1 *and*: — CPU bus address bit A[15] is 1, the contents of GRA[7:0] are added to the contents of CPU bus address bits A[19:12] to provide access to up to 1 Mbyte of address into display memory, with 4-Kbyte granularity. — GRB[5] is 1, the contents of GRA[6:0] are added to the contents of CPU bus address bits A[20:14] to provide access to up to 2 Mbytes of address into display memory, with 16-Kbyte granularity.

12.35 GRB: Graphics Controller Mode Extensions Register

I/O Port Address: 3CF

Index: B

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Offset Granularity	0
4	16-Bit Pixel Enhanced Write Enable	0
3	8-Byte-Wide Display Memory Data Latches Enable	0
2	Extended Write Modes Enable	0
1	By-8 Addressing Enable	0
0	Offset Register 1 Enable	0

This register is used to enable or disable extended write modes which provide enhanced performance.

Bit	Description
7:6	**Reserved**
5	**Offset Granularity :** When this bit is programmed to 1, Extension registers GR9 and GRA are redefined as containing CPU bus address bits A[6:0]. In this case: • These GRB bits are added to CPU bus address bits A[20:14] to provide access to 2 Mbytes of display memory with 16-Kbyte granularity. • Extension register SR7[4] (the least-significant bit of a 1-Mbyte address page) becomes a 'don't care'. • Linear address memory mapping becomes 2 Mbytes on any 2-Mbyte boundary.
4	**16-Bit Pixel Enhanced Write Enable :** GRB[2] must be 1 in order to enable this bit. When both GRB[2] and GRB[4] are programmed to 1, the CL-GD7541/GD7543 executes the following enhanced write modes when Extended Write modes 4 and 5 are enabled and executed: • **By-16 Addressing Enabled :** The system address is shifted by 4, relative to true packed-pixel addressing, so that each system byte address points to a different 8-pixel (16-byte) block in display memory. • **16-Byte Transfer Enabled :** Up to 16 bytes (8 pixels) can be written into display memory for each CPU byte transfer. • **Extension Registers GR10 and GR11 Enabled :** GR10 and GR11 are enabled as foreground and background color extensions. • **Sequencer Register SR2 Doubling Enabled :** Each bit of SR2 is used as a pixel write mask for two bytes (one pixel).

12.35 GRB: Graphics Controller Mode Extensions Register *(cont.)*

Bit	Description
3	**8-Byte-Wide Display Memory Data Latches Enable :** When this bit is 1, display memory data latches are 8 bytes wide rather than the normal 4 bytes.
2	**Extended Write Modes Enable :** When this bit is 1, the CL-GD7541/GD7543 enables and executes the following extended write modes: • Graphics Controller register GR5[2] is enabled. As a result, Extended Write modes 4 and 5 can be enabled. • Graphics Controller register GR0 is extended from 4 bits to 8 bits. • Graphics Controller register GR1 is extended from 4 bits to 8 bits. • Sequencer register SR2 is extended from 4 bits to 8 bits. • GRB[4] is enabled. As a result, enhanced writes for 16-bit pixels can be enabled. • 8-Byte Transfer Enabled: — When GRB[2] is 1, up to 8 bytes (8 pixels) can be written into display memory for each CPU byte transferred. — When GRB[2] is 1 *and* GRB[4] is 1, up to 16 bytes can be written into display memory for color expansion.
1	**By-8 Addressing Enable :** • When this bit is 1, the system address is shifted by 3, relative to true packed-pixel addressing, so that each system byte address points to a different 8-pixel (8-byte) block in display memory. • When GRB[4] is 1, this bit is a 'don't care'.
0	**Offset Register 1 Enable :** • When this bit is programmed to 1, the value in system address [15] is used to choose between Offset register 0 and Offset register 1. • When this bit is programmed to 0, the value in system address [15] is ignored, and Offset register 0 is always chosen. • This bit must always be programmed to a 0 for 1 Mbyte of linear addressing.

12.36 GRC: Color Key Compare Registe r

I/O Port Address: 3CF

Index: C

Bit	Description	Reset Stat e
7	Color Key Compare [7]	1
6	Color Key Compare [6]	1
5	Color Key Compare [5]	1
4	Color Key Compare [4]	1
3	Color Key Compare [3]	1
2	Color Key Compare [2]	1
1	Color Key Compare [1]	1
0	Color Key Compare [0]	1

This register contains an 8-bit value that is compared to video data. For more information, refer to application note “8-Bit Dynamic Video Overlay” in the *CL-GD754X Application Boo k*.

Bit	Descripti on
7:0	**Color Key Compare [7:0] :** This register contains an 8-bit value that is compared to the video data. When Mode Switching 10 or 11 is chosen, a match between this value in GRC[7:0] and the video data value causes the video data pixel to be replaced with data from the Feature Connector.

12.37 GRD: Color Key Compare Mask Registe r

I/O Port Address: 3CF

Index: D

Bit	Description	Reset Stat e
7	Color Key Compare Mask [7]	0
6	Color Key Compare Mask [6]	0
5	Color Key Compare Mask [5]	0
4	Color Key Compare Mask [4]	0
3	Color Key Compare Mask [3]	0
2	Color Key Compare Mask [2]	0
1	Color Key Compare Mask [1]	0
0	Color Key Compare Mask [0]	0

This register contains an 8-bit mask under which the color key comparison of GRC is made. For more information, refer to application note “8-Bit Dynamic Video Overlay” in the *CL-GD754X Application Boo k*.

Bit	Descriptio n
7:0	**Color Key Compare Mask [7:0] :** A bit value of 1 for a GRD bit causes the corresponding video data bit to be masked out and *not* participate in the color comparison.

12.38 GRE: PCI Burst-Write and Gree n PC Control Registe r

I/O Port Address: 3CF

Index: E

Bit	Description	Reset Stat e
7	Reserved	
6	Reserved	
5	Reserved	
4	PCI Burst-Write Mode Enable	0
3	PCI Extensive Burst-Write Mode Enable	0
2	Display Power Management Signaling (Green PC) Control [1]	0
1	Display Power Management Signaling (Green PC) Control [0]	0
0	DCLK Output Divided By Two	0

This register contains miscellaneous control bits.

Bit — **Descriptio n**

7:5 — **Reserve d**

4 — **PCI Burst-Write Mode Enable :**

- When the PCI bus is selected (SR22[7] is 1 or SR22[0] is 1), *and* this bit is 1, the CPU can execute burst writes during vertical non-display time.
- When the system BitBLT (bit block transfer) is enabled, the CL-GD7541/GD7543 automatically disables this burst-write function.
- The CL-GD7541/GD7543 does not support PCI burst-read cycles.

3 — **PCI Extensive Burst-Write Mode Enable :**
When the PCI bus is selected (SR22[7] is 1 or SR22[0] is 1), *and* this bit is 1, the CPU can execute burst writes anytime during a frame.

2:1 — **Display Power Management Signaling (Green PC) Control [1:0] :**
These two bits control the CRT monitor power as specified in the DPMS (Display Power Management Signaling) specification, as shown in the following table:

GRE [2]	GRE [1]	CRT Monitor Power Mode	VSYNC Activity	HSYNC Activity	DAC Power	CL-GD7541/GD754 3 Power Management Mode
0	0	On	Pulsing	Pulsing	On	Active
0	1	Standby	Pulsing	Static at MISC[6] inactive level	Off	Active, Standby, or Suspend
1	0	Suspend	Static at MISC[7] inactive level	Pulsing	Off	Active, Standby, or Suspend
1	1	Off	Static at MISC[7] inactive level	Static at MISC[6] inactive level	Off	Active, Standby, or Suspend

12.38 GRE: PCI-Burst and Green-PC Control Register *(cont.)*

Bit	Descriptio n
2:1(*cont.*)	**Display Power Management Signaling (Green PC) Control [1:0]** *(cont.)*: Because DPMS CRT power-management modes are not related to the CL-GD7541/GD7543 controller power-management modes, they can be independently programmed, except for the following restrictions: • Prior to placing the CL-GD7541/GD7543 in Suspend mode, the BIOS can program any DPMS power-saving mode for the CRT. — The 32-kHz input to the CL-GD7541/GD7543 is used to provide any synchronization pulse required by the DPMS. • Because the CL-GD7541/GD7543 Standby mode is timer-driven (that is, hardware-controlled), as a result, — The DPMS STANDBY signal is forced by the hardware. — Software control is not allowed. • When the CL-GD7541/GD7543 is in LCD-only mode, the BIOS must set GRE[2:1] to 11 to power off any CRT that may be connected to the notebook computer. • The inactive static VSYNC and HSYNC signal levels are determined by the polarity selection in External/General register MISC[7:6]. — When MISC[7] is 1, the inactive level is low for the VSYNC signal. — When MISC[6] is 1, the inactive level is low for the HSYNC signal.
0	**DCLK Output, Divided By Two :** When this bit is: • 0, the CL-GD7541/GD7543 operates normally. • 1, the CL-GD7541/GD7543 emulates external DAC clocking mode 1. — The DCLK rising edge can be used to clock a 16-bit data pixel low byte. — The DCLK falling edge can be used to clock a 16-bit data pixel high byte. — The option of setting this bit to 1: — Works only for the CRT-only mode. — Does not work for the LCD or SimulSCAN mode. When this bit is 1, the clock to the LCD section is divided by two, which prevents the LCD from working properly.

12.39 GR10: 16-Bit Pixel Background Color Hig h Register

I/O Port Address: 3CF

Index: 10

Bit	Description	Reset State
7	Background Color [15]	0
6	Background Color [14]	0
5	Background Color [13]	0
4	Background Color [12]	0
3	Background Color [11]	0
2	Background Color [10]	0
1	Background Color [9]	0
0	Background Color [8]	0

This register contains the most-significant 8 bits of the 16-bit background color field for Extended Write mode 5.

Bit	Descriptio n
7:0	**Background Color [15:8] :** • The contents of this register are the most-significant 8 bits of the 16-bit background color for Extended Write mode 5. — These bits are sent to display memory map planes 1 and 3. • The contents of Graphics Controller register GR0 are the least-significant 8 bits of the background color for Extended Write mode 5. — The GR0 register bits are sent to display memory map planes 0 and 2.

12.40 GR11: 16-Bit Pixel Foreground Color Hig h Register

I/O Port Address: 3CF

Index: 11

Bit	Description	Reset State
7	Foreground Color [15]	0
6	Foreground Color [14]	0
5	Foreground Color [13]	0
4	Foreground Color [12]	0
3	Foreground Color [11]	0
2	Foreground Color [10]	0
1	Foreground Color [9]	0
0	Foreground Color [8]	0

This register contains the most-significant 8 bits of the 16-bit foreground color field for Extended Write modes 5 and 4.

Bit	Descriptio n
7:0	**Foreground Color [15:8] :** • The contents of this register are the most-significant 8 bits of the 16-bit foreground color for Extended Write modes 5 and 4. — These bits are sent to display memory map planes 1 and 3. • The contents of Graphics Controller register GR1 are the least-significant 8 bits of the foreground color for Extended Write modes 5 and 4. — The GR1 register bits are sent to display memory map planes 0 and 2.

12.41 GR20: BitBLT Width Low Register

I/O Port Address: 3CF

Index: 20

Bit	Description	Reset State
7	BitBLT Width [7]	0
6	BitBLT Width [6]	0
5	BitBLT Width [5]	0
4	BitBLT Width [4]	0
3	BitBLT Width [3]	0
2	BitBLT Width [2]	0
1	BitBLT Width [1]	0
0	BitBLT Width [0]	0

This register contains the least-significant 8 bits of the 11-bit BitBLT (bit block transfer) width field.

Bit	Description
7:0	**BitBLT Width [7:0]:** • These bits are the least-significant 8 bits of the BitBLT width field. • For details, refer to Extension register GR21, which contains the most-significant 3 bits.

12.42 GR21: BitBLT Width High Register

I/O Port Address: 3CF

Index: 21

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	BitBLT Width [10]	0
1	BitBLT Width [9]	0
0	BitBLT Width [8]	0

This register contains the most-significant 3 bits of the 11-bit BitBLT width field. For more information on the BitBLT, refer to Appendix A.

Bit	Description
7:3	**Reserved**
2:0	**BitBLT Width [10:8]:** • These bits are the most-significant 3 bits of the 11-bit value specifying the width-1, in bytes, of the areas involved in a BitBLT. • The least-significant bits are in Extension register GR20.

12.43 GR22: BitBLT Height Low Register

I/O Port Address: 3CF

Index: 22

Bit	Description	Reset State
7	BitBLT Height [7]	0
6	BitBLT Height [6]	0
5	BitBLT Height [5]	0
4	BitBLT Height [4]	0
3	BitBLT Height [3]	0
2	BitBLT Height [2]	0
1	BitBLT Height [1]	0
0	BitBLT Height [0]	0

This register contains the least-significant 8 bits of the 10-bit BitBLT height field.

Bit	Description
7:0	**BitBLT Height [7:0]:** • These bits are the least-significant 8 bits of the BitBLT height field. • For details, refer to Extension register GR23, which contains the most-significant 2 bits.

12.44 GR23: BitBLT Height High Register

I/O Port Address: 3CF

Index: 23

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	Reserved	
1	BitBLT Height [9]	0
0	BitBLT Height [8]	0

This register contains the most-significant 2 bits of the 10-bit BitBLT height field. For more information on the BitBLT, refer to Appendix A.

Bit	Description
7:2	**Reserved**
1:0	**BitBLT Height [9:8]:** • These bits are the most-significant 2 bits of the 10-bit value specifying the height-1, in scanlines, of the areas involved in a BitBLT. • The least-significant bits are in Extension register GR22.

12.45 GR24: BitBLT Destination Pitch Low Register

I/O Port Address: 3CF

Index: 24

Bit	Description	Reset State
7	BitBLT Destination Pitch [7]	0
6	BitBLT Destination Pitch [6]	0
5	BitBLT Destination Pitch [5]	0
4	BitBLT Destination Pitch [4]	0
3	BitBLT Destination Pitch [3]	0
2	BitBLT Destination Pitch [2]	0
1	BitBLT Destination Pitch [1]	0
0	BitBLT Destination Pitch [0]	0

This register contains the least-significant 8 bits of the 12-bit BitBLT destination pitch field.

Bit	Description
7:0	**BitBLT Destination Pitch [7:0]:** • These bits are the least-significant 8 bits of the BitBLT destination pitch field. • For details, refer to Extension register GR25, which contains the most-significant 4 bits.

12.46 GR25: BitBLT Destination Pitch High Register

I/O Port Address: 3CF

Index: 25

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	BitBLT Destination Pitch [11]	0
2	BitBLT Destination Pitch [10]	0
1	BitBLT Destination Pitch [9]	0
0	BitBLT Destination Pitch [8]	0

This register contains the most-significant 4 bits of the 12-bit BitBLT destination pitch field. For more information on the BitBLT, refer to Appendix A.

Bit	Description
7:4	**Reserved**
3:0	**BitBLT Destination Pitch [11:8]:** • These bits are the most-significant 4 bits of the 12-bit value specifying the destination pitch (that is, the scanline-to-scanline byte address offset) of the areas involved in a BitBLT. • The least-significant bits are in Extension register GR24.

12.47 GR26: BitBLT Source Pitch Low Register

I/O Port Address: 3CF

Index: 26

Bit	Description	Reset State
7	BitBLT Source Pitch [7]	0
6	BitBLT Source Pitch [6]	0
5	BitBLT Source Pitch [5]	0
4	BitBLT Source Pitch [4]	0
3	BitBLT Source Pitch [3]	0
2	BitBLT Source Pitch [2]	0
1	BitBLT Source Pitch [1]	0
0	BitBLT Source Pitch [0]	0

This register contains the least-significant 8 bits of the 12-bit BitBLT source pitch field.

Bit	Descriptio n
7:0	**BitBLT Source Pitch [7:0]:** • These bits are the least-significant 8 bits of the BitBLT source pitch field. • For details, refer to Extension register GR27, which contains the most-significant 4 bits.

12.48 GR27: BitBLT Source Pitch High Register

I/O Port Address: 3CF

Index: 27

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	BitBLT Source Pitch [11]	0
2	BitBLT Source Pitch [10]	0
1	BitBLT Source Pitch [9]	0
0	BitBLT Source Pitch [8]	0

This register contains the most-significant 4 bits of the 12-bit BitBLT source pitch field. For more information on the BitBLT, refer to Appendix A.

Bit	Description
7:4	**Reserved**
3:0	**BitBLT Source Pitch [11:8]:** • These bits are the most-significant 4 bits of the 12-bit value specifying the source pitch (that is, the scanline-to-scanline byte address offset) of the areas involved in a BitBLT. • The least-significant bits are in Extension register GR26.

12.49 GR28: BitBLT Destination Start Low Registe r

I/O Port Address: 3CF

Index: 28

Bit	Description	Reset State
7	BitBLT Destination Start [7]	0
6	BitBLT Destination Start [6]	0
5	BitBLT Destination Start [5]	0
4	BitBLT Destination Start [4]	0
3	BitBLT Destination Start [3]	0
2	BitBLT Destination Start [2]	0
1	BitBLT Destination Start [1]	0
0	BitBLT Destination Start [0]	0

This register contains the least-significant 8 bits of the 21-bit BitBLT destination start field.

Bit	Descriptio n
7:0	**BitBLT Destination Start [7:0]:** • These bits are the least-significant 8 bits of the BitBLT destination start field. • The other bits of this field are in Extension registers GR29 and GR2A • For details on this field, refer to Extension register GR2A

12.50 GR29: BitBLT Destination Start Mid Register

I/O Port Address: 3CF

Index: 29

Bit	Description	Reset State
7	BitBLT Destination Start [15]	0
6	BitBLT Destination Start [14]	0
5	BitBLT Destination Start [13]	0
4	BitBLT Destination Start [12]	0
3	BitBLT Destination Start [11]	0
2	BitBLT Destination Start [10]	0
1	BitBLT Destination Start [9]	0
0	BitBLT Destination Start [8]	0

This register contains the middle 8 bits of the 21-bit BitBLT destination start field.

Bit	Description
7:0	**BitBLT Destination Start [15:8]:** • These bits are the middle 8 bits of the BitBLT destination start field. • The other bits of this field are in Extension registers GR28 and GR2A. • For details on this field, refer to Extension register GR2A.

12.51 GR2A: BitBLT Destination Start High Register

I/O Port Address: 3CF

Index: 2A

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	BitBLT Destination Start [20]	0
3	BitBLT Destination Start [19]	0
2	BitBLT Destination Start [18]	0
1	BitBLT Destination Start [17]	0
0	BitBLT Destination Start [16]	0

This register contains the most-significant 5 bits of the 21-bit BitBLT destination start field. For more information on the BitBLT, refer to Appendix A.

Bit	Descriptio n
7:5	**Reserve d**
4:0	**BitBLT Destination Start [20:16]:** • These bits are the most-significant 5 bits of the 21-bit BitBLT destination start value that specifies the byte address of the beginning destination pixel for a BitBLT. • The other bits of this field are in Extension registers GR28 and GR29.

12.52 GR2C: BitBLT Source Start Low Register

I/O Port Address: 3CF

Index: 2C

Bit	Description	Reset State
7	BitBLT Source Start [7]	0
6	BitBLT Source Start [6]	0
5	BitBLT Source Start [5]	0
4	BitBLT Source Start [4]	0
3	BitBLT Source Start [3]	0
2	BitBLT Source Start [2]	0
1	BitBLT Source Start [1]	0
0	BitBLT Source Start [0]	0

This register contains the least-significant 8 bits of the 21-bit BitBLT source start field.

Bit	Descriptio n
7:0	**BitBLT Source Start [7:0]:** • These bits are the least-significant 8 bits of the BitBLT source start field. • The other bits of this field are in Extension registers GR2D and GR2E • For details on this field, refer to Extension register GR2E

12.53 GR2D: BitBLT Source Start Mid Register

I/O Port Address: 3CF

Index: 2D

Bit	Description	Reset State
7	BitBLT Source Start [15]	0
6	BitBLT Source Start [14]	0
5	BitBLT Source Start [13]	0
4	BitBLT Source Start [12]	0
3	BitBLT Source Start [11]	0
2	BitBLT Source Start [10]	0
1	BitBLT Source Start [9]	0
0	BitBLT Source Start [8]	0

This register contains the middle 8 bits of the 21-bit BitBLT source start field.

Bit	Descriptio n
7:0	**BitBLT Source Start [15:8]:** • These bits are the middle 8 bits of the BitBLT source start field. • The other bits of this field are in Extension registers GR2C and GR2E • For details on this field, refer to Extension register GR2E

12.54 GR2E: BitBLT Source Start High Register

I/O Port Address: 3CF

Index: 2E

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	BitBLT Source Start [20]	0
3	BitBLT Source Start [19]	0
2	BitBLT Source Start [18]	0
1	BitBLT Source Start [17]	0
0	BitBLT Source Start [16]	0

This register contains the most-significant 5 bits of the 21-bit BitBLT source start. For more information on the BitBLT, refer to Appendix A.

Bit	Description
7:5	**Reserved**
4:0	**BitBLT Source Start [20:16]:** • These bits are the most-significant 5 bits of the 21-bit BitBLT source start value that specifies the byte address of the beginning source pixel for a BitBLT. • The other bits of this field are in Extension registers GR2C and GR2D.

12.55 GR30: BitBLT Mode Register

I/O Port Address: 3CF

Index: 30

Bit	Description	Reset State
7	Color Expand Enable	0
6	8 × 8 Pattern Copy Enable	0
5	Reserved	
4	Color Expand / Transparency Width	0
3	Transparency Compare Enable	0
2	BitBLT Source Display Memory / System Memory	0
1	BitBLT Destination Display Memory / System Memory	0
0	BitBLT Direction	0

This register contains the bits that specify the BitBLT (bit block transfer) details, but not the BitBLT raster operation. For more information on the BitBLT, refer to Appendix A.

Bit **Description**

7 **Color Expand Enable :**

- When this bit is programmed to 1, the raster operation source is the expanded result from the bit-mapped source.
  - — The destination must be screen memory.
  - — The direction must be incremental.
  - — Raster operations are available for all block moves.
  - — Graphics Controller registers GR0 and GR1 and Extension registers GR10 and GR11 are used for bit-map color-expanded BitBLT operations.
  - — When the source data is expanded, the most-significant bit of the first source byte becomes the first pixel in the screen memory destination.
  - — For color-expanded BitBLTs (the source is system memory or display memory), each logical line must be an even byte.
    - — Source bytes must be completely used. As a result, when a logical line is not an even multiple of eight pixels, 'dummy' bits are used to fill it out to an even byte.
    - — 'Dummy' bits are ignored under control of the BitBLT width setting.
  - — When the source of color-expanded data is display memory, the source starting address must be on a 4-byte boundary, and the addressing is always linear. (The source pitch is ignored.)
  - — For information regarding color expansion, refer to Appendix D.
- When this bit is programmed to 0, the raster operation source is the pixel data read from the source.

12.55 GR30: BitBLT Mode Register *(cont.)*

Bit | **Description**

6 — **8 × 8 Pattern Copy Enable :**
When this bit is 1, the source pattern is copied repeatedly to the destination rectangular area.
- The pattern source must be aligned on a four-byte boundary.
- The pattern source is linear-addressed data in one of three arrangements as shown in the following table:

Operating Mode	Pattern Source Arrangement
Color Extension Enabled	8 bytes of monochrome bitmap for the 8 × 8 pattern
8-bit Pixels	64 bytes of color data for 64 pixels
16-bit Pixels	128 bytes of color data for 64 pixels

5 — **Reserved**

4 — **Color Expand / Transparency Width :**
- When GR30[7] is 1 *and* this bit is:
  - — 1, the bit-mapped source is expanded to 16 bits/pixel.
  - — 0, the bit-mapped source is expanded to 8 bits/pixel.
- When GR30[3] is 1 *and* this bit is:
  - — 1, the transparency compare is on 16-bit pixels.
  - — 0, the transparency compare is on 8-bit pixels.

3 — **Transparency Compare Enable :**
- When this bit is 1, then for each pixel, the result of the raster operation is compared to the transparent color in Extension registers GR34 and GR35.
  - — When the compare is a match, data bits are not written to the destination.
  - — When the color-expand BitBLT is to be used with an opaque foreground and a transparent background (similar to Extended Write mode 4), the transparency feature must be used, and the transparent color must be set to the background color.
- When this bit is 0, the data bits are written to the destination without regard to the contents of Extension registers GR34 and GR35.

12.55 GR30: BitBLT Mode Register *(cont.)*

Bit	Descripti on
2	**BitBLT Source Display Memory / System Memory :** • When this bit is 1, the BitBLT source is system memory. — The CPU performs the system bus transfers, but the CL-GD7541/GD7543 ignores the address provided with such transfers. — The CPU is required to transfer data in increments of four bytes. When the total number of bytes moved for a BitBLT is not a multiple of four, the CPU must write 'extra' bytes. — System memory-to-system memory BitBLTs are not allowed. • When this bit is 0, the BitBLT source is display memory. • When system-to-screen BitBLTs are being executed that: — Involve color expansion, Extension registers GR2C, GR2D, and GR2E must be cleared to 0. — Do not involve color expansion, 16-bit host transfers must be used, or the system becomes non-operative.
1	**BitBLT Destination Display Memory / System Memory:** • When this bit is 1, the BitBLT destination is system memory. — The CPU performs the system bus transfers, but the CL-GD7541/GD7543 ignores the address provided with such transfers. — The CPU is required to transfer data in increments of four bytes. When the total number of bytes moved for a BitBLT is not a multiple of four, the CPU must read 'extra' bytes. — System memory-to-system memory BitBLTs are not allowed. • When this bit is 0, the BitBLT destination is display memory. • When system-to-screen BitBLTs are being executed, 16-bit host transfers must be used, or the system becomes non-operative.
0	**BitBLT Direction :** When this bit is: • 1: — The source and destination addresses are decremented. — The BitBLT proceeds from higher addresses to lower addresses. — The starting address is the highest addressed byte in each area. • 0: — The source and destination addresses are incremented. — The BitBLT proceeds from lower addresses to higher addresses.

12.56 GR31: BitBLT Start/Status Register

I/O Port Address: 3CF

Index: 31

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	BitBLT Progress Status (Read Only)	0
2	BitBLT Reset	0
1	BitBLT Start / Suspend	0
0	BitBLT Status (Read Only)	0

This register contains the bit that begins a BitBLT and a bit that indicates whether the BitBLT has completed. For more information on the BitBLT, refer to Appendix A.

Bit	Description
7:4	**Reserved**
3	**BitBLT Progress Status (Read Only):** This bit is set to 1 at the start of a BitBLT. • When the BitBLT operation resets (refer to GR32[2]), this bit clears to 0. • When the BitBLT operation suspends (refer to GR31[1]), this bit remains a 1.
2	**BitBLT Reset:** • When this bit is set to 1: — The entire BitBLT engine is immediately reset and any operation in progress is terminated. The operation cannot be restarted. — GR31[3] clears to 0. • This bit must be cleared to 0 before any BitBLT operations are attempted.
1	**BitBLT Start / Suspend :** • When this bit is set to 1, the BitBLT starts with the next available display memory cycle. • GR31[0] must be monitored to determine when the BitBLT is complete. • This bit clears to 0 when the BitBLT completes. • When this bit is cleared to 0, the BitBLT suspends at the current scanline end. — When the BitBLT is suspended, the BitBLT Height registers reflect the line count for the last completed transfer. — When the BitBLT is suspended, GR31[3] remains a 1. — A suspended BitBLT may resume by setting this bit to 1.
0	**BitBLT Status (Read Only):** • When this bit is a 1, the BitBLT is in progress. • When this bit is a 0, the BitBLT is complete.

12.57 GR32: BitBLT Raster Operation (ROP) Register

I/O Port Address: 3CF

Index: 32

Bit	Description	Reset State
7	f Raster Operation Function [7]	0
6	f Raster Operation Function [6]	0
5	f Raster Operation Function [5]	0
4	f Raster Operation Function [4]	0
3	f Raster Operation Function [3]	0
2	f Raster Operation Function [2]	0
1	f Raster Operation Function [1]	0
0	f Raster Operation Function [0]	0

This register selects a raster operation function. For more information, refer to Appendix A.

Bit **Descriptio n**

7:0 **f Raster Operation Function [7:0] :**
This 8-bit value selects 1 of 16 possible two-operand raster operation (ROP) functions, as indicated in the table below:

Z (Logical Function: Algebraic Notation)	ROP No. (Hex)	Comparable Microsoft Name	Value Microsoft Uses to Get ROP
0	00	BLACKNESS	00000042
1	0E	WHITENESS	00FF0062
S	0D	SRCCOPY	00CC0020
D	06	–	00AA0029
~S	D0	NOTSRCCOPY	00330008
~D	0B	DSTINVERT	00550009
S.D	05	SRCAND	008800C6
S.~D	09	SRCERASE	00440328
~S.D	50	–	00220326
~S.~D	90	NOTSRCERASE	001100A6
S+D	6D	SRCPAINT	00EE0086
S+~D	AD	–	00DD0228
~S+D	D6	MERGEPAINT	00BB0226
~S+~D	DA	–	007700E6
S~ = D	59	SRCINVERT (xor)	00660046
S = D	95	- (xnor)	00990066

12.58 GR34: BitBLT Transparent Color Select Low Register

I/O Port Address: 3CF

Index: 34

Bit	Description	Reset State
7	BitBLT Transparent Color Select [7]	0
6	BitBLT Transparent Color Select [6]	0
5	BitBLT Transparent Color Select [5]	0
4	BitBLT Transparent Color Select [4]	0
3	BitBLT Transparent Color Select [3]	0
2	BitBLT Transparent Color Select [2]	0
1	BitBLT Transparent Color Select [1]	0
0	BitBLT Transparent Color Select [0]	0

This register contains the least-significant 8 bits of the 16-bit Transparent Color Select field.

Bit	Description
7:0	**BitBLT Transparent Color Select [7:0] :** • These bits are the least-significant 8 bits of the BitBLT Transparent Color Select field. • For details, refer to Extension register GR35, which contains the most-significant 8 bits.

12.59 GR35: BitBLT Transparent Color Select High Register

I/O Port Address: 3CF

Index: 35

Bit	Description	Reset State
7	BitBLT Transparent Color Select [15]	0
6	BitBLT Transparent Color Select [14]	0
5	BitBLT Transparent Color Select [13]	0
4	BitBLT Transparent Color Select [12]	0
3	BitBLT Transparent Color Select [11]	0
2	BitBLT Transparent Color Select [10]	0
1	BitBLT Transparent Color Select [9]	0
0	BitBLT Transparent Color Select [8]	0

This register contains the most-significant 8 bits of the 16-bit BitBLT Transparent Color Select field For more information on the BitBLT, refer to Appendix A.

Bit	Description
7:0	**BitBLT Transparent Color Select [15:8] :** • These bits are the most-significant 8 bits of the 16-bit BitBLT Transparent Color Select field. • The least-significant 8 bits are in Extension register GR34. • When Extension register GR30[3] is 1, the value of this field is compared with the value that results from the raster operation. If the values are equal, the value that results from the raster operation is not written to the destination. • For 8-bit color modes, the contents of this register must be set equal to those of Extension register GR34.

12.60 GR38: BitBLT Transparent Color Mask Low Register

I/O Port Address: 3CF

Index: 38

Bit	Description	Reset State
7	BitBLT Transparent Color Mask [7]	0
6	BitBLT Transparent Color Mask [6]	0
5	BitBLT Transparent Color Mask [5]	0
4	BitBLT Transparent Color Mask [4]	0
3	BitBLT Transparent Color Mask [3]	0
2	BitBLT Transparent Color Mask [2]	0
1	BitBLT Transparent Color Mask [1]	0
0	BitBLT Transparent Color Mask [0]	0

This register contains the least-significant 8 bits of the 16-bit BitBLT Transparent Color Mask field.

Bit	Description
7:0	**BitBLT Transparent Color Mask [7:0] :** • These bits are the least-significant 8 bits of the BitBLT Transparent Color Mask field. • For details, refer to Extension register GR39, which contains the most-significant 2 bits of this field.

12.61 GR39: BitBLT Transparent Color Mask High Register

I/O Port Address: 3CF

Index: 39

Bit	Description	Reset State
7	BitBLT Transparent Color Mask [15]	0
6	BitBLT Transparent Color Mask [14]	0
5	BitBLT Transparent Color Mask [13]	0
4	BitBLT Transparent Color Mask [12]	0
3	BitBLT Transparent Color Mask [11]	0
2	BitBLT Transparent Color Mask [10]	0
1	BitBLT Transparent Color Mask [9]	0
0	BitBLT Transparent Color Mask [8]	0

This register contains the most-significant 8 bits of the 16-bit BitBLT Transparent Color Mask field. For more information on the BitBLT, refer to Appendix A.

Bit	Description
7:0	**BitBLT Transparent Color Mask [15:8] :** • These bits are the most-significant 8 bits of the 16-bit BitBLT Transparent Color Mask field. • The least-significant 8 bits are in Extension register GR38. • When Extension register GR30[3] is 1, the value of the transparent color is compared with the value that results from the raster operation under this mask. If the values are equal, the value that results from the raster operation is not written to the destination. • For 8-bit color modes, the contents of this register must be set equal to those of register GR38. • A 1 in any bit location makes the corresponding compare a 'don't care'.

12.62 CR19: Interlace End Register

I/O Port Address: 3?5

Index: 19

Bit	Description	Reset State
7	Interlace End [7]	0
6	Interlace End [6]	0
5	Interlace End [5]	0
4	Interlace End [4]	0
3	Interlace End [3]	0
2	Interlace End [2]	0
1	Interlace End [1]	0
0	Interlace End [0]	0

This register contains the ending horizontal character count for the Odd Field VSYNC.

Bit	Description
7:0	**Interlace End :** • This value is the number of characters in the last scanline of the Odd Field in interlaced timing. • This value can be adjusted to center the scanlines in the Odd Field half-way between scanlines in the Even Field. • This register is typically programmed to approximately half the Horizontal Total.

NOTE: The '?' in the I/O port address of the registers in the next sections implies 'B' in Monochrome mode and 'D' in Color mode .

12.63 CR1A: Miscellaneous Control Register

I/O Port Address: 3?5

Index: 1A

Bit	Description	Reset State
7	Vertical Blanking End Extension [9]	0
6	Vertical Blanking End Extension [8]	0
5	Horizontal Blanking End Extension [7]	0
4	Horizontal Blanking End Extension [6]	0
3	DAC Mode Switching / Video Overlay Mode Control [1]	0
2	DAC Mode Switching / Video Overlay Mode Control [0]	0
1	Display Start Address Double Buffer Enable	0
0	Interlaced Timing Enable	0

This register contains timing extension bits as well as some miscellaneous control bits.

Bit	Descriptio n
7:6	**Vertical Blanking End Extension [9:8] :** This 2-bit field is used to extend the Vertical Blanking End value to 10 bits. • These bits are enabled only when CR1B[5] is 1 or when CR1B[7] is 1. • For more information on these bits, refer to CRT Controller register CR16.
5:4	**Horizontal Blanking End Extension [7:6] :** This 2-bit field is used to extend the Horizontal Blanking End value to 8 bits. • These bits are enabled only when CR1B[5] is 1 or when CR1B[7] is 1. • For more information on these bits, refer to CRT Controller register CR3[4:0].

12.63 CR1A: Miscellaneous Control Register *(cont.)*

Bit | **Description**

3:2 **DAC Mode Switching / Video Overlay Mode Control [1:0] :**
This field is used to select DAC Mode Switching and the Video Overlay mode, as summarized in the following table. For more information, refer to application note "8-Bit Dynamic Video Overlay" in the *CL-GD754X Application Book*.

CR1A [3]	CR1A [2]	DAC Mode Switching Enabled or Disabled	Video Overlay Mode Control
0	0	Disabled	No Video Overlay. (Normal VGA-compatible operation.)
0	1	Enabled	Video Overlay controlled with FCEVIDEO#[a]
1	0	Enabled	Video Overlay controlled with FCEVIDEO# and color key.
1	1	Enabled	Video Overlay controlled with color key only.

[a] FCEVIDEO# is typically generated by OVRW#. For more information, refer to application note "8-Bit Dynamic Video Overlay" in the *CL-GD754X Application Book*.

1 **Display Start Address Double Buffer Enable :**
When this bit is 1, the Display Start Address is updated on the VSYNC following a write to Start Address Low. This update provides control of display frame switching without the need to explicitly monitor VSYNC.

0 **Interlaced Timing Enable**:
When this bit is 1, it enables interlaced timing.
- In text mode, interlaced synchronization is enabled.
- In graphics mode:
  - — Both interlaced synchronization and video data are enabled.
  - — For both interlaced synchronization and video data, the CRTC Scanline Double bit (CR9[7]) must be 0.
  - — Graphics modes 4 and 6 must always be non-interlaced.
- When this bit is 1, IRQ requests are generated only at the end of odd fields, that is, at the end of a frame.

12.64 CR1B: Extended Display Controls Register

I/O Port Address: 3?5

Index: 1B

Bit	Description	Reset State
7	Horizontal and Vertical Blanking End Extension Enable	0
6	Text Mode Fast-Page Enable	0
5	Blanking Control	0
4	Offset Register Extension [8]	0
3	Screen A Start Address [18]	0
2	Screen A Start Address [17]	0
1	Extended Address Wrap Enable	0
0	Screen A Start Address [16]	0

This register contains miscellaneous bits that control extended display functions.

Bit **Descriptio n**

7 **Horizontal and Vertical Blanking End Extension Enabl e**:
When this bit is:
- 0, *and* CR1B[5] is 0, the Horizontal and Vertical Blanking End Extension bits of CR1A[7:6] and CR1A[5:4] are disabled.
- 1, the Horizontal and Vertical Blanking End Extension bits of CR1A[7:6] and CR1A[5:4] are enabled, regardless of the CR1B[5] level.

6 **Text Mode Fast-Page Enabl e**:
When this bit is:
- 0, all font fetch cycles take place as random-read cycles. This bit must be 0 for standard VGA dual-font operation.
- 1, fast-page-mode cycles are used to fetch font data. This setting allows for text modes with a VCLK greater than 30 MHz, as is required for 132-column modes.

5 **Blanking Control :**
- When this bit is 0 (the standard VGA mode):
  - — The blanking signal generated by the CRTC controls the DAC blanking.
  - — The border can be used. (For more information, refer to Attribute Controller register AR11.)
- When this bit is 1:
  - — The display enable controls the DAC blanking.
  - — The border cannot be used, as the blanking registers are no longer available to control the border. Instead, the blanking registers are used to generate the OVRW# signal.
  - — The DAC is blanked during the time the border is normally displayed.
  - — The OVRW# pin is an output and follows the blanking signal generated by the CRTC.
  - — The Horizontal and Vertical Blanking End Extension bits in CR1A[7:4] are enabled and used to specify the active portion of the Video Overlay Window. For more information, refer to application note "The 8-Bit Dynamic Video Overlay" in the *CL-GD754X Application Boo k*.

12.64 CR1B: Extended Display Controls Register *(cont.)*

Bit	Description
4	**Offset Register Extension [8] :** This bit is the most-significant ninth bit of the CRT Controller Offset field. For details on this field, refer to CRT Controller register CR13.
3:2	**Screen A Start Address [18:17] :** These bits are the most-significant 2 bits of the CTR Controller Screen A Start Address registers CRC and CRD. Bit 16 is in CR1B[0].
1	**Extended Address Wrap Enable :** • When this bit is 0, VGA compatibility is offered as follows: — The CRTC Character Address Counter is 16 bits wide. — The display memory address wraps at 64K maps (for 256K total memory). • When this bit is 1: — The CL-GD7541/GD7543 CRT character counter addresses CA[16] and CA[18] provide up to 256K bytes in each bit plane, or one Mbyte of packed-pixel memory. — The CL-GD7541/GD7543 CRT controller address counter is 19 bits wide. — The display memory address wraps at the total available memory size. — *and* Chain-4 addressing is selected (Sequencer register SR4[3] is 1): — DRAM addresses MA[0] and MA[1] are supplied from addresses XMA[16] and XMA[17]. — The other DRAM addresses are supplied from addresses XMA[18:12]. These addresses result from the sum of bus addresses XA[16:12] and the contents of either Graphics Controller Offset register 0 (GR9) or Offset register 1 (GRA). — *and* CRTC Double-Word addressing is selected (CRT Controller register CR14[6] is 1): — DRAM addresses MA[0] and MA[1] are supplied from the internal CL-GD7541/GD7543 CRT address counter addresses CR[15:14]. (The other DRAM addresses are supplied from addresses XMA[18:12], in the same manner as Chain-4 addressing.) — This action provides four displayable pages in Graphics mode 13h.
0	**Screen A Start Address [16] :** This is bit 16 of the Screen A Start Address. Bits 17 and 18 are in CR1B[3:2]. For more information, refer to CRT Controller Screen A Start Address registers CRC and CRD.

12.65 CR1D: Video Overlay Mode Registe r

I/O Port Address: 3?5

Index: 1D

Bit	Description	Reset State
7	Reserved	
6	Video Overlay Timing Signal Source	0
5	Reserved	
4	Reserved	
3	Reserved	
2	DAC Mode Switching Control [1]	0
1	DAC Mode Switching Control [0]	0
0	Reserved	

This register contains controls for the extended Video Overlay modes.

Bit **Descriptio n**

7 **Reserve d**

6 **Video Overlay Timing Signal Source :**
- When this bit is 0, *and* Extension register CR1A[3:2] is 01, the FCEVIDEO# input is used as the timing signal for the Video Overlay modes.
- When this bit is 1, *and* Extension register CR1A[3:2] is 10, the internally generated OVRW# output is the timing signal for the Video Overlay modes. This setting eliminates the need to connect the OVRW# output to the FCEVIDEO# input

5:3 **Reserve d**

2:1 **DAC Mode Switching Control [1:0] :**
This field controls DAC mode switching. CR1A[3:2] selects the Video Overlay mode.

CR1D		DAC Mode Switch State and Result s		
[2]	[1]	DAC Mode Switch State	Result for Background :	Result for Video Overlay Window Mode:
0	0	True. Selected Extended DAC mode is enabled.	VGA data from display memory (typically Graphics mode 5Fh)	Live video (typically true color)
0	1	False. Selected Extended DAC mode is enabled.	Live video (typically true color)	VGA data from display memory (typically Graphics mode 5Fh)
1	X	Don't Care. Extended DAC mode is disabled.	–	–

0 **Reserve d**

12.66 CR1E: LCD Shading Register

I/O Port Address: 3?5

Index: 1E

Bit	Description	Access	Reset State
7(MSB)	Shade Mapping [1]	R/W	0
6	Shade Mapping [0]	R/W	0
5	Reverse Video for Text Modes	R/W	0
4	Reverse Video for Graphics Modes	R/W	0
3	Reserved		
2	Horizontal CRTC Registers Access Control Override	R/W	0
1	Text-Mode Contrast Enhancement	R/W	0
0(LSB)	Graphics Mode Dithering Enable	R/W	0

Bit **Description**

7:6 **Shade Mapping [1:0]:**
These 2 bits are used to program monochrome grayscale mapping (that is, shading) according to the following table:

CR1E [7]	CR1E [6]	Shade Map
0	0	Graphics mode. 18-bit output of LUT converted to 64 shades, with NTSC weighting.
0	1	Green gun output of LUT only. 6-bit output of Look-up Table converted to 64 shades.
1	0	Text mode. Direct display of up to 16 or 64 shades of pixel data (4-bit planar, or lower 6 of 8 bits packed-pixel)
1	1	Reserved

5 **Reverse Video for Text Modes:**
When this bit is:
- 0, this bit is disabled.
- 1, all text modes are displayed in reverse video.

4 **Reverse Video for Graphics Modes:**
When this bit is:
- 0, this bit is disabled.
- 1, all graphics modes are displayed in reverse video.

3 **Reserved**

12.66 CR1E: LCD Shadin g *(cont.)*

Bit | **Descriptio n**

2 — **Horizontal CRTC Registers Access Control Overrid e:**
If this bit is:
- 1, *or* the following conditions exist:
  — CR20[5] is 1 (the LCD panel interface is enabled)
  — R9X[3:2] is 01 (the LCD panel interface is set for 800 × 600 panel)
  — CR2E[5] is 1 (horizontal centering is on)
  then Extension registers RiY and RiZ (i = 0,2,3,4,5) – the horizontal timing shadow registers – are automatically used to control the CRT controller.
- 0, *or* not all of the above conditions occur as described, then horizontal timing CRT controller registers CR0, CR2, CR3, CR4, CR5 – the standard VGA horizontal timing registers – are automatically used to control the CRT controller.

1 — **Text-Mode Contrast Enhancement:**
This bit is used along with Extension register R8X[4] to enable text-mode contrast enhancement.

CR1E[1]	R8X[4]	Text-Mode Contrast- Enhancement Characteristic s
0	0	No enhancement of text mode.
0	1	Foreground-only enhancement If BG > FG, then BGC = BG and FGC = 0. If BG < FG, then BGC = BG and FGC = 1.
1	0	Contrast enhancement If BG > FG, then BGC = BG and FGC = 0. If BG < FG, then BGC = 0 and FGC = FG.

BG = Background, FG = Foreground, xxC = Color

0 — **Graphics Mode Dithering Enable:**
This bit is:
- 1 to enable dithering in graphics mode.
- 0 to disable dithering in non-packed pixel graphics mode.

12.67 CR1F: LCD Modulation Control Registe r

I/O Port Address: 3?5

Index: 1F

Bit	Description	Access	Reset Stat e
7(MSB)	External / Internal Modulation Control	R/W	0
6	MOD or Retrace LLCLK Control [6]	R/W	0
5	MOD or Retrace LLCLK Control [5]	R/W	0
4	MOD or Retrace LLCLK Control [4]	R/W	0
3	MOD or Retrace LLCLK Control [3]	R/W	0
2	MOD or Retrace LLCLK Control [2]	R/W	0
1	MOD or Retrace LLCLK Control [1]	R/W	0
0(LSB)	MOD or Retrace LLCLK Control [0]	R/W	0

This register is used for one of two purposes:

1) It controls the characteristics of the LCD Modulation (MOD) signal .

2) During vertical blanking, it generates extra line clocks (LLCLKs), which have two function s:

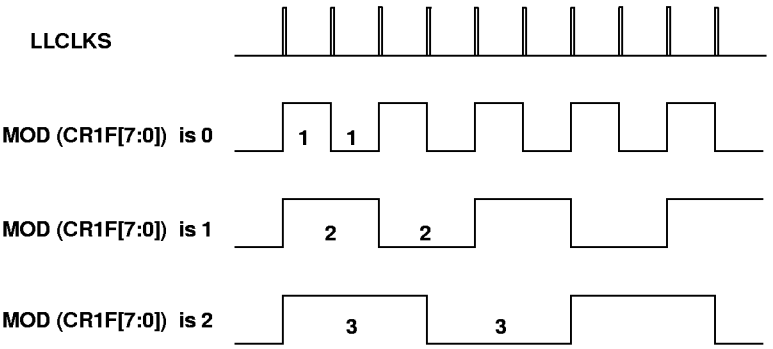
a) They eliminate any "waterfall motion" (that is, rolling lines appearing on the entire LCD).

b) They guarantee the LCD receives a specific number of LLCLKs per frame .

Bit	Descriptio n
7	**External or Internal Modulation Control:** This bit controls the source of the modulation (MOD) signal for the LCD. • Clear this bit to 0 when an LCD needs an externally supplied MOD signal. — In this case, CR1F[6:0] can be used to program from 1 to 128 scanlines before MOD changes polarity. — Program CR1F[6:0] to determine the half-period of the square-wave output on the MOD pin, based on the programmed number of LLCLKs

12.67 CR1F: LCD Modulation Control Registe r *(cont.)*

Bit	Description
7*(cont.)*	**External or Internal Modulation Control** *(cont.)*: • When CR1F[7] is 0, the resulting value of the MOD signal is one more than the value that is programmed into CR1F[7:0]. — For example, if register bits CR1F[7:0] are programmed to: — 0, the half-period of the square-wave MOD output is 1. — 1, the half-period of the square-wave MOD output is 2. — 2, the half-period of the square-wave MOD output is 3, and so on.



	• Set this bit to 1 when the LCD generates its own internal MOD signal and does not require an externally supplied MOD signal. (In addition, set CR1F[6:0] appropriately, as described below.)
6:0	**MOD or Retrace LCD Line Clock (LLCLK) Contro l [6:0]:** • When CR1F[7] is 0: — The contents of CR1F[6:0] can select up to 128 scanlines before the MOD signal changes polarity. • When CR1F[7] is 1: — For dual-scan LCDs, program CR1F[6:0] for only the number of LLCLKs that appear for each full frame. (Any extra clocks are seen on every other half-frame of the LCD during CRT vertical retrace.) — For single-scan LCDs, program CR1F[6:0] for the total number of LLCLKs for the entire frame of the LCD. — The contents of CR1F[6:0] are added to 180 hex (384 decimal) to determine the total number of LLCLKs. (The number 180 hex has beenpredetermined to allow a working range of LLCLKs.) — Total number of LLCLKs = 180h + [value in (CR1F[6:0])]

12.68 CR20: Power Management Register

I/O Port Address: 3?5

Index: 20

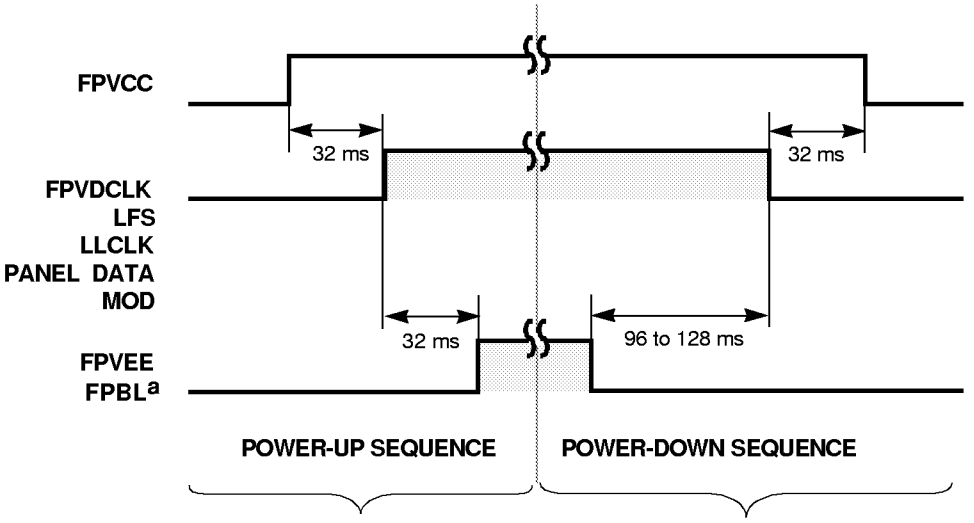
Bit	Description	Access	Reset State
7(MSB)	Suspend Mode Debounce Timer Resolution	R/W	0
6	CRT Enable	R/W	0
5	LCD Enable	R/W	0
4	Standby Mode Activate	R/W	0
3	Suspend Mode Activate	R/W	0
2	Display Memory Refresh Select [1]	R/W	0
1	Display Memory Refresh Select [0]	R/W	0
0(LSB)	Text Mode Shading Control	R/W	0

Bit	Description
7	**Suspend Mode Debounce Timer Resolution:** When this bit is: • 0, the Suspend mode debounce-timer resolution = 30 µsec (32-kHz period). • 1, the Suspend mode debounce-timer resolution = 1.0 sec.
6	**CRT Enable**: Setting this bit to 1 enables the analog CRT output from the video DAC.

12.68 CR20: Powe r Management Register *(cont.)*

Bit	Descriptio n
5	**LCD Enable:** To enable the LCD interface, set this bit to 1. • As shown in the following figure, when this bit has a transition that is: — Low to high, the CL-GD7541/GD7543 LCD power-up sequence occurs, which enables the following signals in the proper sequence: the FPVCC signal, the drive signals (FPVDCLK, LFS, LLCLK, Panel Data, and MOD), the logic supply signal (FPVEE), and the backlight signal (FPBL). — High to low, the CL-GD7541/GD7543 LCD power-down sequence occurs, which disables in the proper sequence the backlight signal (FPBL) and logic supply signal (FPVEE), the drive signals, and the FPVCC signal.

CL-GD7541/GD7543 Signals



[a] This timing diagram applies to FPBL only if FPBL is enabled.

Figure 1 2-1. Normal Power-Up/Power-Down Sequenc e

NOTES:

1) The LCD power-up sequence begins when any of the following occur :
   a) When the LCD is powered on and CR20[5] = 1
   b) When Standby or Suspend modes are terminated, and the LCD was on prior to entering the Standby or Suspend mod e
   c) When switching from CRT-only mode to an LCD or SimulSCAN mod e
2) The LCD power-down sequence begins when any of the following occur :
   a) When the LCD is powered off and CR20[5] = 0
   b) When Standby or Suspend modes are entered, and the LCD was previously o n
   c) When switching from an LCD or SimulSCAN mode to a CRT-only mod e

12.68 CR20: Power Management Register *(cont.)*

Bit **Description**

5 *(cont.)* **LCD Enable** *(cont.)*:

- When this bit is 1, the Line Frame Start (LFS) and LCD Line Clock (LLCLK) timing signals for monochrome LCDs are generated. These bits are generated from the Extension registers, R2X through RBX.
  - — For most TFT-color LCDs, the synchronization timing programmed by the CRT controller is used, in which case, specially compensated VSYNC and HSYNC signals are sent to the LFS and LLCLK outputs.
  - — In addition, the display enable signal controls the display data.
- When this bit is 1, some VGA register bits are redefined for LCDs as shown in the following table.

VGA-Defined Register Bits	New LCD Definition for Register Bits *When CR20[5] is 1*
AR13[3:0]	When Sequencer register SR1[0] is 0 (DCLK is divided by 8) and when pixel panning, the shift effect of Attribute Controller register AR13[3:0] is masked. As a result, a value of either 8h or 0h equals a 'no shift'.
MISC[7:6]	CRT synchronization polarity bits are redefined for External/General register MISC[7:6] so that 00 is an 800 × 600 LCD and 11 is a 640 × 480 LCD.
SR1[0]	This bit is locked to 0 so that it is 8 dots/character.
SR1[3]	Except for Graphics mode 13h, this bit selects the horizontally-locked timing for 40- or 80-column (character) modes.

NOTE: Clock select bits do not need to be locked. As required by the LCD, clock programming registers must be set for the same frequency.

4 **Standby Mode Activate:**
When this bit is:
- 0, the current internal Standby mode timer setting controls when the CL-GD7541/GD7543 is placed into Standby mode.
- 1, the current internal Standby mode timer setting is overridden, and immediately the CL-GD7541/GD7543 is placed into Standby mode.

3 **Suspend Mode Activate:**
This bit takes effect only when no hardware-controlled Suspend mode is in effect. When this bit is:
- 0, the input on the SUSPI pin controls when the CL-GD7541/GD7543 is placed into Suspend mode.
- 1, a software-controlled Suspend mode is initiated. As a result, the power-down sequence blanks the LCD screen.

12.68 CR20: Powe r Management Register *(cont.)*

Bit | **Descriptio n**

2:1 **Display Memory Refresh Select :**
The programming of these 2 bits control the type of refresh applied to the display memory during Suspend mode as follows.

CR20		Display Memory Refresh Typ e
[2]	[1]	
0	0	Refresh cycle 8 ms, CAS*-before-RAS*.
0	1	Refresh cycle 64-ms, CAS*-before-RAS*.
1	0	Self-refresh. RAS* and CAS* are driven low .
1	1	No refresh. All clock inputs are disabled. All outputs to display memory are high-impedance .

0 **Text Mode Shading Contro l**:
When this bit is:
- 0, text shades are derived directly from foreground/background data
- 1, text shades are derived the same way as graphics, with CR1E[7:6].

12.69 CR21: Power-Down Timer Control Registe r

I/O Port Address: 3?5

Index: 21

Bit	Description	Access	Reset Stat e
7(MSB)	Backlight Timer Control [3]	R/W	0
6	Backlight Timer Control [2]	R/W	0
5	Backlight Timer Control [1]	R/W	0
4	Backlight Timer Control [0]	R/W	0
3	Standby Mode Timer Control [3]	R/W	0
2	Standby Mode Timer Control [2]	R/W	0
1	Standby Mode Timer Control [1]	R/W	0
0(LSB)	Standby Mode Timer Control [0]	R/W	0

This register has two timers, and each controls the time at which power to the LCD is switched off.

- Programming CR21[7:4] controls the time it takes for the LCD backlight to switch off
- Programming CR21[3:0] controls the time it takes for the Standby mode to be entered and power to the LCD to be switched off.

The timers operate as follows.

- Both timers may be set for times from 1 to 15 minutes.
- A programmed value of zero disables the timer.
- Instead of 60 seconds, the timers use 64 seconds for each 'minute' programmed.
- The timers subtract a correcting factor of 32 seconds from the timed subtotal.
- For example, a setting of 15 minutes (Fh) results in:
  [(15 counts × 64 seconds) − 32 seconds] =
  [(960 seconds) − 32 seconds] =
  928 seconds, or an actual time of (928 ÷ 60) = 15.5 minutes.

For typical power-down timer settings, refer to the table shown on the following page.

Bit	Descriptio n
7:4	**Backlight Timer Control [3:0]:** These bits program the value for the internal flat panel backlight timer, FPBL
3:0	**Standby Mode Timer Contro l [3:0]:** These bits program the value for the internal Standby mode timer as shown in the table which follows.237

12.69 CR21: Power-Down Timer Control Register *(cont.)*

CR21 Backlight Timer Control Bit s				Hex Code	Actual Seconds Programmed for Delay Time (Seconds)	Approximate Corresponding Delay Time (Minutes)
[7]	[6]	[5]	[4]			
CR21 Standby Mode Timer Control Bit s						
[3]	[2]	[1]	[0]			
0	0	0	0	0h	Disabled	Disabled
0	0	0	1	1h	32	0.5
0	1	0	1	5h	288	4.8
0	1	1	1	7h	416	6.9
1	0	1	0	Ah	608	10.1
1	1	1	1	Fh	928	15.5

12.70 CR23: Suspend Mode Debounce Timer Register

I/O Port Address: 3?5

Index: 23

Bit	Description	Access	Reset State
7(MSB)	Suspend Mode Debounce Timer [3]	R/W	0
6	Suspend Mode Debounce Timer [2]	R/W	0
5	Suspend Mode Debounce Timer [1]	R/W	0
4	Suspend Mode Debounce Timer [0]	R/W	0
3	FPBL Control Override	R/W	0
2	FPBL Output State	R/W	0
1	FPVCC Control Override	R/W	0
0(LSB)	FPVCC Output State	R/W	0

Bit **Description**

7:4 **Suspend Mode Debounce Timer [3:0]:**
These bits define the number of seconds the input to the SUSPI pin must remain high and stable before the CL-GD7541/GD7543 enters Suspend mode.

- The SUSPI debounce timer may be set for 1 to 15 seconds or 30 to 450 µs.
- A setting of 0000 disables the SUSPI debounce timer.

CR23				CR20	
[3]	[2]	[1]	[0]	CR20[7] is 1: Resolution for SUSPI Debounce Timer = 1.0 second	CR20[7] is 0: Resolution for SUSPI Debounce Timer = 30 µs
0	0	0	0	0 (SUSPI debounce timer disabled)	
0	0	0	1	1 second	30 µs
0	0	1	0	2 seconds	60 µs
0	0	1	1	3 seconds	90 µs
0	1	0	0	4 seconds	120 µs
0	1	0	1	5 seconds	150 µs
0	1	1	0	6 seconds	180 µs
0	1	1	1	7 seconds	210 µs
1	0	0	0	8 seconds	240 µs
1	0	0	1	9 seconds	270 µs
1	0	1	0	10 seconds	300 µs
1	0	1	1	11 seconds	330 µs
1	1	0	0	12 seconds	360 µs
1	1	0	1	13 seconds	390 µs
1	1	1	0	14 seconds	420 µs
1	1	1	1	15 seconds	450 µs

12.70 CR23: Suspend Mode Debounce Timer Register *(cont.)*

Bit	Descriptio n
3	**FPBL Control Overrid e**: Setting this bit to 1: • Overrides the state of the flat panel backlight (FPBL) output pin. • Enables CR23[2] to directly control the output state of the flat panel backlight FPBL pin.
2	**FPBL Output State :** When CR23[3] is 1, *and* this bit is: • 0, the output state of the flat panel backlight FPBL pin is 0. • 1, the output state of the flat panel backlight FPBL pin is 1.
1	**FPVCC Control Overrid e**: Setting this bit to 1: • Overrides the state of the flat panel VCC (FPVCC) output pin. • Enables CR23[0] to directly control the output state of the flat panel VCC (FPVCC) pin. **CAUTION:** Setting this bit to 1 can cause excessive power consumption and damage the flat panel. It is strongly recommended that this bit be left in the 0 state.
0	**FPVCC Output State :** When CR23[1] is 1, *and* this bit is: • 0, the output state of the flat panel VCC (FPVCC) pin is 0. • 1, the output state of the flat panel VCC (FPVCC) pin is 1.

12.71 CR25: Manufacturing Revision ID Registe r

I/O Port Address: 3?5

Index: 25

Bit	Description	Reset State
7(MSB)	Manufacturing Revision ID [7]	'MFG revision'
6	Manufacturing Revision ID [6]	'MFG revision'
5	Manufacturing Revision ID [5]	'MFG revision'
4	Manufacturing Revision ID [4]	'MFG revision'
3	Manufacturing Revision ID [3]	'MFG revision'
2	Manufacturing Revision ID [2]	'MFG revision'
1	Manufacturing Revision ID [1]	'MFG revision'
0(LSB)	Manufacturing Revision ID [0]	'MFG revision'

This register contains the least-significant 8 bits of the 10-bit read-only Manufacturing Revision ID field.

Bit	Descriptio n
7:0	**Manufacturing Revision ID [7:0] :** • These bits are the least-significant 8 bits of the Manufacturing Revision ID field that uniquely identifies the CL-GD7541/GD7543 manufacturing revision level. • This read-only ID field is used for factory testing and internal tracking purposes only. Application programs must not use this field. • The most-significant 2 bits are in Extension register CR27[1:0].

12.72 CR27: Device ID and Manufacturing Revision ID Registe r

I/O Port Address: 3?5

Index: 27

Bit	Description	Reset State
7(MSB)	Device ID [5]	0
6	Device ID [4]	0
5	Device ID [3]	1
4	Device ID [2]	0
3	Device ID [1]	1
2	Device ID [0]	1
1	Manufacturing Revision ID [9]	'MFG revision'
0(LSB)	Manufacturing Revision ID [8]	'MFG revision'

This read-only register returns in bits [7:2] a value that uniquely identifies the CL-GD7541/GD7543.

Bit	Descriptio n
7:2	**Device ID [5:0] :** This 5-bit field contains a unique value that identifies the CL-GD7541/GD7543 as a Cirrus Logic product.
1:0	**Manufacturing Revision ID [9:8] :** • These bits are the most-significant 2 bits of the Manufacturing Revision ID field. • For details, refer to Extension register CR25[7:0], which contains the least-significant 8 bits of this field.

12.73 CR29: Configuration Status Registe r

I/O Port Address: 3?5

Index: 29

Bit	Description	Reset Stat e
7(MSB)	Suspend Mode Status	0
6	32-kHz Input Status	0
5	Power-Up/Power-Down Cycling Activity	0
4	Standby Mode Status	0
3	Reserved	
2	Reserved	
1	Reserved	
0(LSB)	Reserved	

This read-only register identifies the configuration of the memory and bus interface selected for the chip.

Bit	Descriptio n
7	**Suspend Mode Status:** • This bit is 1 when the CL-GD7541/GD7543 is in Suspend mode. This bit remains 1 from the time the clocks are stopped until 32 ms after the clocks are restarted, that is, until power-up sequencing is started. • While this bit is 1, the SUSPST# pin output remains low.
6	**32-kHz Input Status:** This bit reflects the status of the 32-kHz input clock. • This bit is 1 when the 32-kHz input clock signal is high. • This bit is 0 when the 32-KHz input clock signal is low. • This bit can be used to create a software timer.
5	**Power-Up/Power-Down Cycling Activity :** • This bit is 1 while the CL-GD7541/GD7543 is going through a power-up or power-down sequence. • This bit can be read in all modes except hardware-controlled Suspend mode, which locks out access to all registers.
4	**Standby Mode Status:** • This bit is 1 when the CL-GD7541/GD7543 is in Standby mode. This bit remains 1 from the time the clocks are stopped until 32 ms after the clocks are restarted, that is, until power-up sequencing is started. • While this bit is 1, the SBYST# pin remains low.
3:0	**Reserve d**

12.74 CR2C: LCD Interface Registe r

I/O Port Address: 3?5

Index: 2C

Bit	Description	Reset Stat e
7(MSB)	LCD Class Select [1]	0
6	LCD Class Select [0]	0
5	Horizontal Timing Shadow Registers Write Protect	0
4	Horizontal Timing Shadow Registers Select	0
3	CRT Controller Registers for LCD Timing Write Protect	0
2	Reserved	
1	LLCLK Invert	0
0(LSB)	LFS Invert	0

Bit **Descriptio n**

7:6 **LCD Class Select [1:0]:**
These 2 bits select the class of LCD to be connected. The following table lists available choices:

CR2C		LCD Class Selecte d
[7]	[6]	
0	0	Dual-scan monochrome LCD selected if CR2C[7:6] is 00 *and* R8X[5] is 0. Single-scan monochrome LCD selected if CR2C[7:6] is 00 *and* R8X[5] is 1.
0	1	Reserved
1	0	Dual-scan color STN LCD selected if CR2C[7:6] is 10 *and* SR21[6] is 1. Single-scan color STN LCD selected if CR2C[7:6] is 10 *and* SR21[6] is 0.
1	1	TFT-color LCDs selected. R9X[1:0] selects the pixel data format: 9-, 12-, 18- or 24-bit width .

5 **Horizontal Timing Shadow Registers Write Protect :**

- When this bit is 0:
  - — Extension registers RiY and RiZ (i = 0,2,3,4,5) are write-protected and cannot be accessed.
  - — Writing and reading applies only to standard VGA horizontal timing registers.
- When this bit is 1:
  - — Writing is done to both the standard VGA horizontal timing registers and Extension registers RiY and RiZ (i = 0,2,3,4,5).
  - — Reading is done only from the shadow registers.
- For write accesses to standard VGA horizontal timing registers, this bit is a ‘don’t care’.

12.74 CR2C: LCD Interface Register *(cont.)*

Bit	Description
4	**Horizontal Timing Shadow Registers Select:** This bit selects which set of horizontal-timing shadow registers the CL-GD7541/GD7543 uses. When CR2C[5] is 1 *and* this bit is: • 0, it selects Extension registers R0Y to R5Y, used with the normal DCLK. • 1, it selects Extension registers R0Z to R5Z, used with DCLK ÷ 2. (For information on DCLK ÷ 2, refer to Sequencer register SR1[3].)
3	**CRT Controller Registers for LCD Timing Write Protect:** • For LCD operation, some CRT controller registers must be write protected, that is, the last data bits written are used for CRT controller timing control, and a read/write shadow register is enabled for any subsequent I/O. • When this bit is 0, the value that is written is the same as the value that is read. • When this bit is 1, the value that is written is *not* the same as the value that is read and which takes effect. — In this case, the CRT Controller registers in the table below are write protected for LCD timing. — The value that does take effect is not a standard VGA value, because it is used to control the LCD (and not the CRT).
2	**Reserved**
1	**LLCLK Invert:** When this bit is 1, the normally active-high LLCLK output is inverted to active-low.
0	**LFS Invert:** When this bit is 1, the normally active-high LFS output is inverted to active-low.

CRT Controller Register / Bits	Description of CRT Controller Registers That Are Write Protected for LCD Timing
CR6 [7:0]	Vertical Total (protected value is used.)
CR7 [7, 5, 2, 0]	Vertical Overflow bits for total and synchronization start
CR10 [7:0]	Vertical Retrace Start (protected value is used for CRT VSYNC)
CR11 [3:0]	Vertical Retrace End (protected value is used for CRT VSYNC)
CR15 [7:0]	Vertical Blanking Start
CR16 [7:0]	Vertical Blanking End

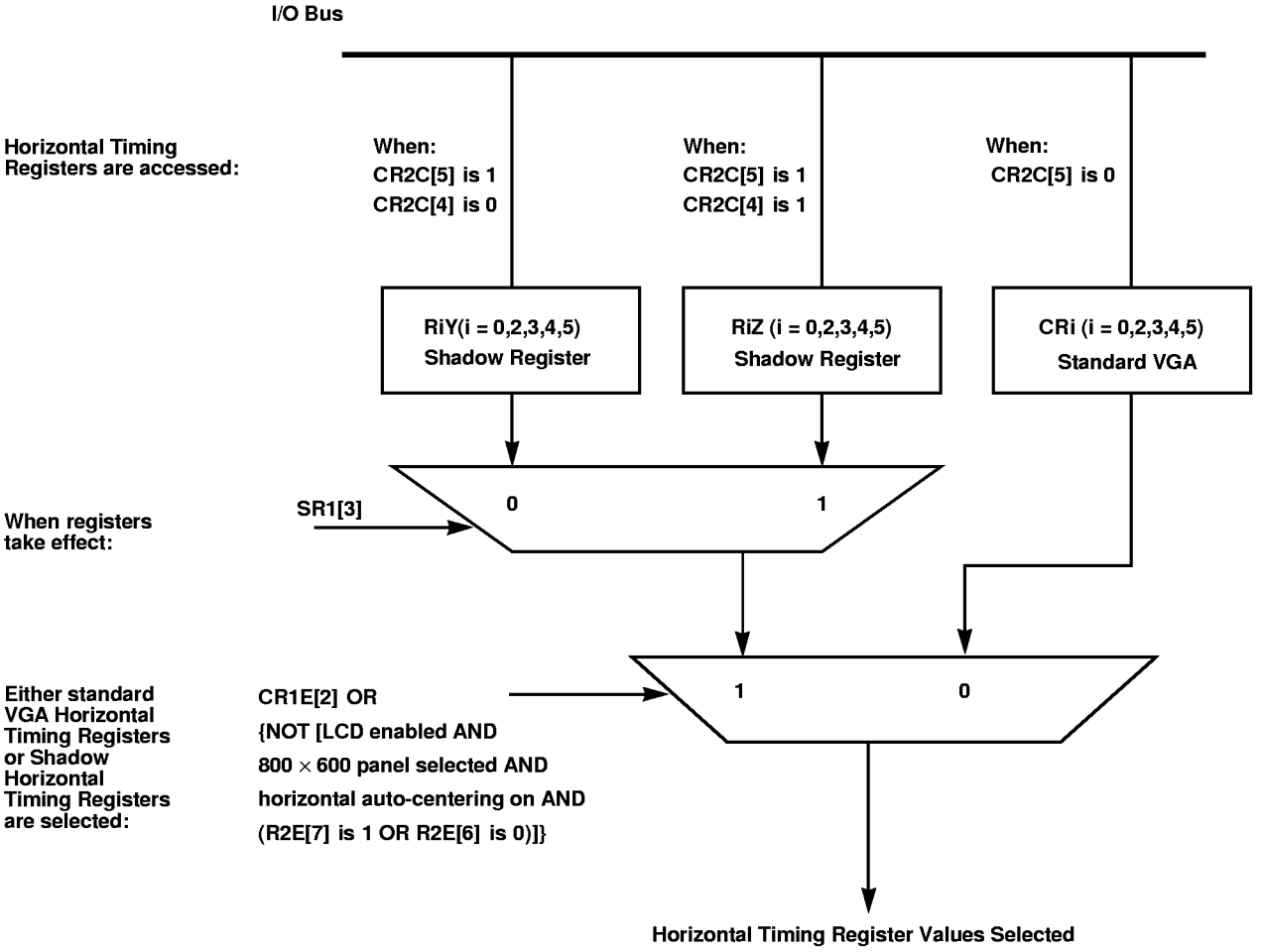


Figure 1 2-2. Horizontal Timing Register Values Selection

Table 1 2-1. Horizontal Timing Register Reference s

CRi (Standard VGA) Horizontal (H) Timing Register s		Horizontal (H) Timing Shadow Register s			
		RiY Register s		RiZ Register s	
CR0	H Total	R0Y	H Total	R0Z	H Total
CR2	H Blanking Start	R2Y	H Blanking Start	R2Z	H Blanking Start
CR3	H Blanking End	R3Y	H Blanking End	R3Z	H Blanking End
CR4	H Sync Start	R4Y	H Sync Start	R4Z	H Sync Start
CR5	H Sync End	R5Y	H Sync End	R5Z	H Sync End

12.75 CR2D: LCD Display Controls Register

I/O Port Address: 3?5

Index: 2D

Bit	Description	Reset State
7(MSB)	LCD Timing Registers Enable	0
6	Standby Mode Timer Reset by ACTI	0
5	Standby Mode Timer Reset by VGA Access	0
4	Suspend Mode Clock Source	0
3	Backlight Timer Reset by ACTI	0
2	Backlight Timer Reset by VGA Access	0
1	Automatic Vertical Expansion for 640 × 480 LCDs	0
0(LSB)	Automatic Centering Enable	0

Bit	Description
7	**LCD Timing Registers Enable:** • The CRT Controller Index register (CRX) does not have bits to index the LCD timing registers (Extension registers R2X to REX). Instead, CR2D[7] acts as an extra CRT Controller Index register bit to enable registers R2X to REX. • When this bit is 1, it enables read/write of Extension registers R2X to REX, which are mapped at the standard CRTC locations. These special timing control registers are used to control LLCLK, LFS, and other LCD control signals.
6	**Standby Mode Timer Reset by ACTI:** When this bit is set to 1, activity on the ACTI input pin resets the internal Standby Timer.
5	**Standby Mode Timer Reset by VGA Access:** When this bit is set to 1, any valid VGA memory access resets the internal Standby Timer.
4	**Suspend Mode Clock Source**: This bit selects the source for the clock used during Suspend mode. • When this bit is 0, a 32-kHz clock must be connected to the 32-kHz pin. • When this bit is 0, *and* when the CL-GD7541/GD7543 is in Suspend mode, the OSC input pin is disabled. • When this bit is set to 1, the 14-MHz clock required on the OSC input pin is divided by 432 to derive the 32-kHz clock.
3	**Backlight Timer Reset by ACTI:** When this bit is set to 1, activity on the ACTI input resets the Backlight control timer for the LCD.
2	**Backlight Timer Reset by VGA Access:** When this bit is set to 1, any valid VGA memory access resets the Backlight control timer for the LCD.

12.75 CR2D: LCD Display Controls Registe r *(cont.)*

Bit **Descriptio n**

1 **Automatic Vertical Graphics and Text Expansion for 640 × 480 LCDs :**
When this bit is:
- 0, it disables automatic graphics and text vertical expansion.
- 1, it enables automatic graphics and text vertical expansion for 640 × 480 LCDs, as controlled by the synchronization polarity bits in External/General register MISC[7:6].

MISC [7]	MISC [6]	Automatic Vertical Expansio n	
0	0	480 scanlines or more on a 800 × 600 LCD. Reserved in standard VGA .	
0	1	400- or 200-scanline mode	400-scanline mode is for text only. 200-scanline mode is for double-scanned graphics only .
1	0	350-scanline mode (text or graphics)	
1	1	480-scanline mode (graphics only, no vertical expansion)	

Vertical Expansion Method For Graphics Modes :

Original Scanlines	Vertical Expansion Method for Graphics Mode s
200	Pattern used is double-scan and triple-scan: 2,2,3,2,2,3,2, 3. Pattern expands 200 scanlines to 475 by expanding every 8 scanlines to 19.
350	Pattern used is single-scan and double-scan: 1,1,2,1,1,2,1,2,1,1,2,1,1,2. Pattern expands 350 scanlines to 475 by expanding every 14 scanlines to 19.

Vertical Expansion Method For Text Modes :

Original Scanlines / Font	Vertical Expansion Method for Text Mode s
200 scanlines, 8 × 8 font	Normal double-scan is applied . Extra scanlines (1 top and 2 bottom) are added to each character r ow (only when maximum row scan is set for 7 scanlines).
350 scanlines, 8 × 14 font	Extra scanlines (2 top and 3 bottom) are added to each character ro w (only when maximum row scan is set for 14 scanlines).
400 scanlines, 8 × 16 font	Extra scanlines (1 top and 2 bottom) are added to each character ro w (only when maximum row scan is set for 16 scanlines).

0 **Automatic Centering Enable:**
When this bit is:
- 0, automatic centering is disabled.
- 1, *and* when automatic expansion bit CR2D[1] is 0 (based on synchronization polarities), it enables LCD automatic centering. This action uses alternate LFS (line-frame start) timing as programmed in the LCD Timing registers, Extension register R2X to REX.

12.76 CR2E: LCD High-Resolution Control Registe r

I/O Port Address: 3?5

Index: 2E

Bit	Description	Reset Stat e
7(MSB)	Expansion Select Override [1]	0
6	Expansion Select Override [0]	0
5	Horizontal Centering Enable for LCDs	0
4	10-Dot True Fonts	0
3	Horizontal Graphics Expansion for 800 × 600 LCDs	0
2	Horizontal Font Expansion for 800 × 600 LCDs	0
1	Vertical Graphics Expansion for 800 × 600 LCDs	0
0(LSB)	Text Expansion for 800 × 600 LCDs	0

Bit	Descriptio n
7:6	**Expansion Select Override [1:0]:** • When these bits are 00, graphics expansion is controlled by CR2E[3,1]. • When these bits are 01, *and* R9X[3:2] bits are 01, an 800 × 600 LCD display size is selected. However, graphics expansion is disabled, even when bits CR2E[3,1] are set to 1. • Bit values 10 and 11 are reserved.
5	**Horizontal Centering Enable for LCDs:** A 1 in this bit enables horizontal centering for 800 × 600 LCDs.
4	**10-Dot True Fonts:** When this bit is 1 and a text mode is selected, 10-dot true fonts are selected.
3	**Horizontal Graphics Expansion for 800 × 600 LCDs:** When this bit is 1 and a graphics mode is selected, horizontal graphics expansion is enabled, which replicates every fourth pixel. • For an 800 × 600 LCD, this bit is used to expand 640-pixel data of each scanline to 800-pixel data. • This bit does not work in 16-bit/pixel and 24-bit/pixel modes.
2	**Horizontal Font Expansion for 800 × 600 LCDs:** When this bit is 1 and a text mode is selected, 8-dot-wide true fonts are expanded to 10 dots wide (instead of the normal 9-dot-wide VGA expansion).
1	**Vertical Graphics Expansion for 800 × 600 LCDs:** When this bit is 1 and a graphics mode is selected, vertical graphics on 800 × 600 LCDs are expanded by: • Doubling every odd scanline in 350-line and 400-line modes • Replicating every fourth scanline in 480-line mode
0	**Text Expansion for 800 × 600 LCDs:** When this bit is 1 and a text mode is selected, the text font is expanded by: • Doubling every odd scanline for 9 × 14 fonts or 8 × 16 fonts • Tripling every scanline for 8 × 8 fonts

12.77 CR2F: Driver and BIOS Revision Registe r

I/O Port Address: 3?5

Index: 2F

Bit	Description	Reset State
7(MSB)	Driver Revision [3]	'Driver Revision'
6	Driver Revision [2]	'Driver Revision'
5	Driver Revision [1]	'Driver Revision'
4	Driver Revision [0]	'Driver Revision'
3	BIOS Revision [3]	'BIOS Revision'
2	BIOS Revision [2]	'BIOS Revision'
1	BIOS Revision [1]	'BIOS Revision'
0(LSB)	BIOS Revision [0]	'BIOS Revision'

This read-only register returns two 4-bit codes that uniquely identify the CL-GD7541/GD7543 to drivers and to the BIOS.

Bit	Descriptio n
7:4	**Driver Revision [3:0] :** This 4-bit field contains a value identifying the CL-GD7541/GD7543 to various software drivers.
3:0	**BIOS Revision [3:0] :** This 4-bit field contains a value identifying the CL-GD7541/GD7543 to the video BIOS.

12.78 CR30: TV-OUT Control Register

I/O Port Address: 3?5

Index: 30

Bit	Description	Reset State
7(MSB)	PROG Pin-Level Control	0
6	Special CSYNC (CL-GD7541 Only)	0
5	Horizontal Total Dot-Clock Delay Control [1]	0
4	Horizontal Total Dot-Clock Delay Control [0]	0
3	TV-OUT Mode Enable	0
2	NTSC / PAL Output Control	0
1	CSYNC Dot-Clock Delay Control [1]	0
0(LSB)	CSYNC Dot-Clock Delay Control [0]	0

Bit **Description**

7 **PROG Pin-Level Control :**
This bit controls the logic level on the CL-GD7541/GD7543 PROG output pin. When this bit is a:
- 1, the PROG pin level is high.
- 0, the PROG pin level is low.

6 **Special CSYNC (CL-GD7541 Only):**
This bit is for use with special monitors from Apple®. When this bit is a:
- 0, the CSYNC pin operates normally.
- 1, the CSYNC pin outputs the XNOR of VSYNC and HSYNC.
  - — The polarity of the setting of External/General register MISC affects the VSYNC and HSYNC components of this CSYNC signal. Consequently, there is full flexibility of polarity with non-VGA modes.
  - — This bit must not be used with VGA programs that change the polarity of the SYNC bits of External/General register MISC from mode to mode.

5:4 **Horizontal Total Dot-Clock Delay Control [1:0] :**
The value in these bits control the dot-clock delay for the horizontal total signal according to the following table:

CR30		Dot-Clock Delay for Horizontal Total
[5]	[4]	
0	0	No delay
0	1	Delay is 2 Dot Clocks
1	0	Delay is 4 Dot Clocks
1	1	Delay is 6 Dot Clocks

12.78 CR30: TV-OUT Control Register *(cont.)*

Bit	Descriptio n
3	**TV-OUT Mode Enable:** • When this bit is 1, the TV-OUT mode is enabled, and TVON output is high. • When this bit is 0, the NTSC/PAL, CSYNC, and TVON outputs are all forced low, and CR30[2] is disabled. • When Extension register SR25[6] is 1, the TVON pin is not controlled by CR30[3]. However, the TV-OUT feature can still be used without a power-down feature on CR30[3].
2	**NTSC / PAL Output Control :** This bit is programmed to reflect the required input levels to the NTSC/PAL encoder. • When CR30[3] is 0, this bit is disabled. • When CR30[3] is 1, *and* this bit is: — 0, this bit creates a low on the NTSC/PAL output pin. — 1, this bit creates a high on the NTSC/PAL output pin.
1:0	**CSYNC Dot-Clock Delay Control [1:0]:** The value in these bits control the dot-clock delay for the generation of a composite synchronization signal (CSYNC) according to the following table.

CR30		Horizontal CSYNC Start
[1]	[0]	
0	0	No delay
0	1	Delay is 2 Dot Clocks
1	0	Delay is 4 Dot Clocks
1	1	Delay is 6 Dot Clocks

12.79 CR33: MVW Horizontal Start (XS) / Width (XW) Overflow (CL-GD7543 Only)

I/O Port Address: 3?5

Index: 33

Bit	Description	Reset State
7(MSB)	Reserved	
6	MVW Horizontal Start (XS) [9]	0
5	MVW Horizontal Start (XS) [8]	0
4	Reserved	
3	MVW Horizontal Width (XW) [9]	0
2	MVW Horizontal Width (XW) [8]	0
1	MVW Memory Bandwidth Improvement	0
0(LSB)	Fast MVA FIFO Request Enable	0

In the MVW (MotionVideo Window), the horizontal start position is programmed using the number of memory cycles used by the surrounding pixel-depth resolution.

Bit	Description
7	**Reserved**
6:5	**MVW Horizontal Start (XS) [9:8] :** These bits are the most-significant 2 bits of a 10-bit field that defines the horizontal starting position of the MotionVideo Window. For details, refer to Extension register CR34.
4	**Reserved**
3:2	**MVW Horizontal Width (XW) [9:8] :** These bits are the most-significant 2 bits of a 10-bit field that defines the horizontal width of the MotionVideo Window. For details, refer to Extension register CR35.
1	**MVW Memory Bandwidth Improvement:** When this bit is: • 0, the CPU can access the video memory during the MVW refresh. Normally, this bit is 0. • 1, the CPU cannot access the video memory during the MVW refresh. Assert this bit only if there is not enough video memory bandwidth because: — The MVW has a high pixel depth. — The dot clock has a high frequency.
0	**Fast MVA FIFO Request Enable:** This bit enables bypassing the synchronizer in the MVA (MotionVideo Acceleration) circuitry to fill the FIFO faster.

12.80 CR34: MVW Horizontal Start (XS) Register (CL-GD7543 Only)

I/O Port Address: 3?5

Index: 34

Bit	Description	Reset State
7(MSB)	MVW Horizontal Start (XS) [7]	0
6	MVW Horizontal Start (XS) [6]	0
5	MVW Horizontal Start (XS) [5]	0
4	MVW Horizontal Start (XS) [4]	0
3	MVW Horizontal Start (XS) [3]	0
2	MVW Horizontal Start (XS) [2]	0
1	MVW Horizontal Start (XS) [1]	0
0(LSB)	MVW Horizontal Start (XS) [0]	0

This register contains the least-significant 8 bits of the 10-bit MVW (MotionVideo Window) horizontal start position field. In the MVW, the starting horizontal position is programmed by using the number of memory fetch cycles in the surrounding pixel-depth resolution.

Bit **Description**

7:0 **MVW Horizontal Start (XS) [7:0] :**

- These are the least-significant 8 bits of the MVW horizontal start position field.
- The most-significant 2 bits are in Extension register CR33[6:5].

To program XS (the horizontal coordinate to start the MVW on the screen):

- Determine the number of the pixel at which the MVW must start.
- Determine the surrounding pixel-depth resolution, in bits per pixel.
- Determine the size of the memory bus, which determines how many bits each memory fetch cycle transfers.
- Obtain the number of pixels per memory fetch cycle by dividing the size of the memory bus by the number of bits in the surrounding pixel-depth resolution. (If the memory bus is 32 bits wide and 4 bits per pixel is used for the surrounding pixel-depth resolution, the number of pixels per memory fetch cycle is 8.)
- Divide the number of the pixel at which the MVW must start by the number of pixels per memory fetch cycle.
- Program the resulting value into CR34[7:0].

For example,

If: A MVW is to start at pixel 16.
The surrounding pixel-depth resolution is 4 bits per pixel.
The memory bus transfers 32 bits (32-bit memory fetch cycle).

Then: The number of pixels per memory fetch cycle is 32 ÷ 4 = 8.
The number of memory fetch cycles needed for a MWV starting at pixel 16 is 2. (A starting MVW value pixel number of 16 ÷ 8 pixels per memory fetch cycle = 2 memory fetch cycles.)

Program: Into CR34[7:0] the value 2 as the number of memory fetch cycles needed for a MVW starting at pixel 16.

12.81 CR35: MVW Horizontal Width (XW) Register (CL-GD7543 Only)

I/O Port Address: 3?5

Index: 35

Bit	Description	Reset State
7(MSB)	MVW Horizontal Width (XW) [7]	0
6	MVW Horizontal Width (XW) [6]	0
5	MVW Horizontal Width (XW) [5]	0
4	MVW Horizontal Width (XW) [4]	0
3	MVW Horizontal Width (XW) [3]	0
2	MVW Horizontal Width (XW) [2]	0
1	MVW Horizontal Width (XW) [1]	0
0(LSB)	MVW Horizontal Width (XW) [0]	0

This register contains the least-significant 8 bits of the 10-bit MVW horizontal width field, which is calculated in video resolution memory fetch cycles as explained below.

Bit **Description**

7:0 **MVW Horizontal Width (XW) [7:0] :**

- These bits are the least-significant 8 bits of the MVW horizontal width field.
- The most-significant 2 bits are in Extension register CR33[3:2].
- This field must be programmed for the MVW, even when the MVW is displayed on the full screen.

To program the number of memory fetch cycles needed for the value of XW (the horizontal width):

- Determine the width of the MotionVideo Window, in pixels.
- Determine the color depth of the MVW display, in bits per pixel.
- Determine the size of the memory bus, which determines how many bits each memory fetch cycle transfers.
- Multiply the MVW width (in pixels) times the MVW depth (in bits per pixel).
- Divide the above quantity by how many bits each memory fetch cycle transfers.
- Program the resulting value into CR35[7:0].

For example,

If:	A MVW is 320 pixels wide. The MVW display has a color depth of 16 bits per pixel. The memory bus transfers 32 bits wide (a 32-bit fetch cycle).
Then:	Multiply the MVW width (320 pixels) × MVW depth (16 bits/pixel). Divide the above quantity by the number of bits each memory fetch cycle transfers (32).
Program:	Into CR35[7:0] the resulting value of 160 memory fetch cycles.

12.82 CR36: YUV-to-RGB Conversion / MVW Vertical-Position High Register (CL-GD7543 Only)

I/O Port Address: 3?5

Index: 36

Bit	Description	Reset State
7(MSB)	Force Linear Display Memory Map	0
6	YUV-to-RGB Conversion with Standard Algorithm or Other	0
5	YUV-to-RGB Conversion with Excess 128 or 2's Complement	0
4	MVW Memory Address Offset [8]	0
3	MVW Vertical End (YE) Position [9]	0
2	MVW Vertical End (YE) Position [8]	0
1	MVW Vertical Start (YS) Position [9]	0
0(LSB)	MVW Vertical Start (YS) Position [8]	0

Bit	Description
7	**Force Linear Display Memory Map :** This bit is used to simplify the use of MVA drivers by providing a unique way of accessing the memory for MVW, from the CPU side. • When this bit is 1, the CPU linearly writes data to the display memory, the same way as in extended 8-bit-per-pixel packed-pixel modes. • Set this bit to 1 when writing to MVW memory and running Microsoft® Windows in 4-bit-per-pixel planar mode to ensure that writes to MVW memory execute independently of surrounding graphics. • After executing writes to the MVW memory area, the Windows driver must set this bit to 0.
6	**YUV-to-RGB Conversion with Standard Algorithm or Other :** When this bit is: • 0, the YUV-to-RGB conversion uses the standard algorithm: R = Y + 1.375V; G = Y – 0.375U – 0.7V; B = Y + 1.75U • 1, the YUV-to-RGB conversion uses the algorithm: R = Y + V; G = Y – 0.5U – 0.5V; B = Y + U
5	**YUV-to-RGB Conversion with Excess 128 or 2's Complement:** These conversions assume that U and V are expressed in either excess 128 or 2's complement notation. When this bit is: • 0, the YUV-to-RGB conversion uses 2's complement notation. • 1, the YUV-to-RGB conversion uses excess 128 notation.
4	**MVW Memory Address Offset [8]:** This is the most-significant bit of MVW Memory Address Offset register CR3B.
3:2	**MVW Vertical End (YE) Position [9:8] :** These are the most-significant bits of the MVW Vertical End register CR38.
1:0	**MVW Vertical Start (YS) Position [9:8] :** These are the most-significant bits of the MVW Vertical Start register CR37.

12.83 CR37: MVW Vertical Start (YS) Position Register (CL-GD7543 Only)

I/O Port Address: 3?5

Index: 37

Bit	Description	Reset State
7(MSB)	MVW Vertical Start (YS) Position [7]	0
6	MVW Vertical Start (YS) Position [6]	0
5	MVW Vertical Start (YS) Position [5]	0
4	MVW Vertical Start (YS) Position [4]	0
3	MVW Vertical Start (YS) Position [3]	0
2	MVW Vertical Start (YS) Position [2]	0
1	MVW Vertical Start (YS) Position [1]	0
0(LSB)	MVW Vertical Start (YS) Position [0]	0

Bit	Description
7:0	**MVW Vertical Start (YS) Position [7:0] :** • These bits are the least-significant 8 bits of the 10-bit field for the MVW Vertical Start (YS) Position. • The 10 bits of this field: — Define actual scanlines — Are not affected by scanline doubling or LCD vertical expansion • The most-significant 2 bits are in Extension register CR36[1:0].

12.84 CR38: MVW Vertical End (YE) Position Register (CL-GD7543 Only)

I/O Port Address: 3?5

Index: 38

Bit	Description	Reset State
7(MSB)	MVW Vertical End (YE) Position [7]	0
6	MVW Vertical End (YE) Position [6]	0
5	MVW Vertical End (YE) Position [5]	0
4	MVW Vertical End (YE) Position [4]	0
3	MVW Vertical End (YE) Position [3]	0
2	MVW Vertical End (YE) Position [2]	0
1	MVW Vertical End (YE) Position [1]	0
0(LSB)	MVW Vertical End (YE) Position [0]	0

Bit	Description
7:0	**MVW Vertical End (YE) Position [7:0] :** • These bits are the least-significant 8 bits of the 10-bit field for the MVW Vertical End (YE) position. • The 10 bits of this field: — Define actual scanline — Are not affected by scanline doubling or LCD vertical expansion • The most-significant 2 bits are in Extension register CR36[3:2].

12.85 CR39: MVW Surroundin g Address Offset Registe r (CL-GD754 3 Only)

I/O Port Address: 3?5

Index: 39

Bit	Description	Reset State
7(MSB)	MVW Surrounding Address Offset [7]	0
6	MVW Surrounding Address Offset [6]	0
5	MVW Surrounding Address Offset [5]	0
4	MVW Surrounding Address Offset [4]	0
3	MVW Surrounding Address Offset [3]	0
2	MVW Surrounding Address Offset [2]	0
1	MVW Surrounding Address Offset [1]	0
0(LSB)	MVW Surrounding Address Offset [0]	0

This register defines an offset value used when the MVW width is less than the screen maximum.

Bit **Descripti on**

7:0 **MVW Surroundin g Address Offse t [7:0] :**
This register is used when the MVW width is less than the screen maximum.

- The address offset value in this register is added to the address in the CRT address counter to allow the counter to skip over the area for the MVW.
- As a result, a restart address for the surrounding area can be defined without having to count through the MVW.
- This address offset value depends on the resolution of the surrounding mode.

To program this register for the surrounding address offset:

- For the MVW, determine its width in pixels.
- For the surrounding area, determine:
  - — The number of bits/pixel.
  - — The number of pixels/memory access.
- Determine the address offset for the MVW by dividing its width by the number of pixels in a memory fetch cycle.
- Program into this register one-half the resulting value.

For example,

If:	The MVW is 320 pixels wide. The surrounding area has 4 bits/pixel. Therefore the number of pixels/memory access is 8. (The 32-bit width of the memory bus divided by 4 = 8 pixels/memory access.)
Then:	The offset is 320 ÷ 8 pixels/address = a 40-address offset. One-half of 40 is 20 decimal (14 hex).
Program:	Into CR39[7:0] the resulting value of 14h.

12.86 CR3A: MVW Memor y Address Start Registe r (CL-GD754 3 Only)

I/O Port Address: 3?5

Index: 3A

Bit	Description	Reset State
7(MSB)	Reserved	
6	MVW Memory Address Start [6]	0
5	MVW Memory Address Start [5]	0
4	MVW Memory Address Start [4]	0
3	MVW Memory Address Start [3]	0
2	MVW Memory Address Start [2]	0
1	MVW Memory Address Start [1]	0
0(LSB)	MVW Memory Address Start [0]	0

Bit	Descriptio n
7	**Reserve d**
6:0	**MVW Memory Addres s Start [6:0] :** This address is programmed in increments of 16 Kbytes (4 Kwords). For example, for: • 1 Mbyte, the physical address is 00000:3FFF F from the display memory start. • 2 Mbytes, the physical address is 00000:7FFF F from the display memory start **NOTE:** This start address *must* be aligned at a 16-Kbyte boundary in the CPU host address space.

12.87 CR3B: MVW Memory Address Offset Register (CL-GD7543 Only)

I/O Port Address: 3?5

Index: 3B

Bit	Description	Reset State
7(MSB)	MVW Memory Address Offset [7]	0
6	MVW Memory Address Offset [6]	0
5	MVW Memory Address Offset [5]	0
4	MVW Memory Address Offset [4]	0
3	MVW Memory Address Offset [3]	0
2	MVW Memory Address Offset [2]	0
1	MVW Memory Address Offset [1]	0
0(LSB)	MVW Memory Address Offset [0]	0

This register, along with the most-significant bit in CR36[4], defines an offset value

Bit	Description
7:0	**MVW Memory Address Offset [7:0] :** • These bits are the least-significant 8 bits of the 9-bit MVW memory address offset value. This offset value is added to the present MVW Memory Start Address to get the next MVW Memory Start Address. ADD: Present MVW Memory Start Address TO: + MVW Memory Address Offset (9-bit value)] × 2 TO OBTAIN: = Next MVW Memory Start Address • Using the MVW Memory Address Offset to define the next memory-start address of the MVW allows panning through a large area of the MVW. The actual image stored in memory may be as large as 2K pixels at 16 bits/pixel. • The most-significant bit is in Extension register CR36[4].

12.88 CR3C: MVW Scaling, Enable, and Encoding Format Register (CL-GD754 3 Only)

I/O Port Address: 3?5

Index: 3C

Bit	Description	Reset State
7(MSB)	MVW Horizontal Scaling	0
6	MVW Vertical Scaling	0
5	Full-Screen Live-Video Enable	0
4	MVW Enable	0
3	MVW Encoding Format [3]	0
2	MVW Encoding Format [2]	0
1	MVW Encoding Format [1]	0
0(LSB)	MVW Encoding Format [0]	0

Bit **Descriptio n**

7 **MVW Horizontal Scaling:**
When this bit is 1, each pixel is duplicated horizontally.

6 **MVW Vertical Scaling:**
When this bit is 1, each pixel is duplicated vertically.

5 **Full-Screen Live-Video Enable:**
When this bit is 1, through MVA the MVW uses the entire screen to display live video from off-screen display memory.

4 **MVW Enable :**
When this bit is 1, the MVW is enabled to fetch data from off-screen display memory and display it on the screen based on current programming for MVA registers.

3:0 **MVW Encoding Format [3:0]:**
These bits define in which format the MVW is encoded.

CR3C[3:0]		Encoding Format for MV W
0h	0000	8-bit RGB (3:3:2 true color)
1h	0001	15-bit RGB (5:5:5)
2h	0010	Reserved
3h	0011	4:2:2 YUV Y0UY1V. (On the CPU bus, this encoding format appears as UY0 VY1.)
4h:7h	0100 to 0111	Reserved
8h	1000	24-bit RGB (8:8:8)
9h	1001	8-bit RGB (mapped through the RAMDAC palett e)
Ah–15h	1010 to 1111	Reserved

12.89 CR3D: MVW Horizontal-Pixel-Width Register (CL-GD7543 Only)

I/O Port Address: 3?5

Index: 3D

Bit	Description	Reset State
7(MSB)	Reserved	
6	MVW Horizontal Pixel Width [6]	0
5	MVW Horizontal Pixel Width [5]	0
4	MVW Horizontal Pixel Width [4]	0
3	MVW Horizontal Pixel Width [3]	0
2	MVW Horizontal Pixel Width [2]	0
1	MVW Horizontal Pixel Width [1]	0
0(LSB)	MVW Horizontal Pixel Width [0]	0

Bit	Description
7	**Reserved**
6:0	**MVW Horizontal Pixel Width [6:0] :** These bits contain a hex value used to define the MVW width for each scanline the MVW is enabled. To calculate the value: • Determine the desired width of the MVW, which must be at least 32 pixels wide. • From the desired width, subtract 24 pixels (three sets of 8 pixels). • Divide the resulting number by 8-pixel increments. • Translate the resulting decimal number into a hex number. For example, to calculate the hex value for a 320-pixel-wide MVW: DIVIDE: The quantity (320 pixels - 24 pixels = 296 pixels) BY: ÷ 8-pixel increments TO OBTAIN: = Value for a 320-pixel-wide MVW, where 37 (decimal) = 25h **NOTE:** The MVW width is expressed in 8-pixel increments in all operation modes.

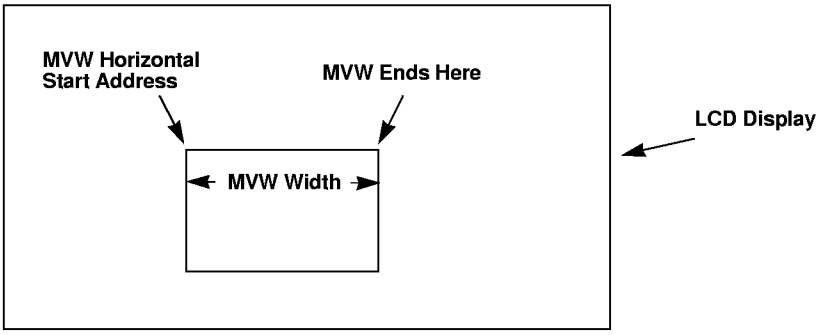


Figure 12-3. LCD Display with MotionVideo™ Window

12.90 CR40: LCD Horizontal-Display-Enable Start Register – No Centerin g

I/O Port Address: 3?5

Index: 40

Bit	Description	Reset State
7(MSB)	LCD HDE Start (No Centering) [7]	0
6	LCD HDE Start (No Centering) [6]	0
5	LCD HDE Start (No Centering) [5]	0
4	LCD HDE Start (No Centering) [4]	0
3	LCD HDE Start (No Centering) [3]	0
2	LCD HDE Start (No Centering) [2]	0
1	LCD HDE Start (No Centering) [1]	0
0(LSB)	LCD HDE Start (No Centering) [0]	0

This register is one of four registers – CR40, CR41, CR42, and CR43 –that are used both to generate LCD horizontal position and to center 640 × 480 and 800 × 600 LCDs.

Three registers – CR40, CR41, and CR42 – are complementary and mutually exclusive. Although they store the same timing-signal parameters, the values for the timing-signal parameters are usually different.

- Only one of these three registers is enabled at any time.
- The selection of which of these three registers control the LCD is done automatically, based on the conditions explained for each register.
- These three registers are generally programmed only once at power-on self-test

The CL-GD7541/GD7543 automatically selects register CR40 as the default LCD horizontal-display-enable (HDE) start register if:

- Either CR41 or CR42 *are not* selected, or
- Horizontal expansion *is* selected

In normal 24-bit LCD modes, the CL-GD7541/GD7543 starts to send data to the LCD immediately after HDE start, which may cause problems for some graphics modes. These three registers may be programmed to avoid the problems.

For typical timing relationships, refer to Figure 12-4.

12.90 CR40: LCD Horizontal-Display-Enable Start Register – No Centering *(cont.)*

Bit	Description
7:0	**LCD HDE Start (No Centering) [7:0]:** When no horizontal centering is needed, this register defines LCD HDE start (that is, the rising edge of the LCD horizontal display enable signal), relative to the previous CRT HDE start. • The value in this register defines both the LCD Line Clock start and the LCD HDE start, for both 640 × 480 and 800 × 600 LCDs. • For this register, a fine (dot-clock) adjustment in 1-DCLK units is in CR43[1:0] The LCD HDE start is expressed in 4-DCLK units. To calculate LCD HDE start: DIVIDE: [(Number of CRT Horizontal Total pixels) minus 32 pixels] BY: ÷ 4 (Number of 4-DCLK units) TO OBTAIN: = LCD HDE Start Where: Horizontal Total = CRT horizontal total in DCLK units. For example, If: A panel is 640 × 480 with a Horizontal Total of 800. Then: The CRT Horizontal Total, minus 32 is (800 – 32) = 768. The quantity 768 expressed in 4-DCLK units is (768 ÷ 4) = 192 decimal. Program: Into CR40 the hex value of 192 decimal, which is C0h.

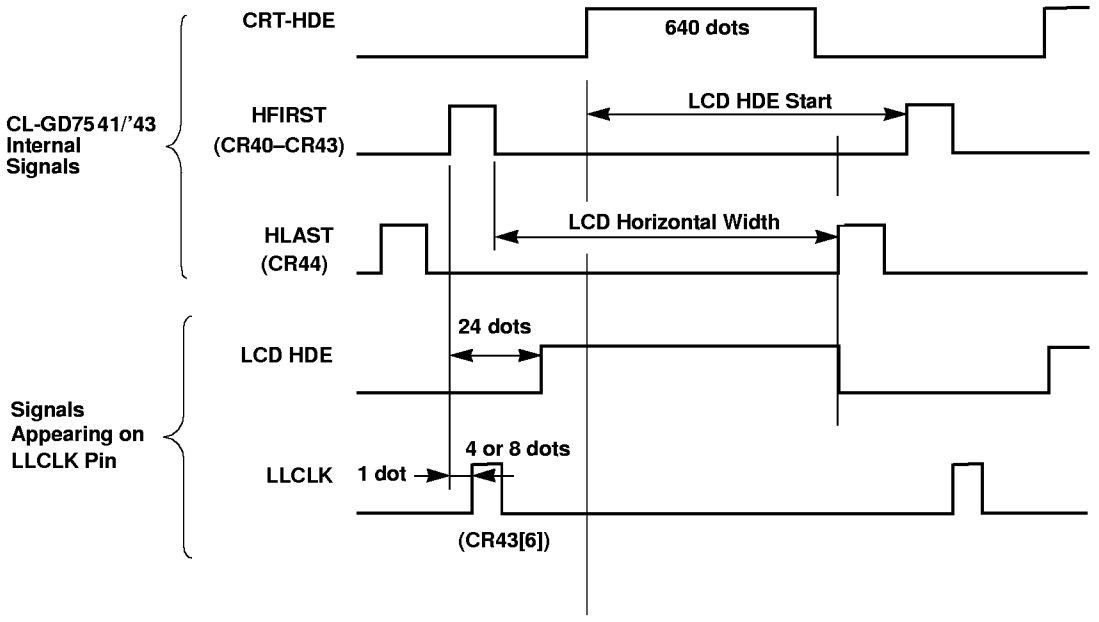


Figure 12-4. Horizontal Position for STN LCD Displaying 640 × 480 Picture

12.91 CR41: LCD Horizontal-Display-Enable Start to Center 720-Dot Displa y

I/O Port Address: 3?5

Index: 41

Bit	Description	Reset State
7(MSB)	LCD HDE Start to Center 720-Dot Display [7]	0
6	LCD HDE Start to Center 720-Dot Display [6]	0
5	LCD HDE Start to Center 720-Dot Display [5]	0
4	LCD HDE Start to Center 720-Dot Display [4]	0
3	LCD HDE Start to Center 720-Dot Display [3]	0
2	LCD HDE Start to Center 720-Dot Display [2]	0
1	LCD HDE Start to Center 720-Dot Display [1]	0
0(LSB)	LCD HDE Start to Center 720-Dot Display [0]	0

This register is one of four registers – CR40, CR41, CR42, and CR43 –that are used both to generate LCD horizontal timing and to center 640 × 480 and 800 × 600 LCDs. (For a description of all four registers and for the formula to calculate the LCD HDE start, refer to CR40.)

The CL-GD7541/GD7543 automatically uses this register to provide centering of a 720-dot display (text or graphics) when all the following conditions are met:

- The LCD is an 800 × 600.
- The LCD is not using 800 × 600 graphics modes.
- The LCD is using a character clock of 9-DCLK cycles (in text mode), or CRT HDE > 50h (in graphics mode).
- The LCD is not using horizontal expansion.

Bit	Descriptio n
7:0	**LCD HDE Start to Center 720-Dot Display [7:0] :** This register provides centering of a 720-dot display (text or RiX graphics mode) on a 800 × 600 LCD by defining the present LCD HDE start signal. • This register defines the present HDE start signal, relative to the previous HDE start signal, in 4-DCLK increments. (The DCLK is never divided by two.) • The value programmed in this register is in 4-DCLK increments, and this value is one less than the HDE start parameter. • On a 800 × 600 LCD, the value in this register defines both the LCD line-clock start and the LCD HDE start signals. A fine adjustment for this register is in Extension register CR43[3:2]. • When horizontal expansion is enabled, instead of using this register to define the LCD HDE start signal, the value in CR40 is used to define the LCD HDE start signal.

12.92 CR42: LCD Horizontal-Display-Enable Start to Center 640-Dot Displa y

I/O Port Address: 3?5

Index: 42

Bit	Description	Reset State
7(MSB)	LCD HDE Start to Center 640-Dot Display [7]	0
6	LCD HDE Start to Center 640-Dot Display [6]	0
5	LCD HDE Start to Center 640-Dot Display [5]	0
4	LCD HDE Start to Center 640-Dot Display [4]	0
3	LCD HDE Start to Center 640-Dot Display [3]	0
2	LCD HDE Start to Center 640-Dot Display [2]	0
1	LCD HDE Start to Center 640-Dot Display [1]	0
0(LSB)	LCD HDE Start to Center 640-Dot Display [0]	0

This register is one of four registers – CR40, CR41, CR42, and CR43 –that are used both to generate LCD horizontal timing and to center 640 × 480 and 800 × 600 LCDs. (For a description of all four registers and for the formula to calculate the LCD HDE start, refer to CR40.)

The CL-GD7541/GD7543 automatically uses this register to provide centering of a 640-dot display (text or graphics) when all the following conditions are met:

- The LCD is an 800 × 600.
- The LCD is not using 800 × 600 graphics modes.
- The LCD is using a character clock of 8-DCLK cycles, and CRT HDE ≤ 50h.
- The LCD is not using horizontal expansion.

Bit	Descriptio n
7:0	**LCD HDE Start to Center 640-Dot Display [7:0]:** This register provides centering of a 640-dot display on a 800× 600 LCD by defining the present LCD HDE start signal. • This register defines the present HDE start signal, relative to the previous HDE start signal, in 4-DCLK increments. (The DCLK is never divided by two.) • The value programmed in this register is in 4-DCLK increments, and this value is one less than the HDE start parameter. • On a 800 × 600 LCD, the value in this register defines both the LCD line-clock start and the LCD HDE start signals. A fine adjustment for this register is inEx-tension register CR43[5:4]. • When horizontal expansion is enabled, instead of using this register to define the LCD HDE start signal, the value in CR40 is used to define the LCD HDE start signal.

12.93 CR43: LCD Dot-Clock-Delay Control Register

I/O Port Address: 3?5

Index: 43

Bit	Description	Reset State
7(MSB)	Reserved	
6	LCD Line-Clock Width	0
5	CR42 Fine Dot-Clock Delay [1]	0
4	CR42 Fine Dot-Clock Delay [0]	0
3	CR41 Fine Dot-Clock Delay [1]	0
2	CR41 Fine Dot-Clock Delay [0]	0
1	CR40 Fine Dot-Clock Delay [1]	0
0(LSB)	CR40 Fine Dot-Clock Delay [0]	0

This register is one of four registers – CR40, CR41, CR42, and CR43 – that are used both to generate LCD horizontal timing and to center 640 × 480 and 800 × 600 LCDs. (For a description of all four registers and for the formula to calculate the LCD HDE start, refer to CR40.)

Bits [7:6] set the LCD line clock width.

Bits [5:0] make up three fields that when required, compensate for the CL-GD7541/GD7543 internal delays of the LCD horizontal display enable (HDE) start signal.

- For the different types of LCDs, these three fields make it possible to change the LCD horizontal display enable (HDE) start by adjusting the fine dot-clock delay in 1-DCLK units.
- When it is necessary to change the LCD horizontal display enable (HDE) start, automatic switching takes place between these three fields. The switching is based on the following:
  — Values in the CRT controller registers
  — Values in the Sequencer registers
  — The type of LCD used (that is, 640 × 480 or 800 × 600)

Note: Because LCD counters are reset 1 dot clock after resetting the CRT HDE Total counter, values in LCD registers must be programmed with a delay of one less than the model.

Bit	Description
7	**Reserved**
6	**LCD Line-Clock Width:** When this bit is: • 0, the LCD line-clock width is 4 dot clocks. • 1, the LCD line-clock width is 8 dot clocks.

12.93 CR43: LCD Dot-Clock-Delay Control Register *(cont.)*

Bit	Descriptio n
5:4	**CR42 Fine Dot-Clock Delay [1:0]:** To program the LCD HDE start signal for a dot-clock delay, refer to Table 12-2.
3:2	**CR41 Fine Dot-Clock Delay [1:0]:** To program the LCD HDE start signal for a dot-clock delay, refer to Table 12-2.
1:0	**CR40 Fine Dot-Clock Delay [1:0]:** To program the LCD HDE start signal for a dot-clock delay, refer to Table 12-2.

Table 1 2-2. Fine Dot-Clock Delay Options for LCD HDE Start Signal s

CR43		Fine Dot-Clock Delay for:
[5]	[4]	CR42
[3]	[2]	CR41
[1]	[0]	CR40
0	0	No delay
0	1	Delay LCD HDE start by 1 DCLK
1	0	Delay LCD HDE start by 2 DCLKs
1	1	Delay LCD HDE start by 3 DCLKs

12.94 CR44: LCD Horizontal Display Width Registe r

I/O Port Address: 3?5

Index: 44

Bit	Description	Reset State
7(MSB)	LCD Horizontal Display Width [7]	0
6	LCD Horizontal Display Width [6]	0
5	LCD Horizontal Display Width [5]	0
4	LCD Horizontal Display Width [4]	0
3	LCD Horizontal Display Width [3]	0
2	LCD Horizontal Display Width [2]	0
1	LCD Horizontal Display Width [1]	0
0(LSB)	LCD Horizontal Display Width [0]	0

This register defines the LCD horizontal width.

Bit	Descriptio n
7:0	**LCD Horizontal Display Width [7:0]:** The value programmed in this register: • Defines the LCD horizontal display width, which can be different from the stored picture width. • Is used to compensate for internal delays when displaying a narrow picture on a wide screen. • Is never expressed in units of DCLK ÷ 2. • Equals the desired width (expressed in 4 DCLK increments), plus four, all expressed in hex. For example, If: An LCD panel is 640 (horizontal) x 480 (vertical). Then: The desired width is 640 pixels. The desired width, when expressed in 4 DCLK increments, is 640 ÷ 4 = 160. The desired 4-DCLK width of 160, plus 4 = 164 decimal. Program: Into CR44[7:0] the hex equivalent of 164 decimal, which is A4 hex.

12.95 CR47: TFT HSYNC Horizontal Start Position Registe r

I/O Port Address: 3?5

Index: 47

Bit	Description	Reset State
7(MSB)	TFT HSYNC Horizontal Start Position [7]	0
6	TFT HSYNC Horizontal Start Position [6]	0
5	TFT HSYNC Horizontal Start Position [5]	0
4	TFT HSYNC Horizontal Start Position [4]	0
3	TFT HSYNC Horizontal Start Position [3]	0
2	TFT HSYNC Horizontal Start Position [2]	0
1	TFT HSYNC Horizontal Start Position [1]	0
0(LSB)	TFT HSYNC Horizontal Start Position [0]	0

This register defines the start of the TFT HSYNC signal. This register is not dependent on character-clock width or DCLK/2 control.

Bit	Descriptio n
7:0	**TFT HSYNC Horizontal Start Position [7:0]:** This register defines the exact starting position of the TFT HSYNC signal The TFT HSYNC Horizontal Start Position is: • Relative to the previous LCD CRT horizontal display enable (HDE) start, in DCLK/4 increments. • Positioned about 144 dot clocks before the start of the LCD HDE start signal, which is also relative to the CRT HDE start. • Adjustable in 1-DCLK increments with CR48[1:0]. When Extension register R7X[2] = 1: • The TFT HSYNC signal, instead of the LLCLK signal, appears on the LLCLK pin. (The LLCLK signal always starts 1 DCLK after the LCD HDE start.) • This setup is needed to support TFT LCDs that require 144 dot clocks between LLCLK and the first shift clock on a scanline. **NOTE :** Some LCD manufacturers call the LLCLK signal HSYNC. Cirrus Logic calls this signal TFT HSYNC, to differentiate it from the CRT HSYNC signal.

12.96 CR48: TFT HSYNC and LCD-Height Overflow Registe r

I/O Port Address: 3?5

Index: 48

Bit	Description	Reset State
7(MSB)	Reserved	
6	Reserved	
5	Vertical Size for LCDs [9]	0
4	Vertical Size for LCDs [8]	0
3	Reserved	
2	Vertical Size for Upper Half of Dual-Scan STN LCDs [8]	0
1	TFT HSYNC Dot-Clock Delay [1]	0
0(LSB)	TFT HSYNC Dot-Clock Delay [0]	0

Bit — **Descriptio n**

7:6 — **Reserve d**

5:4 — **Vertical Size for LCD s [9:8] :**
- These bits are the most-significant 2 bits of a 10-bit field that defines in scan-lines the vertical size for one of the following:
  - — The lower half of a dual-scan STN LCD
  - — The total size of a single-scan LCD, either STN or TFT
- The least-significant 8 bits are in Extension register CR4A[7:0].

3 — **Reserve d**

2 — **Vertical Size for Upper Half of Dual-Scan STN LCD s [8]:**
- This bit is the most-significant bit of a 9-bit field that defines in scanlines the vertical size for the upper half of a dual-scan STN LCD.
- The least-significant 8 bits are in Extension register CR49[7:0].

1:0 — **TFT HSYNC Dot-Clock Delay [1:0] :**
- These bits provide further control, in 1-DCLK increments, for the TFT HSYNC horizontal start position defined in CR47 in 4-DCLK increments.
- These bits control the dot-clock delay in 1-DCLK increments, according to the following table:

CR48		Dot-Clock Dela y
[1]	[0]	
0	0	No Delay
0	1	Delay is 1 Dot Clock
1	0	Delay is 2 Dot Clocks
1	1	Delay is 3 Dot Clocks

12.97 CR49: Vertical Size for Upper Half of Dual-Scan STN LCD s

I/O Port Address: 3?5

Index: 49

Bit	Description	Reset State
7(MSB)	Vertical Size for Upper Half of Dual-Scan STN LCDs [7]	0
6	Vertical Size for Upper Half of Dual-Scan STN LCDs [6]	0
5	Vertical Size for Upper Half of Dual-Scan STN LCDs [5]	0
4	Vertical Size for Upper Half of Dual-Scan STN LCDs [4]	0
3	Vertical Size for Upper Half of Dual-Scan STN LCDs [3]	0
2	Vertical Size for Upper Half of Dual-Scan STN LCDs [2]	0
1	Vertical Size for Upper Half of Dual-Scan STN LCDs [1]	0
0(LSB)	Vertical Size for Upper Half of Dual-Scan STN LCDs [0]	0

Bit	Descriptio n
7:0	**Vertical Size for Upper Half of Dual-Scan STN LCD s [7:0] :** • These bits are the least-significant 8 bits of a 9-bit field that defines the vertical size in scanlines. • The most-significant ninth bit of this field is in CR48[2]. • This vertical display position is relative to the start of the first vertical pulse, which is ahead of the actual vertical display when the centering feature is enabled (using Extension registers CR40 through CR43). • Up to 511 scanlines can be defined for display on the upper half of a dual-scan STN LCD. • The actual value in this register is one less than the lines displayed on the upper half of the LCD. For example, for an LCD using a: — 480-line mode, program 239, which is obtained as follows: (480 lines ÷ 2) = 240 lines being displayed on upper half of LCD display. Therefore, 240 - 1 = 239. — 600-line mode, program 299, which is obtained as follows: (600 lines ÷ 2) = 300 lines being displayed for upper half of LCD display. Therefore, 300 - 1 = 299. **NOTE:** The number of lines programmed in this register represents actual displayed lines.

12.98 CR4A: Vertical Size for LCD s

I/O Port Address: 3?5

Index: 4A

Bit	Description	Reset State
7(MSB)	Vertical Size for LCDs [7]	0
6	Vertical Size for LCDs [6]	0
5	Vertical Size for LCDs [5]	0
4	Vertical Size for LCDs [4]	0
3	Vertical Size for LCDs [3]	0
2	Vertical Size for LCDs [2]	0
1	Vertical Size for LCDs [1]	0
0(LSB)	Vertical Size for LCDs [0]	0

Bit	Descriptio n
7:0	**Vertical Size for LCDs [7:0] :** • These bits are the least-significant 8 bits of a 10-bit field that defines the overall vertical size in scanlines for the LCD, regardless of whether the LCD is dual scan or single scan. • The vertical display position is relative to: — The start of the vertical mid-point on dual-scan LCDs — The first vertical pulse on single-scan LCDs • The actual value in this register is two less than the total lines being displayed. (For example, for a 480-line display, program 478 lines.) • Dual-scan LCDs normally have the same amount of scanlines in both the upper and lower halves of the LCD. • The most-significant 2 bits of this field are in CR48[5:4].

12.99 CR4B: Reserved — Scratchpad Registe r

I/O Port Address: 3?5

Index: 4B

Bit	Description	Reset Stat e
7(MSB)	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	Reserved	
1	Reserved	
0(LSB)	Reserved	

This register is reserved for the exclusive use of the CL-GD7541/GD7543 BIOS and must never be written by any application program.

Bit	Descriptio n
7:0	**Reserved :** This register is used as a scratchpad register by the BIOS.

12.100 CR4C: Graphics Input-Resolution Override for Dithering

I/O Port Address: 3?5

Index: 4C

Bit	Description	Reset State
7(MSB)	Graphics Input-Resolution Override Enable	0
6	Reserved	
5	Reserved	
4	Reserved	
3	Graphics Input-Resolution Override [3]	0
2	Graphics Input-Resolution Override [2]	0
1	Graphics Input-Resolution Override [1]	0
0(LSB)	Graphics Input-Resolution Override [0]	0

This register, which is used with both TFT and STN LCDs, is used to change the CL-GD7541/GD7543 default input resolution settings for graphics data sent to the dither block. (For input resolution for MVA and the Video Overlay, refer to Extension register CR4E.)

- When the MVA is enabled, this override register affects only the surrounding area.
- The MVW display is controlled by independent input and output resolution control bits.
- This register supports a maximum of 6 × 6 dithering.

Bit **Description**

7 **Graphics Input-Resolution Override Enable:**

- When this bit is 0:
  - — The CL-GD7541/GD7543 has default input resolution settings for dithering that maximize the number of colors displayed on an LCD.
  - — The settings from Extension register HDR (the Hidden DAC register) apply, including the default input resolution settings shown in the table below:

Dithering Matrix	Default Input Resolution Settings
8 bits/gun	8-8-8 true-color mode
6 bits/gun	All VGA-compatibility color modes
	All extended color modes that go through the palette RAMDAC
	5-6-5 high-color mode (Video Overlay mode only, and not MVA)
5 bits/gun	5-5-5 direct-color mode
3 bits/gun	3-3-2 color mode (does not go through the palette RAMDAC)

12.100 CR4C: Graphics Input-Resolution Override for Dithering *(cont.)*

Bit	Description
7 *(cont.)*	**Graphics Input-Resolution Override Enable** *(cont.)*: • When this bit is 1: — The default input resolution settings are overridden, and new input resolution values are defined in CR4C[3:0]. — If the default input resolution settings are not desired, the BIOS can override them by programming any number between 0h and Fh. As a result, the CL-GD7541/GD7543 can dither more or less than the default case. — As long as the dithering matrix is smaller than or equal to 6 × 6, the CL-GD7541/GD7543 supports a combination of input and output resolutions.
6:4	**Reserved**
3:0	**Graphics Input-Resolution Override [3:0] :** • When the CR4C[7] override enable bit is 1, the CR4C[3:0] bits define the new input-resolution values for data sent to the dithering block. • The hex value programmed in these bits define the number of bits per gun that the CL-GD7541/GD7543 uses to control the dithering on an LCD, independent of the following: — The output resolution — The dithering state (enabled vs. disabled) — The CL-GD7541/GD7543 mode (graphics vs. text)

CR4C				Dithering Result for LCD
[3]	[2]	[1]	[0]	
0	0	1	1	3 bits/gun
0	1	0	0	4 bits/gun
0	1	0	1	5 bits/gun
0	1	1	0	6 bits/gun
0	1	1	1	7 bits/gun
1	0	0	0	8 bits/gun

12.100 CR4C: Graphics Input-Resolution Override for Ditherin g *(cont.)*

Bit	Descriptio n
3:0 *(cont.)*	**Graphics Input-Resolution Override [3:0] *(cont.)*:**

Example 1 :

When the given conditions are:

- Data comes from the 18-bit palette DAC CLUT as 6 bits/gun.
- Colors displayed are 256.
- There are 8 bits/pixel.
- LCD is a 3 bits/gun TFT.

Then:

- The CL-GD7541/GD7543 default input resolution is 6 bits/gun.
- The CL-GD7541/GD7543 output resolution is 3 bits/gun.
- When 2 × 2 dithering is enough:
  - — The 6 bits/gun default input resolution is overridden with one of 5 bits/gun.
  - — Since 5 bits/gun – 3 bits/gun = 2 bits/gun, this leads to a 2 × 2 dithering and the equivalent of 5 bits/gun (2^5 = 32 colors per gun, or 32K colors).
- When 256K colors is not enough and a better effect is desired:
  - — More dithering is possible by programming an input resolution of 7 bits/gun.
  - — Since 7 bits/gun – 3 bits/gun = 4 bits/gun, this leads to a 4 × 4 dithering and the equivalent of 7 bits/gun (2^7 = 128 colors per gun, or 2M colors).

Example 2 :

When the given conditions are:

- Colors displayed are 16.
- There are 8 bits/pixel.
- LCD is a color STN.
- The output resolution is programmed as 4 bits/gun (2^4 = 16).

Then:

- The CL-GD7541/GD7543 default input resolution is 6 bits/gun. (Combining 2^4 = 16 colors with 2^2 = 4 color dithering results in $2^4 \times 2^2 = 2^6$ = 6 bits/gun.)
- By changing the output resolution to 3 bits/gun, the CL-GD7541/GD7543 generates 2^3 = 8 colors.
- When the input resolution is 6 bits/gun, the CL-GD7541/GD7543 does more dithering to get 6 bits/gun.
- When the input resolution is 4 bits/gun, the CL-GD7541/GD7543 needs only 1 × 1 dithering to get a total of 16 equivalent colors per gun.

12.101 CR4D: Output Resolution for Ditherin g

I/O Port Address: 3?5

Index: 4D

Bit	Description	Reset State
7(MSB)	MVA/Video Overlay Output Resolution for Dithering [3]	0
6	MVA/Video Overlay Output Resolution for Dithering [2]	0
5	MVA/Video Overlay Output Resolution for Dithering [1]	0
4	MVA/Video Overlay Output Resolution for Dithering [0]	0
3	Output Resolution for Dithering [3]	0
2	Output Resolution for Dithering [2]	0
1	Output Resolution for Dithering [1]	0
0(LSB)	Output Resolution for Dithering [0]	0

Bit **Descriptio n**

7:4 **MVA and Video Overlay Output Resolution for Dithering [3:0]:**

- These bits define the output resolution value for dithering exactly in the same way as CR4D[3:0], except they apply to the MVW and/or to the Feature Connector Video Overlay.
- For the CL-GD7543, *both* the MVA and Video Overlay resolution functions apply. (These bits are active even when the MVW displays on the entire screen.)
- For the CL-GD7541, *only* the Video Overlay resolution function applies.

3:0 **Output Resolution for Dithering [3:0]:**

These bits define typical output resolution values for dithering various LCDs. The hex value programmed in these bits define the number of bits per gun used by the CL-GD7541/GD7543.

CR4D				Output Resolution for Dithering LCDs :	
[3]	[2]	[1]	[0]	TFT LCDs (No Frame-Rate Modulation)	STN LCDs (Frame-Rate Modulation Occurs)
0	0	0	1	Not applicable	2-shade STN LCDs: 1 bit/gun
0	0	1	0	Not applicable	4-shade STN LCDs: 2 bits/gun
0	0	1	1	3 bits/gun	8-shade STN LCDs: 3 bits/gun
0	1	0	0	4 bits/gun	16-shade STN LCDs: 4 bits/gu n
0	1	1	0	6 bits/gun	Not applicable
1	0	0	0	8 bits/gun	Not applicable

NOTE: Programming values other than the ones specified in the above table may have unpredictable results. Also, the system reset value of zero is not a valid value. Therefore, **this register must be programmed at start-up with the correct output resolution for the LCD used (TFT or STN) .**

12.102 CR4E: MVA/Video Overlay Input-Resolution Overrid e

I/O Port Address: 3?5

Index: 4E

Bit	Description	Reset State
7(MSB)	MVA/Video Overlay Input-Resolution Override Enable	0
6	MVA Dithering Enable	0
5	Video Overlay Dithering Enable	0
4	Reserved	
3	MVA/Video Overlay Input-Resolution Override [3]	0
2	MVA/Video Overlay Input-Resolution Override [2]	0
1	MVA/Video Overlay Input-Resolution Override [1]	0
0(LSB)	MVA/Video Overlay Input-Resolution Override [0]	0

This register is used to change the CL-GD7541/GD7543 default resolution settings for the video data sent to the dither block, either for the MVA window only, or for when the MVA fills the entire screen.

Bit **Descriptio n**

7 **MVA/Video Overlay Input-Resolution Override Enabl e:**

- When this bit is 0:
  - — The input resolution for video data is controlled by Extension register HDR (the Hidden DAC register) through the MVA or Video Overlay data paths.
  - — The default input resolution settings shown in the table below apply.

Dithering Matri x	Default Input Resolution Setting s
8 bits/gun	8-8-8 true-color mode
6 bits/gun	All VGA-compatibility color mode s
	All extended color modes that go through the palette RAMDA C
5 bits/gun	5-5-5 direct-color mode
3 bits/gun	3-3-2 color mode (does not go through the palette RAMDAC)

- When this bit is 1:
  - — Extension register CR4E[3:0] controls the input resolution for video.
    - — For the CL-GD7541, the video input resolution for only the Video Overlay Window is affected.
    - — For the CL-GD7543, the video input resolution for both the Video Overlay Window and MVA are affected.
  - — The default input resolution settings for the MVA are overridden, and new values are defined in bits CR4E[3:0] of this register.

12.102 CR4E: MV A/Video Overlay Input-Resolution Override *(cont.)*

Bit — **Descriptio n**

6

MVA Dithering Enable (CL-GD754 3 Only):
This bit applies only to the CL-GD7543. When this bit is:
- 0, MVA dithering is disabled.
- 1, MVA dithering is enabled.

5

Video Overlay Dithering Enable (CL-GD754 1 and CL-GD754 3):
When this bit is:
- 0, the Video Overlay Window is dithered exactly as in graphics modes. The color key and the OVRW# signal define the Video Overlay Window.
- 1, Video Overlay dithering is enabled.
  - — Feature Connector Video Overlay data is dithered, based on the input resolution in CR4E[3:0] and the output resolution in CR4D[7:4].
  - — Unlike MVA and graphics modes, Video Overlay does not have an override for input resolution. Instead, the input resolution is always the one in CR4E[3:0].

4

Reserve d

3:0

MVA/Video Overlay Input-Resolution Override [3:0] :
When the CR4E[7] override enable bit is 1, the CR4E[3:0] bits define the new input-resolution values for data sent to the dithering block, so that the amount of colors in MVW can differ from the surrounding area.
- The hex value programmed can be any number between 1h and Fh. For details, refer to Extension register CR4C[3:0]. All explanations apply, exceptthat:
  - — For the CL-GD7543, the effect applies to *both* the MVW and the Video Overlay Window.
  - — For the CL-GD7541, the effect applies to *only* the Video Overlay Window.
- The value programmed in these bits define the number of bits per gun thatthe CL-GD7541/GD7543 uses to control the dithering on an LCD, independent of:
  - — The output resolution
  - — The dithering state (enabled vs. disabled)
  - — The CL-GD7541/GD7543 mode (graphics vs. text)

CR4E				Dithering Result for LC D
[3]	[2]	[1]	[0]	
0	0	1	1	3 bits/gun (3:3:2 RGB)
0	1	0	1	5 bits/gun (5:5:5 RGB)
0	1	1	0	6 bits/gun (all palettized modes)
0	1	1	1	7 bits/gun
1	0	0	0	8 bits/gun. Includes: 8-8-8 RGB mode and YUV 4-2-2

12.103 HDR: Hidden DAC Register

I/O Port Address: 3C6

Index: (n/a)

Bit	Description	Reset Stat e
7	5-5-5 Extended Color Mode Enable	0
6	Extended Color Mode Select Enable	0
5	Clocking Mode	0
4	32K Extended Color Mode Control	0
3	Extended Color Mode Select [3]	0
2	Extended Color Mode Select [2]	0
1	Extended Color Mode Select [1]	0
0	Extended Color Mode Select [0]	0

The Hidden DAC register (HDR):

- Is used to enable extended color modes, including the following:
  - — 15-bit/pixel extended color mode
  - — 16-bit/pixel extended color mode
  - — 24-bit/pixel extended color mode
- Is accessed by reading four times in succession External/General register 3C6 (the Pixel Mask register). The next write or read of the 3C6 register then accesses the HDR.
  - — A *write* to the HDR resets the internal counter, and the four dummy reads of the 3C6 register must be executed again.
  - — A *read* from the HDR resets the internal counter, and the four dummy reads of the 3C6 register must be executed again.
  - — Reads from the 3C6 register do not lock the HDR.
- Is cleared to all zeroes at reset, putting the CL-GD7541/GD7543 in VGA-compatibility mode.
- Does not affect MVA modes.

Bit	Descriptio n
7	**5-5-5 Extended Color Mode Enable :** • When this bit is 0: — The extended color modes are disabled. — The palette DAC is VGA-compatible. • When this bit is 1: — It enables the extended color modes (including the 5-5-5 extended color mode), as chosen by bit [6] and bits [3:0] of this register.
6	**Extended Color Mode Select Enable :** When bit [7] is 1, and this bit is: • 0, the extended color mode select bits [3:0] of this register are ignored, and the extended color mode is the 5-5-5 mode. • 1, the extended color mode select bits [3:0] of this register are enabled to select an extended color mode (other than the 5-5-5 mode).

12.103 HDR: Hidden DAC Register *(cont.)*

Bit — **Description**

5 — **Clocking Mode:**

- When this bit is 0, Clocking mode 1 is chosen. In Clocking mode 1:
  - 16-bit/pixel modes use both edges of DCLK to latch data.
  - The rising edge of DCLK latches the least-significant byte.
  - The falling edge of DCLK latches the most-significant byte.
- When this bit is 1, Clocking mode 2 is chosen. In Clocking mode 2:
  - 16-bit/pixel modes use only the rising edge of DCLK to latch data.
  - The DCLK must be supplied at twice the pixel rate.
  - The first rising edge of DCLK latches the least-significant byte.
  - The second rising edge of DCLK latches the most-significant byte.

NOTE: All modes other than 16-bit/pixel use only the rising DCLK edge, regardless of this bit setting.

4 — **32K Extended Color Mode Control:**

When this bit is:

- 0, a 5-5-5 extended color mode operation takes place normally.
- 1 *and* the 15th pixel data bit of the 5-5-5 operation is:
  - 0, then the 5-5-5 extended color mode operation that is chosen allows 5-5-5 data to overlay 256-color images on a pixel-by-pixel basis.
  - 1, then the first 8 pixel data bits of the 5-5-5 operation choose a palette entry and the last 7 pixel data bits are ignored.

3:0 — **Extended Color Mode Select [3:0]:**

When HDR[7:6] is 11, this 4-bit field selects an extended color mode according to the following table:

HDR						Color Mode	
[7]	[6]	[3]	[2]	[1]	[0]		
0	X	X	X	X	X	VGA compatibility color mode	
1	0	X	X	X	X	Extended color modes	5-5-5
1	1	0	0	0	1		5-6-5 XGA
1	1	0	1	0	1		8-8-8 16M color
1	1	0	1	1	X		DAC power-down
1	1	1	0	0	0		8-bit grayscale
1	1	1	0	0	1		3-3-2 8-bit RGB

NOTE: Any undefined settings are reserved.

12.104 R2X: LCD Timing Register — LFS Vertical Position #1 (MISC[7:6] Is 11)

I/O Port Address: 3?5

Index: 2 — This register is accessible only when Extension register CR2D[7] is 1.

Bit	Description	Access	Reset Sta te
7(MSB)	LFS Vertical Position [7]	R/W	0
6	LFS Vertical Position [6]	R/W	0
5	LFS Vertical Position [5]	R/W	0
4	LFS Vertical Position [4]	R/W	0
3	LFS Vertical Position [3]	R/W	0
2	LFS Vertical Position [2]	R/W	0
1	LFS Vertical Position [1]	R/W	0
0(LSB)	LFS Vertical Position [0]	R/W	0

Register R2X (and registers R3X, R4X, R5X, and RCX, with overflow bits in R6X and REX) define in scanlines the vertical position of the line frame start signal (LFS), relative to the CRT frame start signal.

- At power-on self-test, these registers are programmed according to the size of LCD used
- Which registers are automatically selected depends upon the following:
  - — The expansion and centering options selected.
  - — The setting of MISC[7:6].
  - — The resolution modes selected. (For selection options, refer to Table 12-3.)

Bit	Descriptio n
7:0	**LFS Vertical Position #1 [7:0] :** • These bits are the least-significant 8 bits of a 10-bit field. The field's value defines in scanlines the vertical position of the line frame start (LFS) signal, relative to the CRT frame start signal. • The most-significant 2 bits of this field are stored in register R6X[7:6]. • For 640 × 480 LCDs, the R2X field is used for 480-line modes when: — CR2D[1] is 0 (automatic vertical expansion is disabled). — CR2D[0] is 0 (automatic centering is disabled). — External/General register MISC[7:6] is 11 (480 lines are displayed). • For 640 × 480 LCDs, the R2X field is used for *all* resolution modes when: — CR2D[1] is 1 (automatic vertical expansion is enabled). — CR2D[0] is 0 (automatic centering is disabled). — External/General register MISC[7:6] is XX ('don't care'). • For 800 × 600 LCDs, the R2X field is also used when: — CR2D[1] is 1 (automatic vertical expansion is enabled). — CR2D[0] is 0 (automatic centering is disabled). — External/General register MISC[7:6] is any value *except* 10 (the 350-line display resolution mode option). • For LFS vertical position selection logic diagrams, refer to Figure 12-5.

12.104 R2X: LCD Timing Register s *(cont.)*

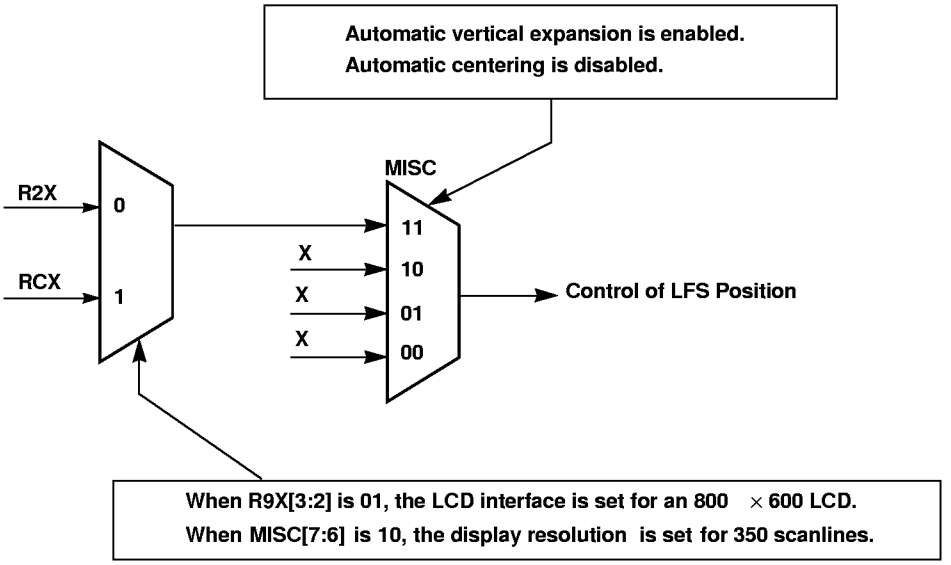
Table 1 2-3. LFS Register Selection Option s

Conditions:					Result:
LCD Size Is:	**Automatic Vertical Expansion[a] Is:**	**Automatic Centering Is:**	**MISC [7:6] =**	**Display Resolution Modes (in Scanlines)**	**LFS Vertical Position Registers Selected**
640 × 480	Off (CR2D[1] is 0)	On (CR2D[0] is 1)	11	480 scanlines	R2X[7:0] and R6X[7:6]
640 × 480	On (CR2D[1] is 1)	Off (CR2D[0] is 0)	XX	All display resolution modes	R2X[7:0] and R6X[7:6]
800 × 600	Off (CR2D[1] is 0)	On (CR2D[0] is 1)	01	400 scanlines	R4X[7:0] and R6X[3:2]
800 × 600	Off (CR2D[1] is 0)	On (CR2D[0] is 1)	00	600 scanlines	R5X[7:0] and R6X[1:0]
800 × 600	On (CR2D[1] is 1)	'Don't care'	11	All display resolution modes *except* for 350 scanlines	R2X[7:0] and R6X[7:6]
			01		
			00		
800 × 600	On (CR2E[1] is 1 and graphics expansion is enabled or CR2E[0] is 1 and text expansion is enabled)	'Don't care'	10	350 scanlines	RCX[7:0] and REX[1:0]
640 × 480 or 800 × 600	Off (CR2D[1] is 0)	On (CR2D[0] is 1)	10	350 scanlines	R3X[7:0] and R6X[5:4]
640 × 480 or 800 × 600	Off (CR2D[1] is 0)	On (CR2D[0] is 1)	01	400 scanlines	R4X[7:0] and R6X[3:2]

[a] Depending on the LCD size selected, automatic vertical expansion is controlled by different registers .

12.104 R2X: LCD Timing Register s *(cont.)*

The following logic diagrams apply to registers R2X to R5X and RCX.



NOTE: For 800 × 600 and 640 × 480 LCDs, the vertical expansions are controlled by different bits, and the expansion algorithms are different.

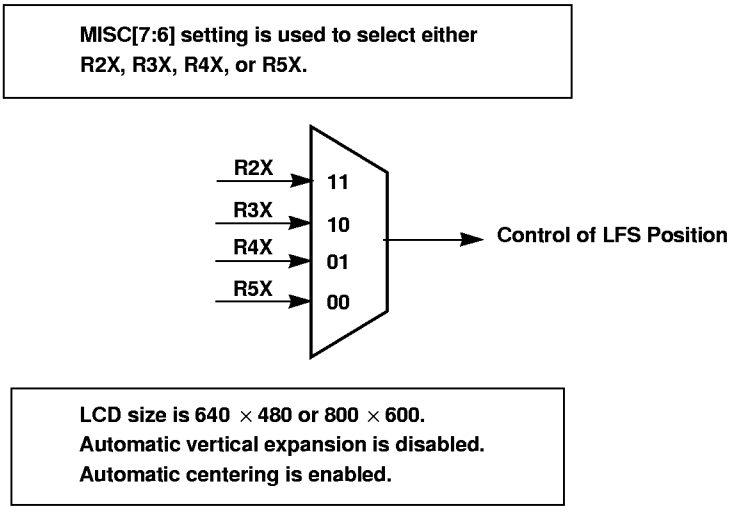


Figure 1 2-5. Logic Diagrams for LFS Vertical Position Selectio n

12.105 R3X: LCD Timing Register — LFS Vertical Position #2 (MISC[7:6] Is 10)

I/O Port Address: 3?5

Index: 3 — This register is accessible only when Extension register CR2D[7] is 1.

Bit	Description	Access	Reset Sta te
7(MSB)	LFS Vertical Position #2 [7]	R/W	0
6	LFS Vertical Position #2 [6]	R/W	0
5	LFS Vertical Position #2 [5]	R/W	0
4	LFS Vertical Position #2 [4]	R/W	0
3	LFS Vertical Position #2 [3]	R/W	0
2	LFS Vertical Position #2 [2]	R/W	0
1	LFS Vertical Position #2 [1]	R/W	0
0(LSB)	LFS Vertical Position #2 [0]	R/W	0

This register defines in scanlines the vertical position of the line frame start signal (LFS), relative to the CRT frame start signal, under the conditions explained below.

Bit	Descriptio n
7:0	**LFS Vertical Position #2 [7:0] :** • These bits are the least-significant 8 bits of a 10-bit value that defines in scan-lines the vertical position of the LFS signal, relative to the CRT frame start sig-nal, when: — External/General register MISC[7:6] is 10 (350 lines are displayed). — Extension register CR2D[1] is 0 (automatic vertical expansion is disabled). — Extension register CR2D[0] is 1 (automatic centering is enabled, when CR2D[1] is 0). • The most-significant 2 bits are stored in Extension register R6X[5:4]. • For selection options, refer to Table 12-3.

12.106 R4X: LCD Timing Register — LFS Vertical Position #3 (MISC[7:6] Is 01)

I/O Port Address: 3?5

Index: 4 — This register is accessible only when Extension register CR2D[7] is 1.

Bit	Description	Access	Reset Sta te
7(MSB)	LFS Vertical Position #3 [7]	R/W	0
6	LFS Vertical Position #3 [6]	R/W	0
5	LFS Vertical Position #3 [5]	R/W	0
4	LFS Vertical Position #3 [4]	R/W	0
3	LFS Vertical Position #3 [3]	R/W	0
2	LFS Vertical Position #3 [2]	R/W	0
1	LFS Vertical Position #3 [1]	R/W	0
0(LSB)	LFS Vertical Position #3 [0]	R/W	0

This register defines in scanlines the vertical position of the line frame start signal (LFS), relative to the CRT frame start signal, under the conditions explained below.

Bit	Descriptio n
7:0	**LFS Vertical Position #3 [7:0]:** • These bits are the least-significant 8 bits of a 10-bit value that defines in scan-lines the vertical position of the LFS signal, relative to the CRT frame start sig-nal, when: — External/General Register MISC[7:6] is 01 (400 lines are displayed). — Extension Register CR2D[1] is 0 (automatic vertical expansion is disabled). — Extension Register CR2D[0] is 1 (automatic centering is enabled, when CR2D[1] is 0). • The most-significant 2 bits are stored in Extension register R6X[3:2]. • For selection options, refer to Table 12-3.

12.107 R5X: LCD Timing Register — LFS Vertical Position #4 (MISC[7:6] Is 00)

I/O Port Address: 3?5

Index: 5 — This register is accessible only when Extension register CR2D[7] is 1.

Bit	Description	Access	Reset Sta te
7(MSB)	LFS Vertical Position #4 [7]	R/W	0
6	LFS Vertical Position #4 [6]	R/W	0
5	LFS Vertical Position #4 [5]	R/W	0
4	LFS Vertical Position #4 [4]	R/W	0
3	LFS Vertical Position #4 [3]	R/W	0
2	LFS Vertical Position #4 [2]	R/W	0
1	LFS Vertical Position #4 [1]	R/W	0
0(LSB)	LFS Vertical Position #4 [0]	R/W	0

This register defines in scanlines the vertical position of the line frame start signal (LFS), relative to the CRT frame start signal, under the conditions explained below.

Bit	Descriptio n
7:0	**LFS Vertica l Position #4 [7:0]:** • These bits are the least-significant 8 bits of a 10-bit value that defines in scan-lines the vertical position of the LFS signal, relative to the CRT frame start sig-nal, when: — External/General register MISC[7:6] is 00. — Extension register CR2D[1] is 0 (automatic vertical expansion is disabled). — Extension register CR2D[0] is 1 (automatic centering is enabled, when CR2D[1] is 0). • The most-significant 2 bits are stored in Extension register R6X[1:0]. • For selection options, refer to Table 12-3.

12.108 R6X: LCD Timing — Overflow Bits for LFS Signal Compar e

I/O Port Address: 3?5

Index: 6 — This register is accessible only when Extension register CR2D[7] is 1.

Bit	Description	Access	Reset Sta te
7(MSB)	R2X LFS Vertical Position #1 [9]	R/W	0
6	R2X LFS Vertical Position #1 [8]	R/W	0
5	R3X LFS Vertical Position #2 [9]	R/W	0
4	R3X LFS Vertical Position #2 [8]	R/W	0
3	R4X LFS Vertical Position #3 [9]	R/W	0
2	R4X LFS Vertical Position #3 [8]	R/W	0
1	R5X LFS Vertical Position #4 [9]	R/W	0
0(LSB)	R5X LFS Vertical Position #4 [8]	R/W	0

This register defines the two most-significant overflow bits for the LFS vertical position registers R2X, R3X, R4X, and R5X.

Bit	Descriptio n
7:6	**R2X LFS Vertical Position #1 [9:8]**: When External/General register MISC[7:6] is 11, these bits are the most-significant 2 bits of Extension register R2X, creating a 10-bit value.
5:4	**R3X LFS Vertical Position #2 [9:8]**: When External/General register MISC[7:6] is 10, these are the most-significant 2 bits of Extension register R3X, creating a 10-bit value.
3:2	**R4X LFS Vertical Position #3 [9:8]**: When External/General register MISC[7:6] is 01, these are the most-significant 2 bits of Extension register R4X, creating a 10-bit value.
1:0	**R5X LFS Vertical Position #4 [9:8]**: When External/General register MISC[7:6] is 00, these are the most-significant 2 bits of Extension register R5X, creating a 10-bit value.

12.109 R7X: LCD Timing Register — Signal Control for Color TFT LCD s

I/O Port Address: 3?5

Index: 7 — This register is accessible only when Extension register CR2D[7] is 1.

Bit	Description	Access	Reset Stat e
7(MSB)	Reserved		
6	Reserved		
5	Reserved		
4	Reserved		
3	LFS Output	R/W	0
2	LLCLK Output	R/W	0
1	FPVDCLK Inversion	R/W	0
0(LSB)	FPVDCLK Free-Running Enable for TFT LCDs	R/W	0

Bit	Descriptio n
7:4	**Reserve d**
3	**LFS Output :** In both of the following cases, the line frame start signal (LFS) output is controlled by the first vertical pulse, which marks the beginning of the LCD display. • When this bit is 0: — The LFS output pin drives both STN and DE-type TFT LCDs. — The LFS output (which may also be called FLM) is one line wide and is programmable. • When this bit is 1: — The LFS output pin drives the VSYNC input for non-DE-type TFT LCDs. — The LFS output (which may also be called TFT-VSYNC) is two lines wide and can support only single-scan LCDs. • Set this bit to 1 for any TFT LCDs that require a VSYNC input wider than one line.

12.109 R7X: LCD Timing Register — Signal Control for Color TFT LCDs *(cont.)*

Bit	Description
2	**LLCLK Output:** • When this bit is 0: — The LLCLK output pin drives both STN and DE-type TFT LCDs. — The LLCLK signal position is controlled by 'LCD Horizontal Display Enable Start' values stored in Extension registers CR40 to CR42, and Extension register CR43 is used for fine positioning. — The LLCLK signal starts with the HFirst pulse. (Refer to the timing diagram within the description of Extension register CR40.) — The LLCLK signal is always 25 dot clocks before the LCD display enable start signal. • When this bit is 1: — Connect LFS to VSYNC. (Refer to Extension register R7X[3].) • This bit *must* be set to 1 for: — Non-DE-type TFT LCDs. — LCDs that require an offset different than 25 dot clocks between the LLCLK (or LCD HSYNC) signal and the LCD display enable start signal. For example, some LCDs require an offset of 144 dot clocks between LLCLK and the first LCD shift clock. In this case, set R7X[2] is 1, which places the LLCLK output under the control of Extension register CR47[7:0].
1	**FPVDCLK Inversion:** This bit can be used with all LCDs. • When this bit is: — 1, the FPVDCLK signal is inverted, and LCD data must be latched on the low-to-high transition of FPVDCLK. — 0, the FPVDCLK signal is not inverted, and LCD data must be latched on the high-to-low transition of FPVDCLK. • During Suspend mode, FPVDCLK is forced low, independent of this bit polarity.
0	**FPVDCLK Free-Running Enable for TFT LCDs:** Set this bit to: • 1 for TFT LCDs that require a free-running FPVDCLK (that is, a clock that constantly toggles). — When this bit is 1 *and* when the LCD power sequence is on, FPVDCLK is always active (free-running) for TFT LCDs. — This setting is the usual setting. • 0 for TFT LCDs that cannot accept a free-running FPVDCLK. — When this bit is 0, FPVDCLK is gated by the display enable signal and remains active only during display time. — This setting is generally not required.

12.110 R8X: LCD Timing Register — Shift Clock and Data Format Select for STN LCD s

I/O Port Address: 3?5

Index: 8 — This register is accessible only when Extension register CR2D[7] is 1.

Bit	Description	Access	Reset Stat e
7(MSB)	Horizontal Cross-Talk Reduction Enable	R/W	0
6	Vertical Cross-Talk Reduction Disable	R/W	0
5	Dual-/Single-Scan Monochrome LCD Select	R/W	0
4	Foreground-Only Text Enhancement	R/W	0
3	Reserved		
2	Reserved		
1	Dual/Single Shift-Clock Select for STN LCDs	R/W	0
0(LSB)	16-Bit / 8-Bit Data-Interface Select for STN LCDs	R/W	0

Bit	Descriptio n
7	**Horizontal Cross-Talk Reduction Enable:** When this bit is 1, horizontal cross-talk reduction is enabled. This bit is a test bit, and it must never be written by any application program. It is listed here only for completeness.
6	**Vertical Cross-Talk Reduction Disable:** When this bit is 1, vertical cross-talk reduction is disabled. This bit is a test bit, and it must never be written by any application program. It is listed here only for completeness.
5	**Dual-/Single-Scan Monochrome LCD Selec t:** When this bit is: • 0, dual-scan monochrome LCDs are selected. • 1, single-scan monochrome LCDs are selected.
4	**Foreground-Only Text Enhancement :** • When this bit is 0, normal text is displayed. • When this bit is 1, *and* Extension register CR1E[1] is 1, the foreground-only text enhancement is enabled.
3:2	**Reserve d**
1	**Dual/Single Shift-Clock Select for STN LCDs:** On an STN LCD, when this bit is: • 0, a single-shift clock is supplied to the FPVDCLK pin. • 1, a dual-shift clock is supplied to the FPVDCLK and FPDE pins.
0	**16-Bit / 8-Bit Data-Interface Select fo r STN LCDs:** On an STN LCD, when this bit is: • 0, a 16-bit data STN LCD interface is selected. • 1, an 8-bit data STN LCD interface is selected. **NOTE:** For 8-bit STN LCDs that are dual-clock, single-scan, and interleaved, only R8X[0] needs to be programmed, and not R8X[1].

12.111 R9X: LCD Size and TFT LCD Data Format Register

I/O Port Address: 3?5

Index: 9 — This register is accessible only when Extension register CR2D[7] is 1.

Bit	Description	Access	Reset State
7(MSB)	Reserved		
6	Reserved		
5	Reserved		
4	Reserved		
3	LCD Size [1]	R/W	0
2	LCD Size [0]	R/W	0
1	TFT LCD Data Format [1]	R/W	0
0(LSB)	TFT LCD Data Format [0]	R/W	0

Bit **Description**

7:4 **Reserved**

3:2 **LCD Size [1:0] :**
These 2 bits select an LCD size as shown in the table below. For details on specific LCD types and connection information, refer to the "Panel Interface Guide" in the *CL-GD754X Application Book*.

R9X		LCD Size	LCD Types to Which LCD Size Can Be Applied
[3]	[2]		
0	0	640 × 480	STN and TFT
0	1	800 × 600	STN and TFT
1	0	Reserved	–
1	1	Reserved	–

1:0 **TFT LCD Data Format [1:0]**:
These 2 bits select the data format for TFT LCDs as shown in the table below. For information on specific LCD types and for detailed connection information, refer to the "Panel Interface Guide" in the *CL-GD754X Application Book*.

R9X		TFT LCD Data Format	Corresponding Cirrus Logic Abbreviation for TFT LCD Data Format
[1]	[0]		
0	0	9-bit (333)	C512SS-9
0	1	12-bit (444)	C4KSS-12
1	0	18-bit (666)	C256K-18
1	1	24-bit (888)	C16MSS-24

12.112 RBX: Shade Conversio n and Extra LCD Line Clock Insertio n Registe r

I/O Port Address: 3?5

Index: B — This register is accessible only when Extension register CR2D[7] is 1.

Bit	Description	Access	Reset Stat e
7(MSB)	Reserved		
6	Reserved		
5	Reserved		
4	Shades 7 and 9 Convert	R/W	0
3	Shades 5 and 11 Convert	R/W	0
2	Extra LCD Line Clock Enable [2]	R/W	0
1	Extra LCD Line Clock Enable [1]	R/W	0
0(LSB)	Extra LCD Line Clock Enable [0]	R/W	0

Bit — **Descriptio n**

7:5 — **Reserve d**

4 — **Shades 7 and 9 Convert :**
When this bit is 1:
- Shade 7 is converted to shade 6.
- Shade 9 is converted to shade 8.

3 — **Shades 5 and 11 Conver t:**
When this bit is 1:
- Shade 5 is converted to shade 4.
- Shade 11 is converted to shade 10.

2:0 — **Extra LCD Line Clock (LLCLK) Enable [2:0]:**
The hex value in these 3 bits define up to five extra LCD line clocks, which can be inserted between the upper and lower half of a dual-scan LCD.
- Extra line clocks are needed for those LCD manufacturers who disconnect the first one or two row drivers on the lower half of a dual-scan LCD.
- These bits generate extra line clocks for disconnected row drivers

RBX			Result
[2]	[1]	[0]	
0	0	0	0 extra LCD line clocks
0	0	1	1 extra LCD line clock
0	1	0	2 extra LCD line clocks
0	1	1	3 extra LCD line clocks
1	0	0	4 extra LCD line clocks
1	0	1	5 extra LCD line clocks

12.113 RCX: LFS Vertical Position for 525-Line Modes Register

I/O Port Address: 3?5

Index: C — This register is accessible only when Extension register CR2D[7] is 1.

Bit	Description	Reset State
7	LFS Vertical Position for 525-Line Modes [7]	0
6	LFS Vertical Position for 525-Line Modes [6]	0
5	LFS Vertical Position for 525-Line Modes [5]	0
4	LFS Vertical Position for 525-Line Modes [4]	0
3	LFS Vertical Position for 525-Line Modes [3]	0
2	LFS Vertical Position for 525-Line Modes [2]	0
1	LFS Vertical Position for 525-Line Modes [1]	0
0	LFS Vertical Position for 525-Line Modes [0]	0

For 800 × 600 LCDs, this register is used to:

- Expand the 350 scanlines that result from a 350-line mode to 525 scanlines and then to center the 525 scanlines
- Define in scanlines the vertical position of the line frame start signal (LFS), relative to the CRT frame start signal, under the conditions explained below.

Bit	Description
7:0	**LFS Vertical Position for 525-Line Modes [7:0]:** • These bits are the least-significant 8 bits of a 10-bit value that defines in scanlines the vertical position of the LFS signal, relative to the CRT frame start signal, when: — The LCD is a 525-line LCD, or the LCD is one that uses a 525-line mode that has been expanded to 600 lines. — External/General register MISC[7:6] is 10 (350 lines are displayed). — Graphics modes 10h or Fh are being used. (These modes display 350 lines.) — Extension register CR2D[1] is 1 (automatic vertical expansion is enabled). • The most-significant 2 bits of this field are in REX[1:0]. • For selection options refer to Table 12-3.

12.114 RDX: LCD Timing Register — LFS Vertical Position # 6

I/O Port Address: 3?5

Index: D — This register is accessible only when Extension register CR2D[7] is 1.

Bit	Description	Access	Reset Stat e
7	LFS Vertical Position #6 [7]	R/W	0
6	LFS Vertical Position #6 [6]	R/W	0
5	LFS Vertical Position #6 [5]	R/W	0
4	LFS Vertical Position #6 [4]	R/W	0
3	LFS Vertical Position #6 [3]	R/W	0
2	LFS Vertical Position #6 [2]	R/W	0
1	LFS Vertical Position #6 [1]	R/W	0
0(LSB)	LFS Vertical Position #6 [0]	R/W	0

For 800 × 600 LCDs, this register is used to define in scanlines the vertical position of the line frame start signal (LFS), relative to the CRT frame start signal, under the conditions explained below.

Bit	Descriptio n
7:0	**LFS Vertical Position #6 [7:0]:** • These bits are the least-significant 8 bits of a 10-bit value that defines in scan-lines the vertical position of the LFS signal, relative to the CRT frame start sig-nal, when: — The LCD is an 800 × 600 LCD. — External/General register MISC[7:6] is 11. — Extension register CR2D[1] is 0 (automatic vertical expansion is disabled). — Extension register CR2D[0] is 1 (automatic centering is enabled). • The most-significant 2 bits are stored in REX[3:2]. • For selection options refer to Table 12-3.

12.115 REX: RDX and RCX Overflow Register

I/O Port Address: 3?5

Index: E — This register is accessible only when Extension register CR2D[7] is 1.

Bit	Description	Access	Reset State
7	Reserved		
6	Reserved		
5	Reserved		
4	Reserved		
3	RDX: LFS Vertical Position #6 [9]	R/W	0
2	RDX: LFS Vertical Position #6 [8]	R/W	0
1	RCX: LFS Vertical Position for 525-Line Modes [9]	R/W	0
0	RCX: LFS Vertical Position for 525-Line Modes [8]	R/W	0

Bit	Description
7:4	**Reserved**
3:2	**RDX LFS Vertical Position #6 [9:8]:** • These overflow bits are the most-significant 2 bits of a 10-bit field, LFS Vertical Position #6. • For more information, refer to Extension register RDX[7:0], which contains the least-significant bits for this field.
1:0	**RCX LFS Vertical Position for 525-Line Modes [9:8]:** • These overflow bits are the most-significant 2 bits of a 10-bit field, LFS Vertical Position for 525-line modes. • For more information, refer to Extension register RCX[7:0], which contains the least-significant bits for this field.

12.116 R0Y: Horizontal Total Shadow Registe r

I/O Port Address: 3?5

Index: This register is accessible only when Extension Register CR2C[5:4] is 10.

Bit	Description	Reset Stat e
7	Horizontal Total [7]	0
6	Horizontal Total [6]	0
5	Horizontal Total [5]	0
4	Horizontal Total [4]	0
3	Horizontal Total [3]	0
2	Horizontal Total [2]	0
1	Horizontal Total [1]	0
0	Horizontal Total [0]	0

The RiY (i = 0,2,3,4,5) Extension registers are horizontal timing shadow registers.

- These registers are used to automatically control the CRT controller on 640× 480 and 800 × 600 LCDs, for both low-resolution and high-resolution applications.
- These registers control LCD timing independent of VGA modes.

Bit	Descriptio n
7:0	**Horizontal Total [7:0] :** When Sequencer register SR1[3] is 0 (the DCLK signal is the same signal as VCLK), this register performs the same function as CRT Controller register CR0[7:0]).

12.117 R2Y: Horizontal Blanking Start Shadow Registe r

I/O Port Address: 3?5

Index: This register is accessible only when Extension register CR2C[5:4] is 10.

Bit	Description	Reset Stat e
7	Horizontal Blanking Start [7]	0
6	Horizontal Blanking Start [6]	0
5	Horizontal Blanking Start [5]	0
4	Horizontal Blanking Start [4]	0
3	Horizontal Blanking Start [3]	0
2	Horizontal Blanking Start [2]	0
1	Horizontal Blanking Start [1]	0
0	Horizontal Blanking Start [0]	0

Bit	Descriptio n
7:0	**Horizontal Blanking Star t [7:0] :** When Sequencer register SR1[3] is 0 (the DCLK signal is the same signal as VCLK), this register performs the same function as CRT Controller register CR2[7:0].

12.118 R3Y: Horizontal Blanking End Shadow Register

I/O Port Address: 3?5

Index: This register is accessible only when Extension register CR2C[5:4] is 10.

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Horizontal Blanking End [4]	0
3	Horizontal Blanking End [3]	0
2	Horizontal Blanking End [2]	0
1	Horizontal Blanking End [1]	0
0	Horizontal Blanking End [0]	0

Bit	Description
7:5	**Reserved**
4:0	**Horizontal Blanking End [4:0] :** When Sequencer register SR1[3] is 0 (the DCLK signal is the same signal as VCLK), this register performs the same function as CRT Controller register CR3[4:0]. • These bits are the least-significant 5 bits of a 6-bit word controlling the horizontal blanking end signal. • The most-significant bit that controls the horizontal blanking end signal is in Extension register R5Y[7].

12.119 R4Y: Horizontal Sync Start Shadow Registe r

I/O Port Address: 3?5

Index: This register is accessible only when Extension register CR2C[5:4] is 10.

Bit	Description	Reset Stat e
7	Horizontal Sync Start [7]	0
6	Horizontal Sync Start [6]	0
5	Horizontal Sync Start [5]	0
4	Horizontal Sync Start [4]	0
3	Horizontal Sync Start [3]	0
2	Horizontal Sync Start [2]	0
1	Horizontal Sync Start [1]	0
0	Horizontal Sync Start [0]	0

Bit	Descriptio n
7:0	**Horizontal Sync Start [7:0] :** When Sequencer register SR1[3] is 0 (the DCLK signal is the same signal as VCLK), this register performs the same function as CRT Controller register CR4[7:0].

12.120 R5Y: Horizontal Sync End Shadow Registe r

I/O Port Address: 3?5

Index: This register is accessible only when Extension register CR2C[5:4] is 10.

Bit	Description	Reset Stat e
7	Horizontal Blanking End [5]	0
6	Reserved	
5	Reserved	
4	Horizontal Sync End [4]	0
3	Horizontal Sync End [3]	0
2	Horizontal Sync End [2]	0
1	Horizontal Sync End [1]	0
0	Horizontal Sync End [0]	0

Bit	Descriptio n
7	**Horizontal Blanking End [5]:** • This bit is the most-significant bit for the 6-bit horizontal blanking end signal. • The least-significant 5 bits of the horizontal blanking end signal are in Extension register R3Y[4:0].
6:5	**Reserve d**
4:0	**Horizontal Sync End [4:0] :** When Sequencer register SR1[3] is 0 (the DCLK signal is the same signal as VCLK), this register performs the same function as CRT Controller register CR5[4:0].

12.121 R0Z: Horizontal Total Shadow Register

I/O Port Address: 3?5

Index: This register is accessible only when Extension register CR2C[5:4] is 11.

Bit	Description	Reset State
7	Horizontal Total [7]	0
6	Horizontal Total [6]	0
5	Horizontal Total [5]	0
4	Horizontal Total [4]	0
3	Horizontal Total [3]	0
2	Horizontal Total [2]	0
1	Horizontal Total [1]	0
0	Horizontal Total [0]	0

The RiZ (i = 0,2,3,4,5) Extension registers are horizontal timing shadow registers.

- These registers are used to automatically control the CRT controller on 640 × 480 and 800 × 600 LCDs, for both low-resolution and high-resolution applications.
- These registers control LCD timing independent of VGA modes.

Bit	Description
7:0	**Horizontal Total [7:0] :** When Sequencer register SR1[3] is 1 (VCLK is divided by 2), this register performs the same function as CRT Controller register CR0[7:0].

12.122 R2Z: Horizontal Blanking Start Shadow Registe r

I/O Port Address: 3?5

Index: This register is accessible only when Extension register CR2C[5:4] is 11.

Bit	Description	Reset Stat e
7	Horizontal Blanking Start [7]	0
6	Horizontal Blanking Start [6]	0
5	Horizontal Blanking Start [5]	0
4	Horizontal Blanking Start [4]	0
3	Horizontal Blanking Start [3]	0
2	Horizontal Blanking Start [2]	0
1	Horizontal Blanking Start [1]	0
0	Horizontal Blanking Start [0]	0

Bit	Descriptio n
7:0	**Horizontal Blanking Star t [7:0] :** When Sequencer register SR1[3] is 1 (VCLK is divided by 2), this register performs the same function as CRT Controller register CR2[7:0].

12.123 R3Z: Horizontal Blanking End Shadow Register

I/O Port Address: 3?5

Index: This register is accessible only when Extension register CR2C[5:4] is 11.

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Horizontal Blanking End [4]	0
3	Horizontal Blanking End [3]	0
2	Horizontal Blanking End [2]	0
1	Horizontal Blanking End [1]	0
0	Horizontal Blanking End [0]	0

Bit	Description
7:5	**Reserved**
4:0	**Horizontal Blanking End [4:0] :** When Sequencer register SR1[3] is 1 (VCLK is divided by 2), these bits perform the same function as CRT Controller register CR3[4:0]. • These bits are the least-significant 5 bits of a 6-bit word controlling the horizontal blanking end signal. • The most-significant sixth bit that controls the horizontal blanking end signal is in Extension register R5Z[7].

12.124 R4Z: Horizontal Sync Start Shadow Registe r

I/O Port Address: 3?5

Index: This register is accessible only when Extension register CR2C[5:4] is 11.

Bit	Description	Reset Stat e
7	Horizontal Sync Start [7]	0
6	Horizontal Sync Start [6]	0
5	Horizontal Sync Start [5]	0
4	Horizontal Sync Start [4]	0
3	Horizontal Sync Start [3]	0
2	Horizontal Sync Start [2]	0
1	Horizontal Sync Start [1]	0
0	Horizontal Sync Start [0]	0

Bit	Descriptio n
7:0	**Horizontal Sync Start [7:0] :** When Sequencer register SR1[3] is 1 (VCLK is divided by 2), this register performs the same function as CRT Controller register CR4[7:0].

12.125 R5Z: Horizontal Sync End Shadow Registe r

I/O Port Address: 3?5

Index: This register is accessible only when Extension register CR2C[5:4] is 11.

Bit	Description	Reset Stat e
7	Horizontal Blanking End [5]	0
6	Reserved	
5	Reserved	
4	Horizontal Sync End [4]	0
3	Horizontal Sync End [3]	0
2	Horizontal Sync End [2]	0
1	Horizontal Sync End [1]	0
0	Horizontal Sync End [0]	0

Bit	Descriptio n
7	**Horizontal Blanking End [5]:** • This bit is the most-significant bit of the 6-bit horizontal blanking end signal • The least-significant 5 bits of the horizontal blanking end signal are in Extension register R3Z[4:0].
6:5	**Reserve d**
4:0	**Horizontal Sync End [4:0] :** When Sequencer register SR1[3] is 1 (VCLK is divided by 2), this register performs the same function as CRT Controller register CR5[4:0].

13. ELECTRICAL SPECIFICATIONS

13.1 Absolute Maximum Ratings

Specification	Maximum Rating
Ambient temperature while operating (T_A)	0° to 70° C
Storage temperature	–65° to 150° C
Voltage on any pin	V_{SS} – 0.5 V to V_{DD} + 0.5 V
Operating power dissipation	1.5 Watts
Power supply voltage	7.0 Volts
Injection current (latch-up testing)	100 mA

NOTES:

1) System components must be operated within the limits of the absolute maximum ratings. If system components are run at ratings at or outside these limits, the system components may be permanently damaged .
2) Functional operation at or outside any of the conditions indicated in the absolute maximum ratings is not implied.
3) Exposure to absolute maximum rating conditions for extended periods may affect system reliability .

13.2 DC Specifications

13.2.1 DC Digital Specifications

In the table below, V_{DD} = 5.00 ± 0.25 V [or V_{DD} = 3.30 (+ 0.30 or – 0.15 V)] and T_A = 0° to 70° C, unless otherwise specified.

Symbol	Parameter	MIN	MAX	Conditions	Note
V_{DD} (5 V)	Power Supply Voltage (TTL)	4.75 Volts	5.25 Volts	Normal Operation	
V_{DD} (3.3 V)	Power Supply Voltage (CMOS)	3.15 Volts	3.45 Volts	Normal Operation	
V_{IL}	Input Low Voltage (TTL)	0 Volts	0.8 Volts	3.15 V < V_{DD} < 5.25 V	
V_{IH}	Input High Voltage (TTL)	2.0 Volts	V_{DD} + 5% V_{DD} (Volts)	3.15 V < V_{DD} < 5.25 V	
V_{IHC}	Input High Voltage (CMOS)	0.7V_{DD} (Volts)	V_{DD} + 5% V_{DD} (Volts)	3.15 V < V_{DD} < 5.25 V	
V_{ILC}	Input Low Voltage (CMOS)	–0.5 Volts	0.3V_{DD} (Volts)	3.15 V < V_{DD} < 5.25 V	
V_{OL}	Output Low Voltage (TTL)		0.4 Volts	I_{OL} = (Refer to Section 13.2.2.)	1
V_{OH}	Output High Voltage (TTL)	2.4 Volts		I_{OH} = (Refer to Section 13.2.2.)	2
V_{OHC}	Output High Voltage (CMOS)	0.9V_{DD} (Volts)		I_{OHC} = –200 µA	
V_{OLC}	Output Low Voltage (CMOS)		0.1V_{DD} (Volts)	I_{OLC} = 3.2 mA	
I_{CC1}	Power Supply Current		150 mA	CRT-only Operation	3
I_{CC2}	Power Supply Current		100 mA	LCD-only Operation	3
I_{CC3}	Power Supply Current		50 µA	Hardware-Controlled Suspend mode	3
I_{IL}	Input Low Current		–10 µA	V_{IN} = 0.0 V	
I_{IH}	Input High Current		10 µA	V_{IN} = V_{DD}	
I_{OZ}	Output Leakage Current	–10 µA	10 µA	0 < V_{OUT} < V_{DD}	4
C_{IN}	Input Capacitance		10 pF		5
C_{OUT}	Output Capacitance		10 pF		5

NOTES:

1) When V_{DD} = 5.0 V, data outputs D[31:0] rated at I_{OL} = 8 mA at V_{OL} = 0.5 V sink I_{OL} = 20 mA at V_{OL} = 0.6 V.
When V_{DD} = 3.3 V, data outputs D[31:0] rated at I_{OL} = 4 mA at V_{OL} = 0.3 V sink I_{OL} = 12 mA at V_{OL} = 0.6 V.

2) When V_{DD} = 5.0 V, data outputs D[31:0] rated at I_{OH} = –6.0 mA at V_{OH} = 4.5 V source I_{OH} = –15 mA at V_{OH} = 4.0 V.
When V_{DD} = 3.3 V, data outputs D[31:0] rated at I_{OH} = –3.0 mA at V_{OH} = 3.0 V source I_{OH} = –12 mA at V_{OH} = 2.0 V.

3) These current values occur when V_{DD} = 3.3 V, FPVDCLK = 28 MHz, and MCLK = 45 MHz .

4) This current is a measure of tristate output leakage current when in high-impedance (high-Z) mode .

5) This capacitance is periodically sampled and tested.

13.2.2 DC Specifications — Loading Value s

Pin Numbe r	Pin Nam e	I_{OH} (mA) When $V_{OH} = 0.9 V_{DD}$		I_{OL} (mA) When $V_{OL} = 0.1 V_{DD}$		Loa d (pF)
		V_{DD} = 3.30 V	V_{DD} = 5.00 V	V_{DD} = 3.30 V	V_{DD} = 5.00 V	
3	LDEV#	–6	–10	10.0	20.0	200
4	RDY#	–6	–10	10.0	20.0	200
5	INTR / INTR#	–4	–8	6	12	200
22	STOP#	–4	–8	10	16	200
23	PAR	–4	–8	10	16	200
43:46, 48:51, 53:61, 63:66, 68:72, 74:79, 136:135, 138:137,139:14 0	AD / D [31:0]	–3.0	–6	2	4	240
81	SLEEP#	–4	–8	6	12	50
91	VSYNC	–4	–8	6	12	50
93	HSYNC	–4	–8	6	12	50
94	NTSC / PAL	–4	–8	6	12	50
140:133, 131:125, 123:122, 120:11 4	FP[23:0]	–3	–6	6	12	50
95	CSYNC	–4	–8	6	12	50
144:141,134,133,125,12 3	FCP[7:0]	–3	–6	6	12	50
101	FCBLANK#	–3	–6	4	8	50
102	FPVEE	–3	–6	6	12	35
103	VCLK	–3	–6	6	12	35
106	FPVCC	–3	–6	6	12	35
108	FPDE	–3	–6	6	12	50
110	LFS[a]	–3	–6	6	12	50
112	LLCLK[a]	–4	–8	6	12	50
113	FPVDCLK	–4	–8	6	12	50
115	FP[1] / OVRW#	–3	–6	6	12	35
117	FP[3] / MO D	–3	–6	6	12	20
123	SBYST#	–4	–8	6	12	35
125	SUSPST#	–4	–8	6	12	35
146	TVON	–3	–6	6	12	50
148	PROG	–3	–6	6	12	35
151:161,163:167,186:191,193 , 196, 202:204, 206:208,1, 2	MD[31:0]	–3	–6	4	8	50
169, 170, 195, 19 4	CAS[3:0]#	–3	–6	4	8	50
169, 170, 195, 19 4	WE[3:0]#	–3	–6	4	8	50
171:180	MA[9:0]	–3	–6	4	8	50
181	CAS# / WE#	–3	–6	4	8	50
182	OE#	–3	–6	4	8	50
184:183	RAS[1:0]#	–3	–6	4	8	50

[a] The LLCLK and FPVDCLK values depend on the bit setting of Extension register SR2B[7].
When this bit = 0, the values for these pins are: I_{OH} = –8 mA, I_{OL} = 12 mA, and the load is 50 pF.
When this bit = 1, the values for these pins are: I_{OH} = –16mA, I_{OL} = 24 mA, and the load remains 50 pF .

13.2.3 DC Specifications — Palette DA C

In the table below, V_{DD} = 5.00 ± 0.25 V [or V_{DD} = 3.30(+ 0.30 or – 0.15 V)] and T_A = 0° to 70° C, unless otherwise specified.

Symbol	Parameter	MIN	MAX	Conditions
DACVDD (5.0 V)	DAC Supply Voltage	4.75 Volts	5.25 Volts	Normal Operation
DACVDD (3.3 V)	DAC Supply Voltage	3.15 Volts	3.45 Volts	Normal Operation
$AI_{DD2,3}$ (5.0 V)	Analog Supply Current		tbd[a]	$AV_{DD2,3}$ = 5.25 V
$AI_{DD2,3}$ (3.3 V)	Analog Supply Current		tbd	$AV_{DD2,3}$ = 3.45 V
I_{REF}[b]	DAC Reference Current (Nominal)	6.20 mA	7.14 mA	6.67 mA ± 7%

[a] 'tbd' = to be determined

[b] Refer to the detailed pin description in Chapter 2 for information regarding nominal I_{REF}.

13.2.4 DC Specifications — Frequency Synthesizer

In the table below, V_{DD} = 5.00 ± 0.25 V [or V_{DD} = 3.30 (+ 0.30 or – 0.15 V)] and T_A = 0° to 70° C, unless otherwise specified.

Symbol	Parameter	MIN	MAX	Conditions
MAV_{DD} VAV_{DD}	Synthesizer Supply Voltage	3.15 Volts	3.45 Volts	V_{DD} = 3.3 (+ 0.30 V or – 0.15 V)
MAV_{DD} VAV_{DD}	Synthesizer Supply Current	4.75 Volts	5.25 Volts	V_{DD} = 5.5 ± 0.25 V

13.3 DAC Characteristics

In the table below, V_{DD} = 5.00 ± 0.25 V [or V_{DD} = 3.30 (+ 0.30 or – 0.15 V)] and T_A = 0° to 70° C, unless otherwise specified.

Symbol	Parameter	MIN	MAX	Notes
Res.	Resolution		8 bits	
I_O	Output Current		30 mA	Note 1
t_D	Analog Output Delay		tbd[9]	Notes 2, 3, 4
t_r, t_f	Analog Output Rise/Fall Time		8 ns	Notes 3, 4, 5
t_s	Analog Output Settling Time		15 ns	Notes 3, 4, 6
t_{SK}	Analog Output Skew		tbd	Notes 3, 4, 7
FT	Clock and Data Feed-Through		tbd	Notes 3, 4, 7
DT	DAC-to-DAC Correlation		tbd	Notes 7, 8
GI	Glitch Impulse		tbd	Notes 3, 4, 7
CT	DAC-to-DAC Crosstalk		tbd	Notes 3, 4, 5

NOTES:

1) Output current measure occurs under the condition V_O < 1 volt.
2) t_D is measured from the 50% point of VCLK to 50% point of full-scale transition.
3) Load is 50 Ω and 30 pF per analog output.
4) I_{REF} = value to be determined from measures taken according to the application note "IREF Current Source" in the *CL-GD754X Application Book*.
5) t_r and t_f are measured from 10% to 90% full-scale.
6) t_S is measured from 50% of full-scale transition to output remaining within 2% of final value.
7) Outputs loaded identically.
8) About the mid-point of the distribution of the three DACs measured at full-scale output.
9) 'tbd' = to be determined.

13.4 AC Parameters — List of Timings

NOTES: In the following diagrams :

1) High-Z is high-impedance.
2) 'tbd' is to be determined.
3) 'MCLK' is the period for MCLK, a clock that is internal to the CL-GD7541/GD7543.

13.5 Bus Configuration — System Reset Timing

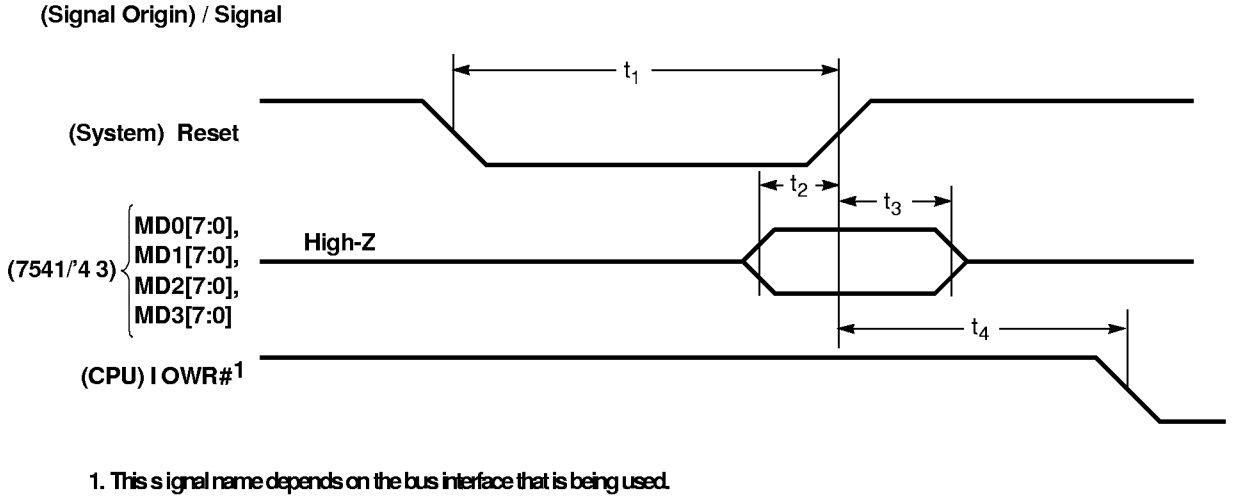
The timing diagram in this section is for the bus configuration, which takes place during system reset.

Table 13-1 and Figure 13-1 refer to information from the SW0, SW1, and SW2 pins, which are read by SR24[2:0] and used by the memory data lines to configure the CL-GD7541/GD7543.

Table 13-1. Bus Configuration — System Reset Timing

Symbol	Parameter	MIN	MAX
t_1[a]	System reset pulse width	12 MCLK	–
t_2	Memory data setup time to system reset rising edge	2 ns	–
t_3	Memory data hold time from system reset rising edge	5 ns	–
t_4	System reset high to first I/O Read/Write command	12 MCLK	–

[a] 'MCLK' is the period for MCLK, a clock that is internal to the CL-GD7541/GD7543.



1. This signal name depends on the bus interface that is being used.

Figure 13-1. Bus Configuration — System Reset Timing

13.6 Timing Diagrams — Local Bus

The timing diagrams in this section apply to the '486 local bus and VESA VL-Bus interfaces to the CL-GD7541/GD7543.

Table 13-2. Local Bus — LCLK Timing

Symbol	Parameter	CLK1X	
		MIN	MAX
t_1	Rise time	0.5 ns	4.0 ns
t_2	Fall time	0.5 ns	4.0 ns
t_3	Positive high pulse width	40% t_5	60% t_5
t_4	Negative low pulse width	40% t_5	60% t_5
t_5	Period	30 ns	tbd[a]

[a] 'tbd' = to be determined

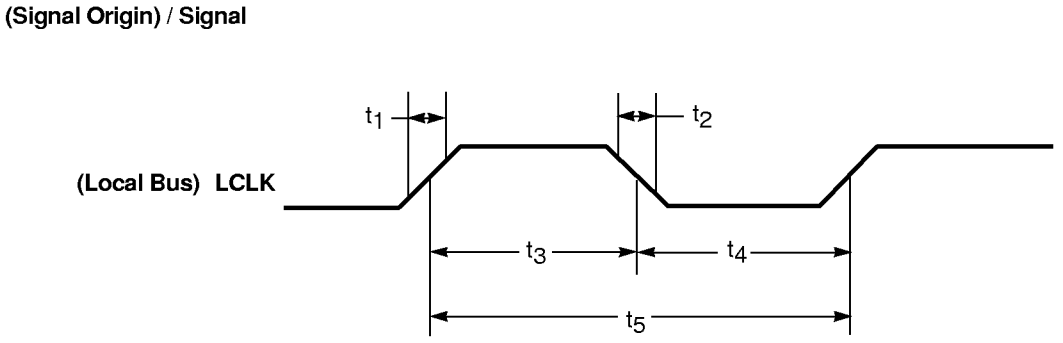


Figure 13-2. Local Bus — LCLK Timing

Table 1 3-3. Local Bus — ADS# and LDEV# Timin g

Symbol	Parameter	MIN	MAX
t_1	Address, Status, ADS# setup to LCLK	5 ns	–
t_2	LDEV# low delay from Address, Status (20-pF loading)	–	15 ns
t_3	LDEV# high delay from Address, Statu s	–	18 ns

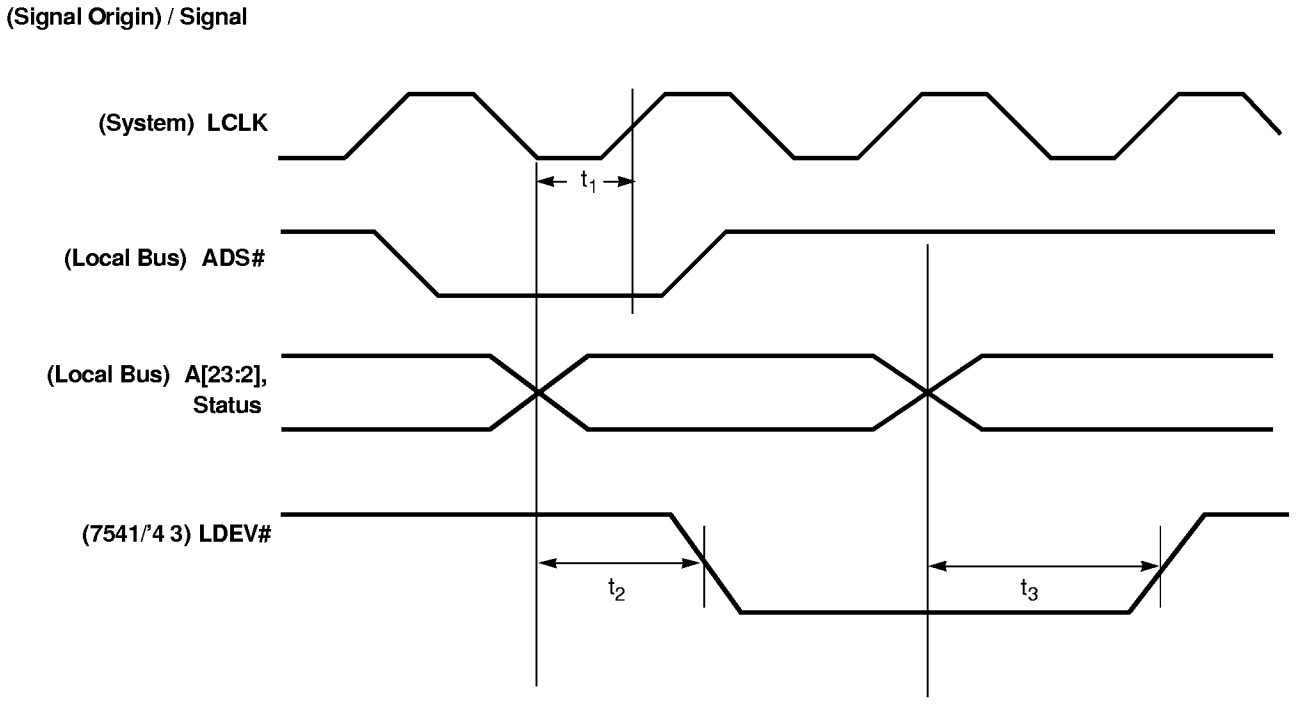


Figure 1 3-3. Local Bus — ADS# and LDEV# Timin g

Table 13-4. Local Bus — RDY# and Read-Data Timing

Symbol	Parameter	MIN	MAX
t_1	RDY# low delay from LCLK	0	12 ns
t_2	RDY# high delay from LCLK	0	12 ns
t_3	RDY# high pulse width before high-Z	1/2 LCLK	–
t_4	Read data setup to RDY# low	0 ns	–
t_5	Read data hold from RDYRTN# high	12 ns	tbd[a]

[a] 'tbd' = to be determined

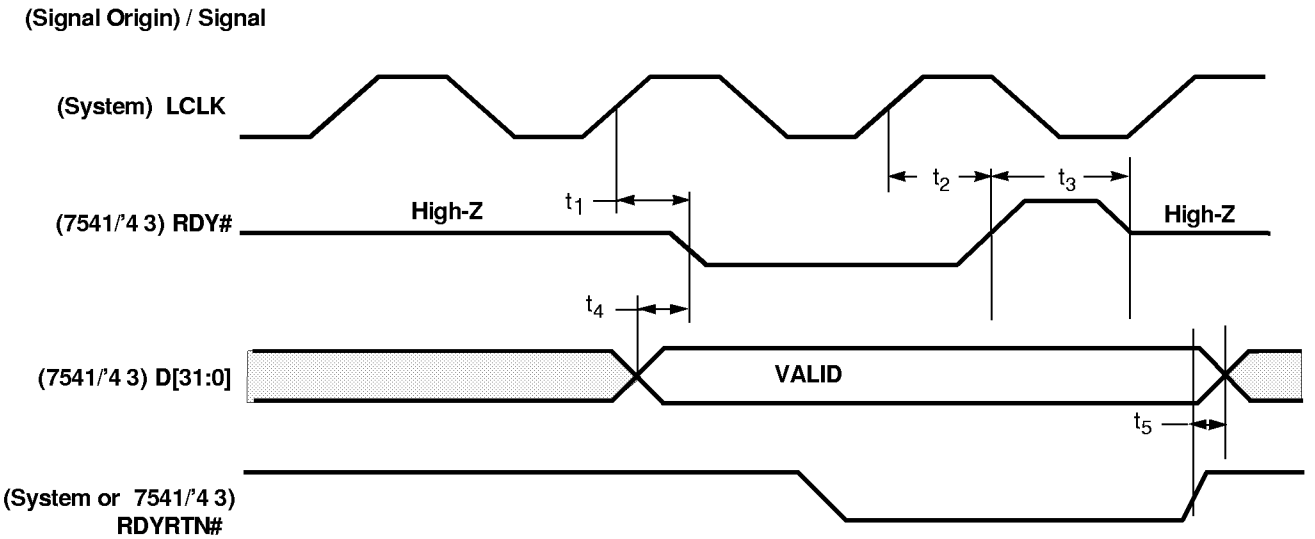


Figure 13-4. Local Bus — RDY# and Read-Data Timing

Table 1 3-5. Local Bus — RDYRTN# Timin g

Symbol	Parameter	MIN	MAX
t_1	RDYRTN# setup time to LCL K	5 ns	–
t_2	RDYRTN# hold time from LCL K	2 ns	–

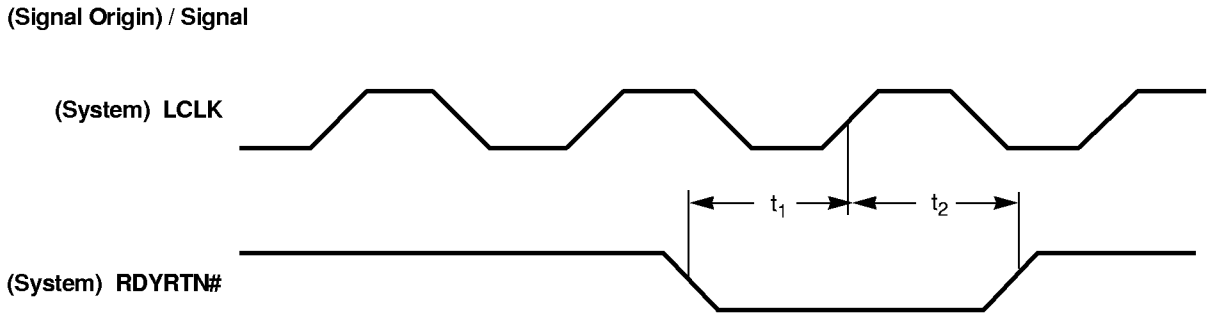


Figure 1 3-5. Local Bus: RDYRTN# Timin g

Table 1 3-6. Local Bus — Write Data Timin g

Symbol	Parameter	MIN	MAX
t_1	Data setup time to LCL K	7 ns	–
t_2	Data hold time from LCL K	2 ns	–

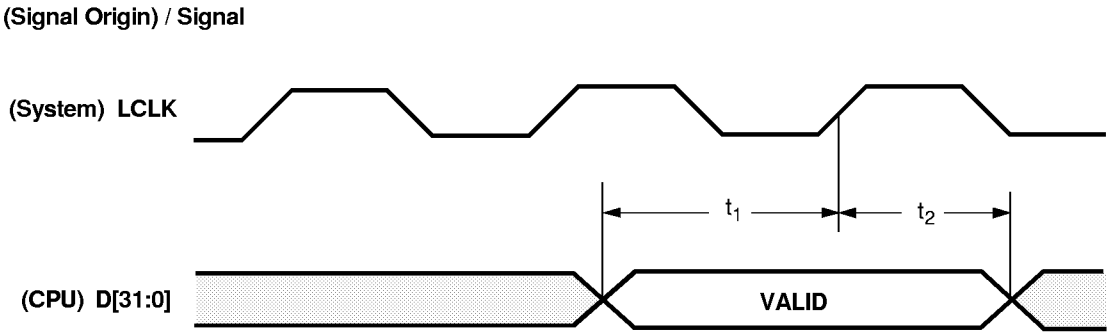


Figure 1 3-6. Local Bus — Write Data Timin g

13.7 Timing Diagrams — PCI Bus

The timing diagrams in this section apply to a PCI bus interface to the CL-GD7541/GD7543.

Table 13-7. PCI Bus — FRAME#, DEVSEL#, AD[31:0], and C/BE[3:0]# Timing (Write)

Symbol	Parameter	MIN	MAX
t_1	FRAME# setup to CLK	7 ns	–
t_2	AD[31:0] (Address) setup to CLK	7 ns	–
t_3	AD[31:0] (Address) hold from CLK	0 ns	–
t_4	AD[31:0] (Data) setup to CLK (write)	7 ns	–
t_5	AD[31:0] (Data) hold from CLK (write)	0 ns	–
t_6	C/BE[3:0]# (Bus CMD) setup to CLK	7 ns	–
t_7	C/BE[3:0]# (Bus CMD) hold from CLK	0 ns	–
t_8	C/BE[3:0]# (Byte Enable) setup to CLK	7 ns	–
t_9	DEVSEL# delay from CLK	0 ns	11
t_{10}	DEVSEL# high before high-Z	1 CLK	–

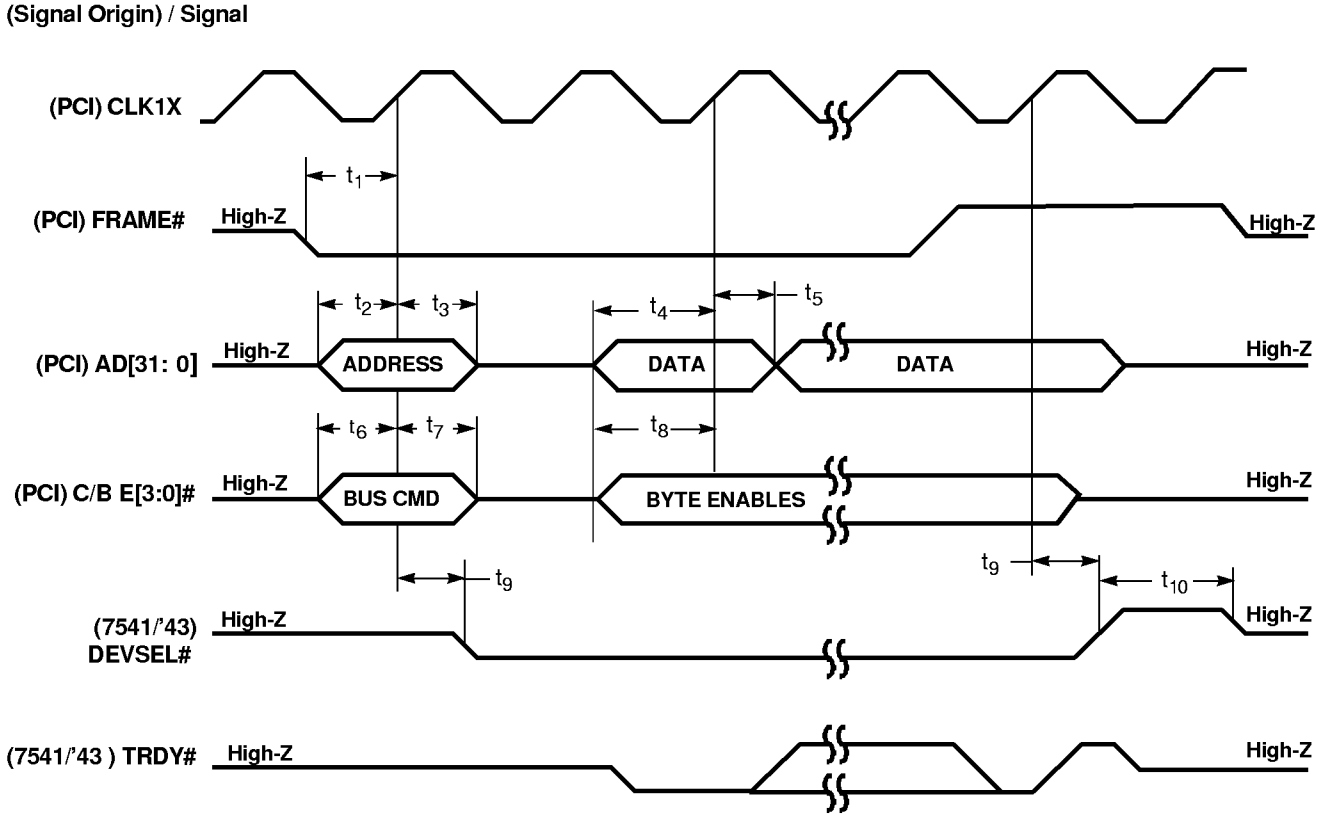


Figure 13-7. PCI Bus — FRAME#, DEVSEL#, AD[31:0], and C/BE[3:0]# Timing (Write)

Table 1 3-8. PCI Bus — FRAME#, DEVSEL#, AD[31:0], and C/BE[3:0]# Timing (Read)

Symbo l	Paramete r	MIN	MAX
t_1	FRAME# setup to CL K	7 ns	–
t_2	AD[31:0] (Address) setup to CL K	7 ns	–
t_3	AD[31:0] (Address) hold from CL K	0 ns	–
t_4	AD[31:0], C/BE[3:0]# high-Z from CLK (read)	0 ns	28 ns
t_5	C/BE[3:0]# (Bus CMD) setup to CL K	7 ns	–
t_6	C/BE[3:0]# (Bus CMD) hold from CL K	0 ns	–
t_7	C/BE[3:0]# (Byte Enable) setup to CL K	7 ns	–
t_8	DEVSEL# delay from CL K	0 ns	11
t_9	DEVSEL# high before high- Z	1 CLK	–
t_{10}	Data delay from CLK (read)	2 ns	11 ns
t_{11}	Data hold from CLK (read)	0 ns	tbd

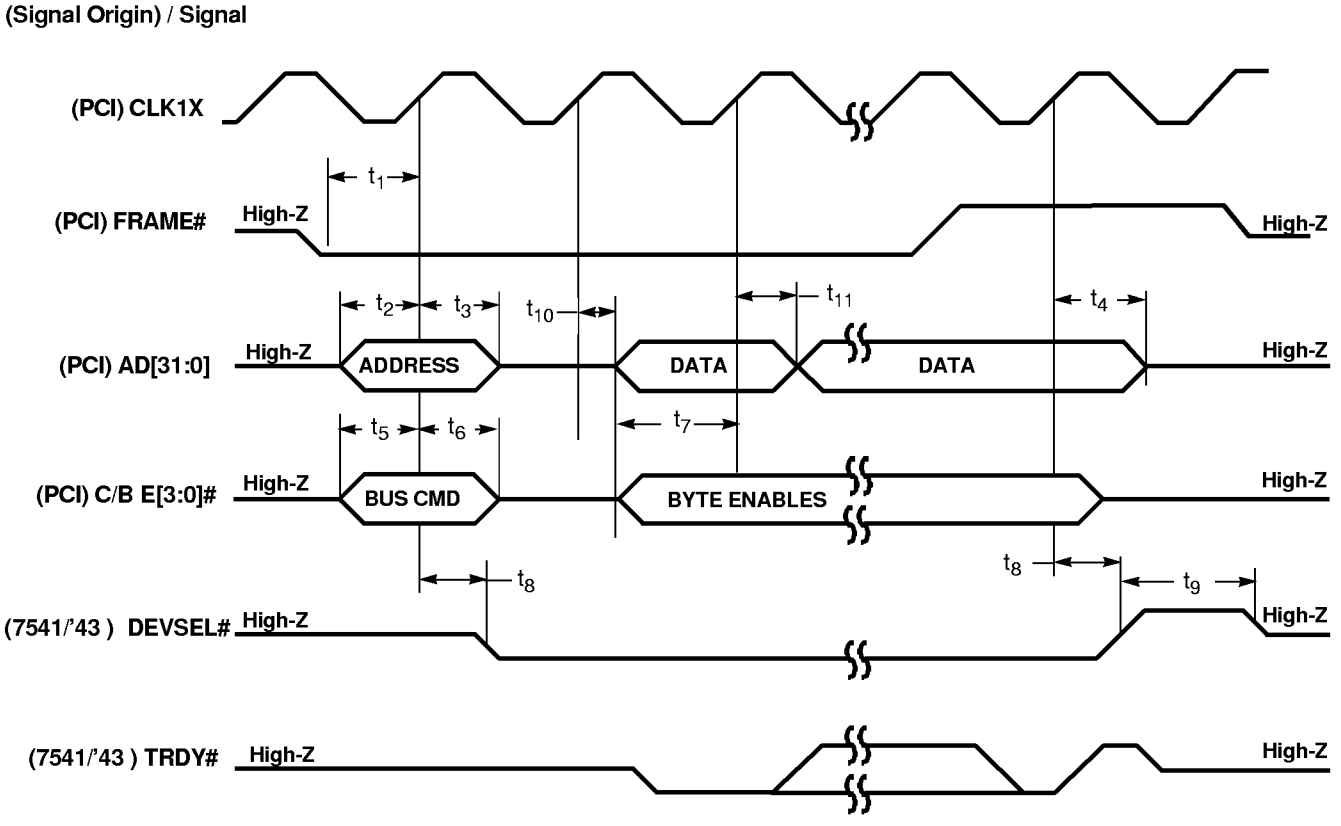


Figure 1 3-8. PCI Bus — FRAME#, DEVSEL#, AD[31:0], and C/BE[3:0]# Timing (Read)

Table 13-9. PCI Bus — TRDY# Delay Timing

Symbol	Parameter	MIN	MAX
t_1	TRDY# low delay from CLK	0 ns	15 ns
t_2	TRDY# high delay from CLK	0 ns	15 ns
t_3	TRDY# high pulse before high-Z	1 CLK	–

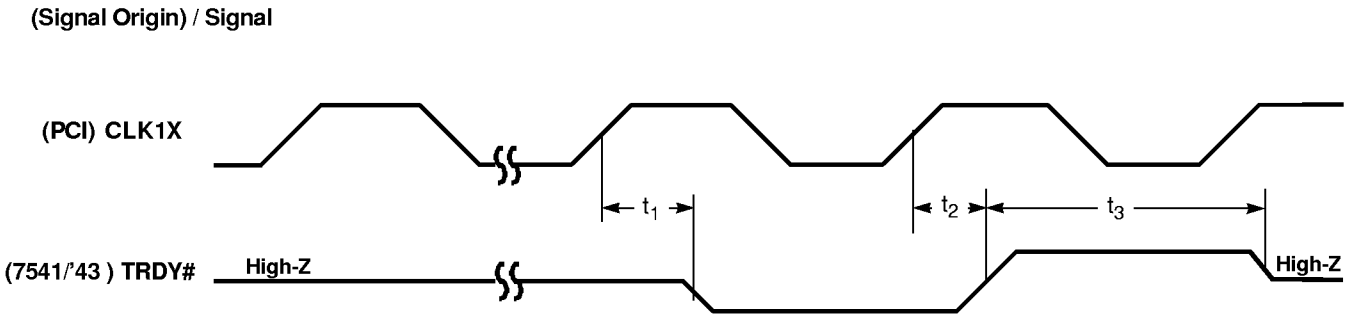


Figure 13-9. PCI Bus — TRDY# Delay Timing

Table 13-10. PCI Bus — Read Data / IRDY# Timing

Symbol	Parameter	MIN	MAX
t_1	IRDY# setup to CLK	7 ns	–
t_2	IRDY# hold from CLK	0 ns	–

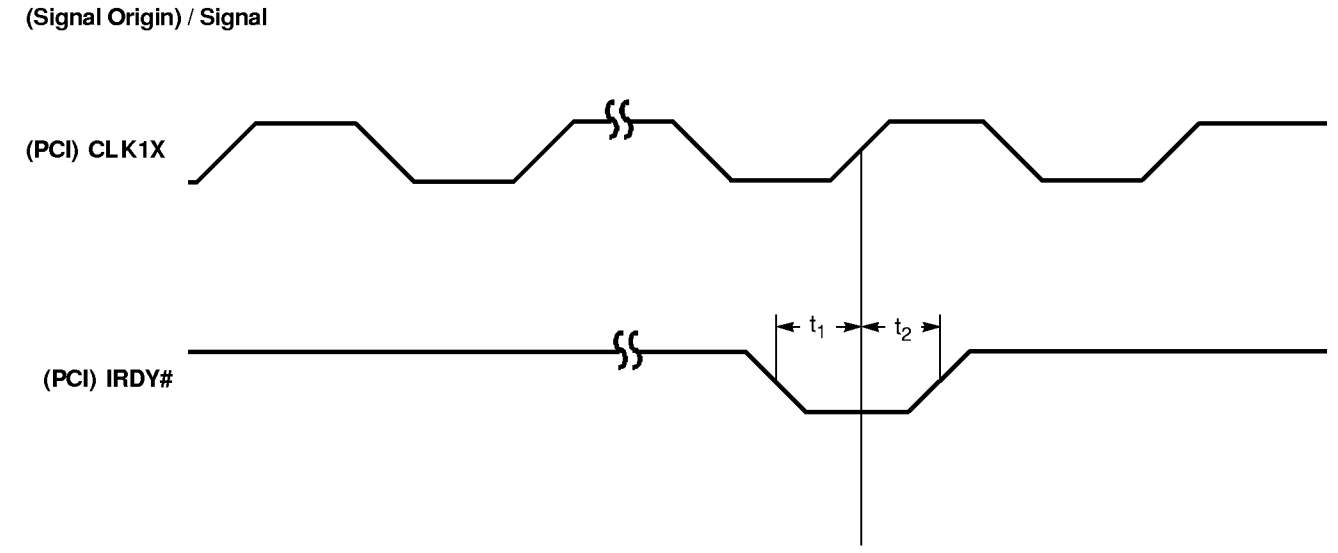


Figure 13-10. PCI Bus — Read Data / IRDY# Timing

Table 1 3-11. PCI Bus — STOP# Delay Timin g

Symbol	Parameter	MIN	MAX
t_1	STOP# low delay from CL K	2 ns	11 ns
t_2	STOP# high delay from CL K	2 ns	11 ns
t_3	STOP# high pulse before high- Z	1 CLK	–

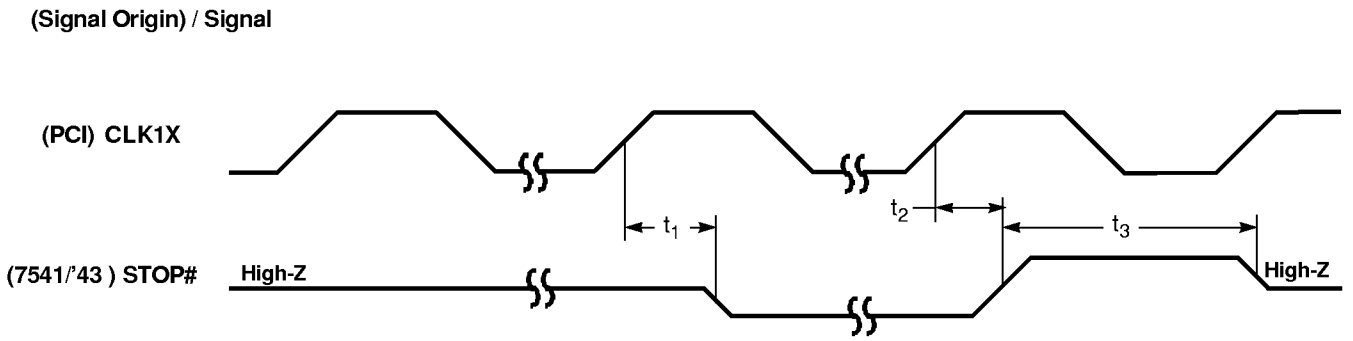


Figure 1 3-11. PCI Bus — STOP# Delay Timin g

Table 13-12. PCI Bus — IDSEL Timing

Symbol	Parameter	MIN	MAX
t_1	IDSEL setup to CLK	7 ns	–
t_2	IDSEL hold	0 ns	–

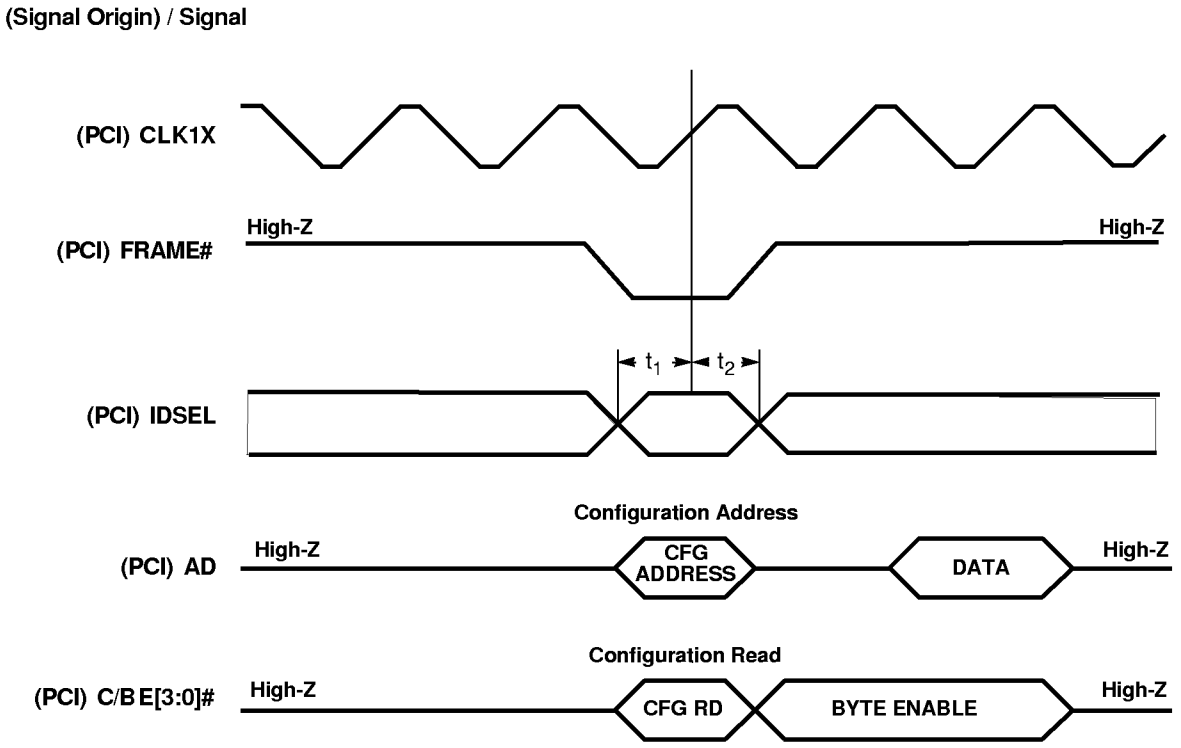


Figure 13-12. PCI Bus — IDSEL Timing

Table 1 3-13. PCI Bus — PAR Timing (Write)

Symbol	Parameter	MIN	MAX
t_1	Address PAR setup from CLK (input to CL-GD7541/GD7543)	7 ns	–
t_2	Address PAR hold from CLK (input to CL-GD7541/GD7543)	0 ns	–
t_3	Data PAR setup from CLK (input to CL-GD7541/GD7543)	7 ns	–
t_4	Data PAR hold from CLK (input to CL-GD7541/GD7543)	0 ns	–

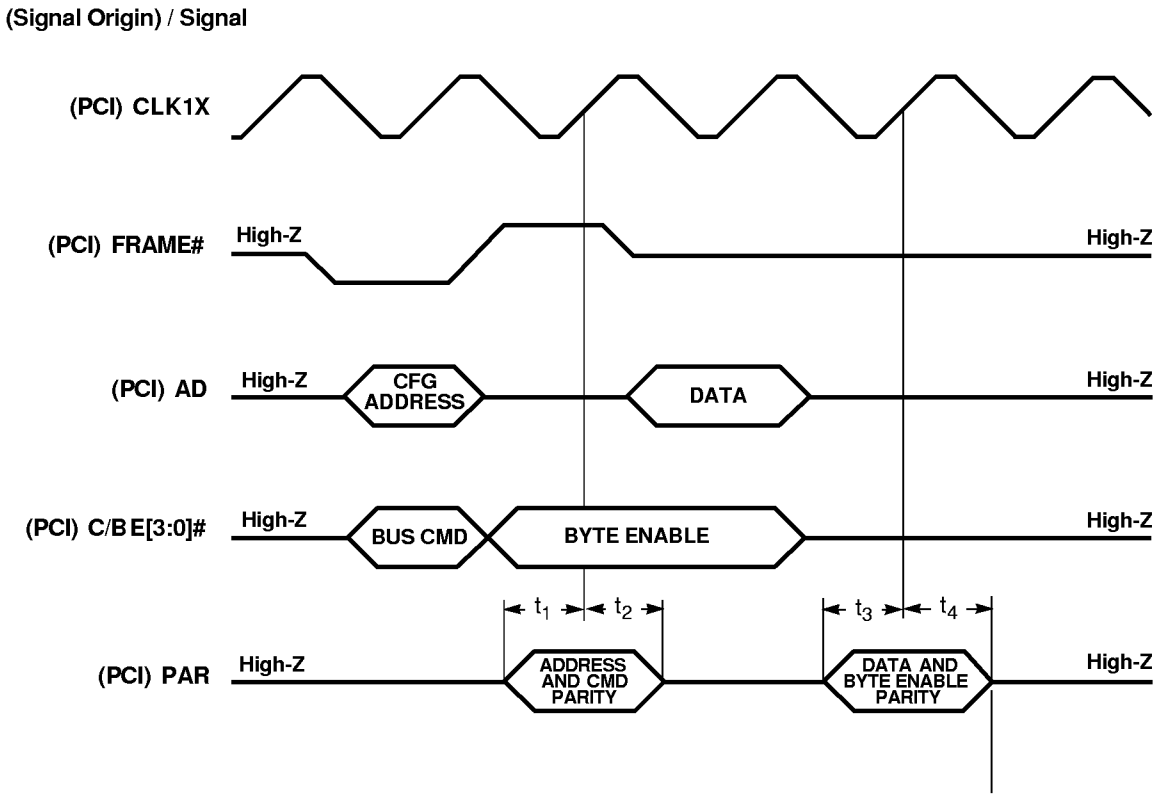


Figure 1 3-13. PCI Bus — PAR Timing (Write)

Table 13-14. PCI Bus — PAR Timing (Read)

Symbol	Parameter	MIN	MAX
t_1	PAR setup from CLK (input to CL-GD7541/GD7543)	7 ns	–
t_2	PAR hold from CLK (input to CL-GD7541/GD7543)	0 ns	–
t_3	PAR delay from CLK (output to CL-GD7541/GD7543)	2 ns	11 ns
t_4	PAR off delay from CLK (output to CL-GD7541/GD7543)	–	28 ns

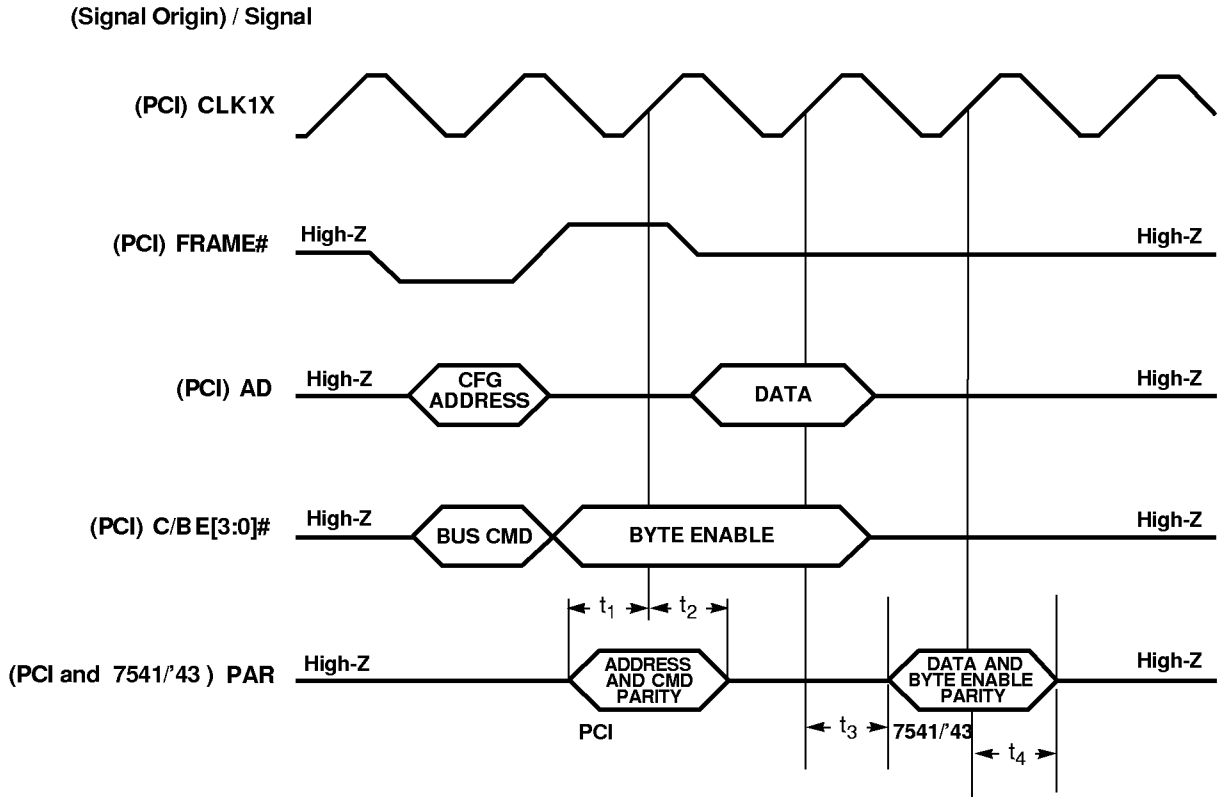


Figure 13-14. PCI Bus — PAR Timing (Read)

13.8 Timing Diagrams — Display Memory Buses

The timing diagrams in this section apply to the CL-GD7541/GD7543 bus interface to the display memory.

Table 13-15. Display Memory Bus — Read Timing

Symbol	Parameter	MIN	MAX
t_1	Address setup to RAS# low	1.5 MCLK[a] – 2 ns	–
t_2	Address setup to CAS# low	1.0 MCLK – 1 ns	–
t_3	RAS# low to CAS# low delay (standard RAS#)	2.5 MCLK – 2 ns	
	RAS# low to CAS# low delay (extended RAS#)	3.0 MCLK – 2 ns	
t_4	Row Address hold from RAS# low	1.5 MCLK	–
t_5	Column Address hold from CAS# low	1.0 MCLK	–
t_6	RAS# precharge (RAS# pulse width high) (standard RAS#)	2.5 MCLK – 2 ns	–
	RAS# precharge (RAS# pulse width high) (extended RAS#)	3.0 MCLK	–
t_7	Read cycle time (standard RAS#)	6.0 MCLK	–
	Read cycle time (extended RAS#)	7.0 MCLK	–
t_8	Read Command hold from CAS# high	0.5 MCLK – 7.5 ns	0.5 MCLK – 5 ns
t_9	CAS# precharge (CAS# pulse width high)	1.0 MCLK – 6 ns	1.0 MCLK – 3 ns
t_{10}	RAS# pulse width low (standard RAS#)	3.5 MCLK	–
t_{11}	CAS# pulse width low	1.0 MCLK + 3 ns	1 MCLK + 6 ns
t_{12}	Read Data hold from CAS# high	10 ns	–
t_{13}	CAS# cycle time	2.0 MCLK	–
t_{14}	Read Data hold from OE# high	10 ns	–

[a] 'MCLK' is the period for MCLK, a clock that is internal to the CL-GD7541/GD7543.

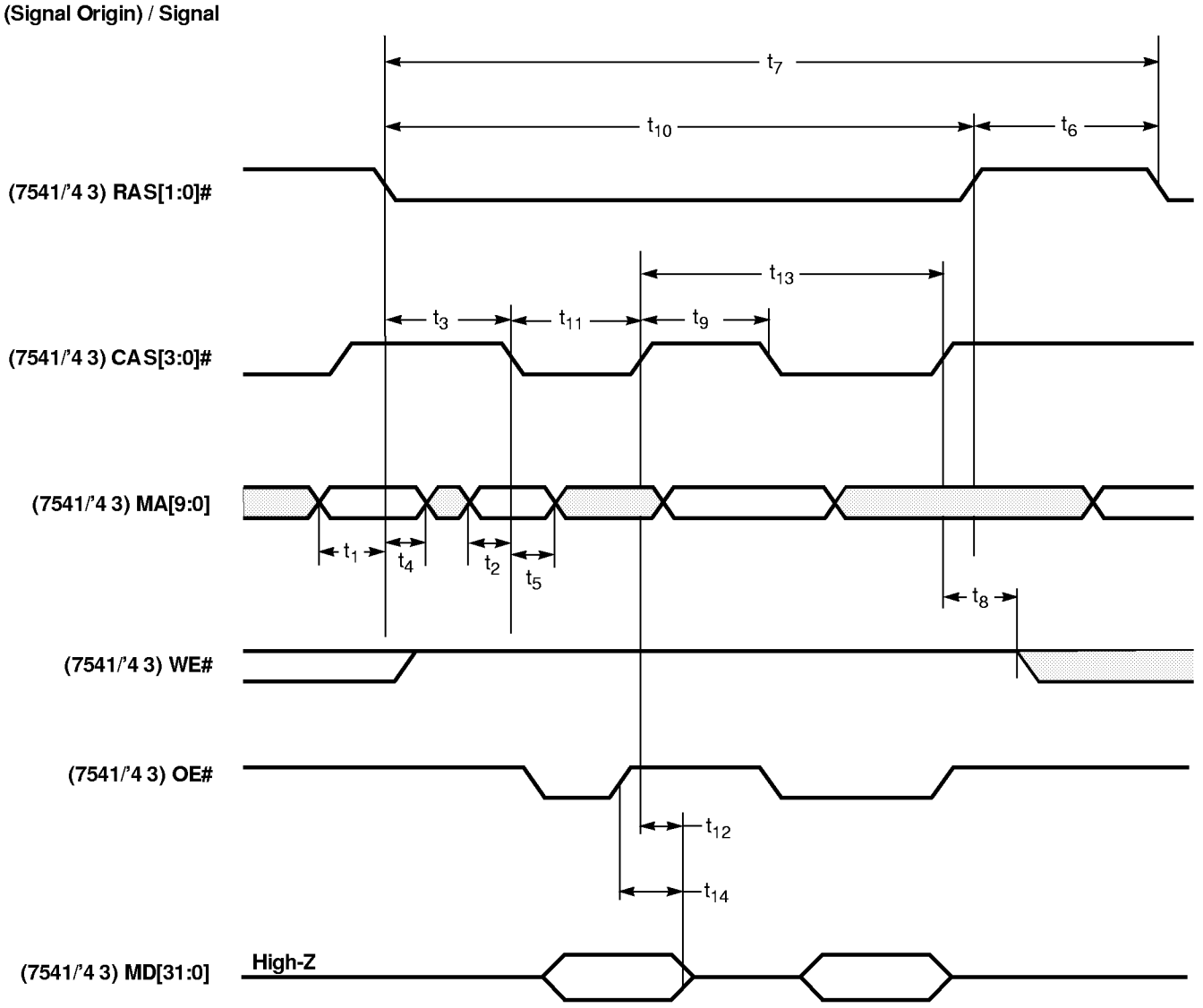


Figure 1 3-15. Display Memory Bus — Read Timin g

In Table 13-16, the memory interface specifications are valid at operating voltages of V_{DD} = 5.00 ± 0.25 V [or V_{DD} = 3.30 (+ 0.30 or – 0.15 V)] and T_A = 0° to 70° C, unless otherwise specified.

Table 1 3-16. Display Memory Bus — Write Ti ming

Symbol	Parameter	MIN	MAX
t_1	Address setup to RAS# lo w	1.5 MCLK[a] – 2 ns	–
t_2	Address setup to CAS# lo w	1.5 MCLK – 1 ns	–
t_3	RAS# low to CAS# low delay (standard RAS#)	2.5 MCLK – 2 ns	–
	RAS# low to CAS# low delay (extended RAS#)	3.0 MCLK – 2 ns	–
t_4	Row Address hold from RAS# lo w	1.5 MCLK	–
t_5	Column Address hold from CAS# lo w	1 MCLK	–
t_6	RAS# precharge (RAS# pulse width high) (standard RAS#)	2.5 MCLK – 2 ns	–
	RAS# precharge (RAS# pulse width high) (extended RAS#)	3.0 MCLK	–
t_7	Write cycle time (standard RAS#)	6.0 MCLK	–
	Write cycle time (extended RAS#)	7.0 MCLK	–
t_8	CAS# precharge (CAS# pulse width high)	1.0 MCLK – 6 ns	1 MCLK – 3 ns
t_9	CAS# cycle tim e	2.0 MCLK	–
t_{10}	CAS# pulse width lo w	1.0 MCLK + 3 ns	1 MCLK + 6 ns
t_{11}	RAS# pulse width low (standard RAS#)	3.5 MCLK	
t_{12}	WE# low setup to CAS# lo w	1.0 MCLK + 2 ns	–
t_{13}	WE# low hold to CAS# lo w	1.5 MCLK	–
t_{14}	Write Data setup to CAS# lo w	1.0 MCLK – 2 ns	1 MCLK + 2 ns
t_{15}	Write Data hold from CAS# low	1.0 MCLK + 1 ns	–
t_{16}	RAS# low to first CAS# high (standard RAS#)		4 MCLK – 1 ns

[a] 'MCLK' is the period for MCLK, a clock that is internal to the CL-GD7541/GD7543.

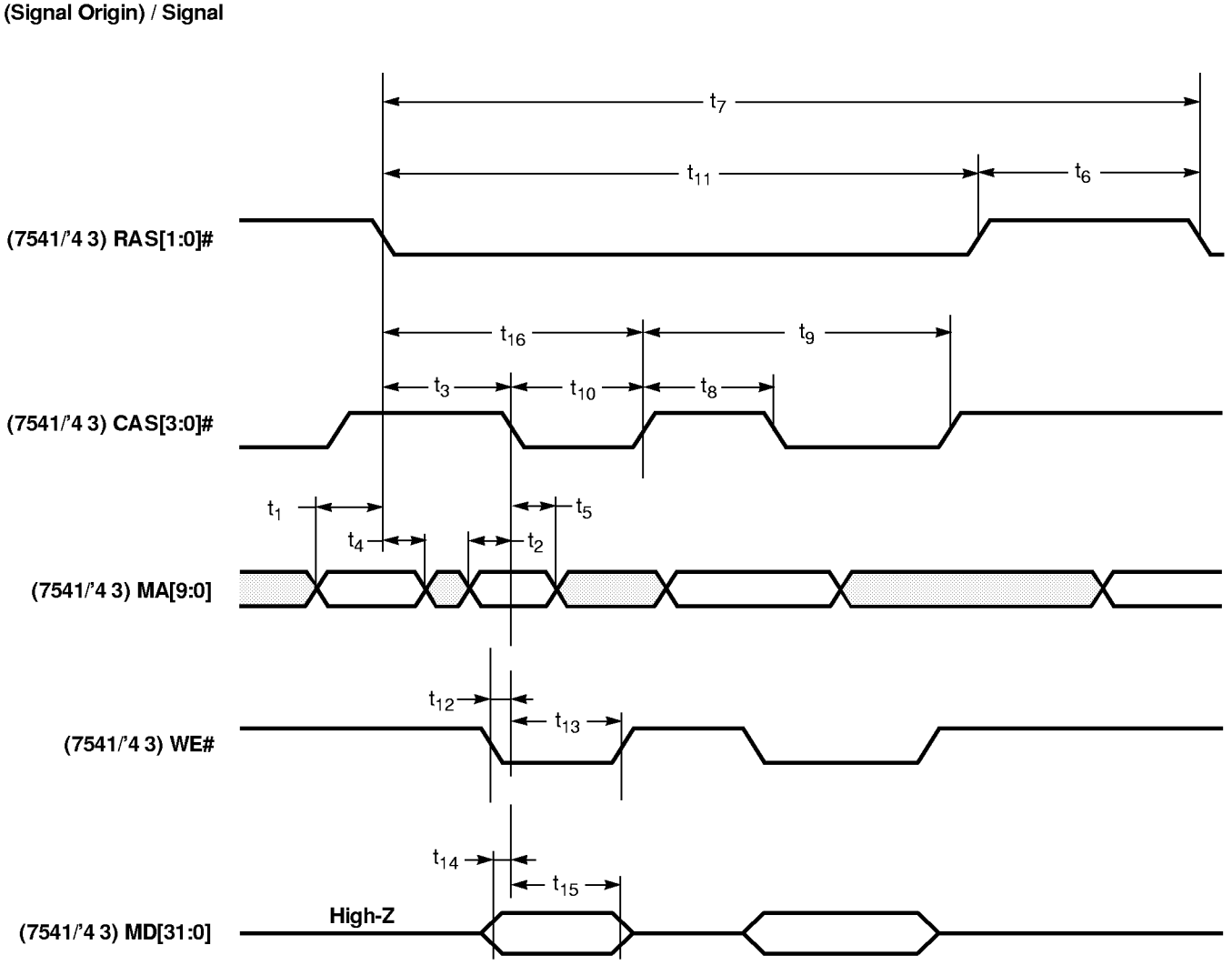


Figure 1 3-16. Display Memory Bus — Write Timin g

Table 13-17. Display Memory Bus — CAS#-before-RAS# Refresh Timing

Symbol	Parameter	MIN	MAX
t_1	CAS# low setup time to RAS# Active[a]	1 MCLK[b]	–
t_2	RAS# low pulse width	4 MCLK	–
t_3	RAS# high pulse width	3 MCLK	–
t_4	CAS# hold time for refresh	1.5 MCLK	–
t_5	Refresh cycle period	7 MCLK	–
t_6	CAS# pulse width high (precharge time)	2 MCLK	–
t_7	RAS# high to CAS# low (precharge time)	1 MCLK	–

[a] There are either three or five RAS# pulses while CAS# remains low.

[b] 'MCLK' is the period for MCLK, a clock that is internal to the CL-GD7541/GD7543.

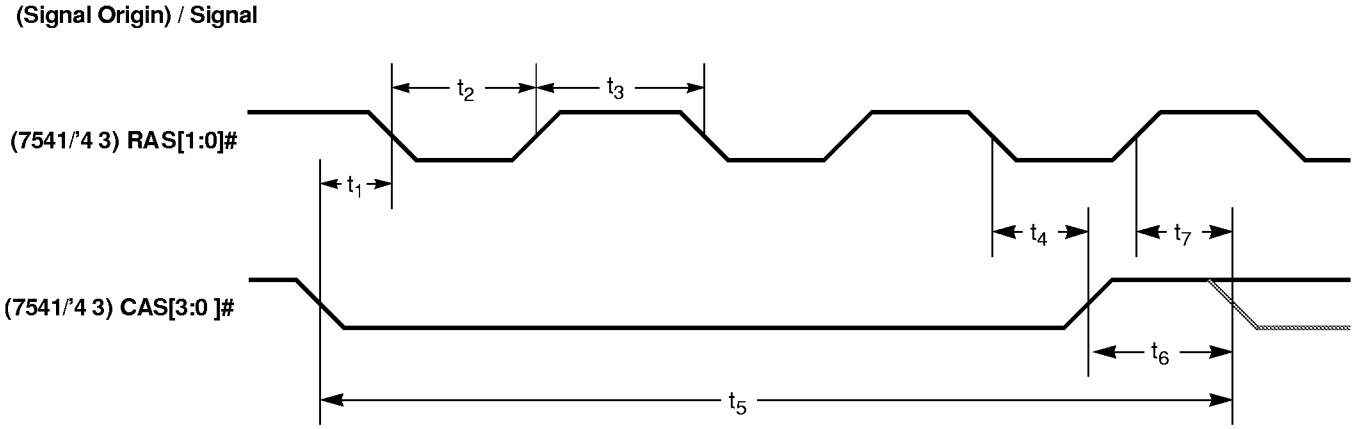


Figure 13-17. Display Memory Bus — CAS#-before-RAS# Refresh Timing

13.9 Timing Diagrams — Feature Connecto r

The timing diagrams in this section apply to the CL-GD7541/GD7543 interface to the Feature Connector (FC). For more information, refer to application note “8-Bit Dynamic Video Overlay” in the *CL-GD754X Application Boo k*.

Table 1 3-18. Feature Connector — Timing with Clock and Data Driven Externall y

Symbol	Parameter	MIN	MAX
t_1	FCP[7:0] setup to FCVCL K	6 ns	–
t_2	FCP[7:0] hold from FCVCL K	6 ns	–

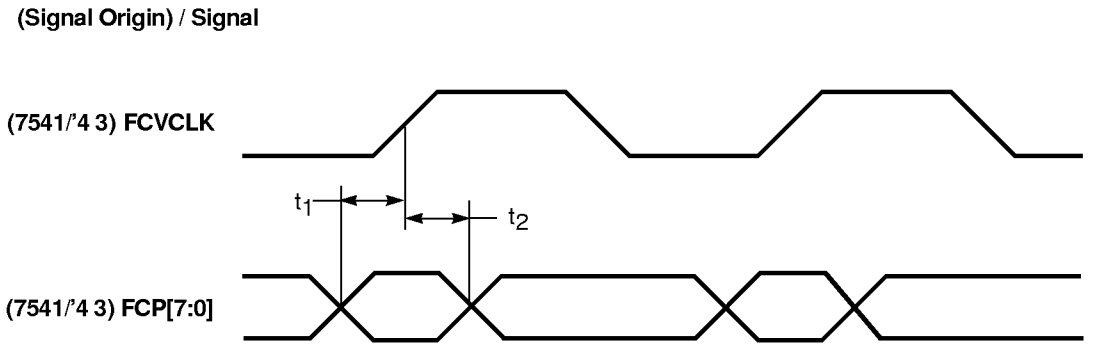


Figure 1 3-18. Feature Connector — Timing with Clock and Data Driven Externall y

Table 1 3-19. Feature Connector — FCVCLK Input Timing Requirement s

Symbol	Parameter	MIN	MAX
t_1	Rise time (FCVCLK)	–	3 ns
t_2	Fall time (FCVCLK)	–	3 ns
t_3	High period (FCVCLK)	40% of t_5	60% of t_5
t_4	Low period (FCVCLK)	40% of t_5	60% of t_5
t_5	Period (FCVCLK)	20 ns	–

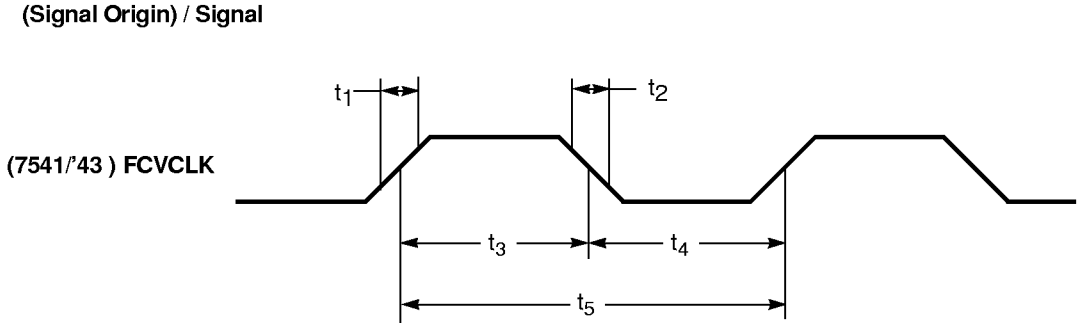


Figure 1 3-19. Feature Connector — FCVCLK Input Timing Requirement s

13.10 Timing Diagrams — LCD Interfac e

The timing diagrams in this section apply to the CL-GD7541/GD7543 interface to LCD flat panels.

NOTES:

M2DD-8 is:	monochrome	2-color	dual-scan	8-bit data interface
M2SS-8 is:	monochrome	2-color	single-scan	8-bit data interface
C8DD-16 is:	color	8-color	dual-scan	16-bit data interface
C8DD-8 is:	color	8-color	dual-scan	8-bit data interface
C8SS-16 is:	color	8-color	single-scan	16-bit data interface
M2DD-16 is:	monochrome	2-color	dual-scan	16-bit data interface
C8SS-id-8 is:	color	8-color	single-scan	8-bit interleaved data interfac e
C512SS is:	color	512 colors	single-scan	
C4KSS is:	color	4K colors	single-scan	
C256KSS is:	color	256K colors	single-scan	
C16MSS is:	color	16M colors	single-scan	
C4SSI is:	color	4 colors	single-scan	

Table 1 3-20. LCD Interface: Timing for STN Monochrome and Color-Passive LC D[a]

Symbol	Parameter	M2DD-8	M2SS-8	C8DD-16	C8DD-8	C8SS-16	M2DD-16	C8SS-id-8
		Mono.	Mono.	Color	Color	Color	Mono. Hi-Res.	Color
t_1	FPVDCLK period	$4t_1$[b]	$8t_1$	$2.5t_1$	t_1	$5t_1$	$8t_1$	$5t_1$
t_2	FPVDCLK high time	$2t_1$ – 6 ns	$4t_1$ – 6 ns	t_1 – 6 ns	$0.5t_1$ – 6 ns	$2t_1$ – 6 ns	$4t_1$ – 6 ns	t_1 – 6 ns
t_3	FPVDCLK low time	$2t_1$ – 6 ns	$4t_1$ – 6 ns	t_1 – 6 ns	$0.5t_1$ – 6 ns	$2t_1$ – 6 ns	$4t_1$ – 6 ns	$4t_1$ – 6 ns
t_4	FPVDCLK rise and fall time (maximum)	6 ns	6 ns	6 ns	6 ns	6 ns	6 ns	6 ns
t_5	Data setup time	$2t_1$ – 10 ns	$4t_1$ – 10 ns	t_1 – 6 ns	$0.5t_1$ – 6 ns	$2t_1$ – 10 ns	$4t_1$ – 10 ns	t_1 – 10 ns
t_6	Data hold time	$2t_1$ – 10 ns	$4t_1$ – 10 ns	t_1 – 6 ns	$0.5t_1$ – 6 ns	$2t_1$ – 10 ns	$4t_1$ – 10 ns	t_1 – 10 ns
t_7	FPVDCLK low to LLCLK low	$4t_1$ – 10 ns	$8t_1$ – 10 ns	t_1 – 6 ns	$2t_1$ – 10 ns	$4t_1$ – 10 ns	$8t_1$ –10 ns	$2t_1$ – 10 ns
t_8	FPVDCLK low from LLCLK low	$4t_1$ – 10 ns	$8t_1$ – 10 ns	t_1 – 6 ns	$2t_1$ – 10 ns	$4t_1$ – 10 ns	$8t_1$ – 10 ns	$2t_1$ – 10 ns
t_9	LLCLK high time	$4t_1$ – 6 ns	$4t_1$ – 6 ns	$4t_1$ – 6 ns	$4t_1$ – 6 ns	$4t_1$ – 6 ns	$4t_1$ – 6 ns	$4t_1$ – 6 ns
t_{10}	LFS high setup to LLCLK low (typical)	$2t_1$	t_1	$2t_1$	$2t_1$	$2t_1$	t_1	$2t_1$
t_{11}	LFS high hold time from LLCLK low (typical)	$2t_1$	$2t_1$	$2t_1$	$2t_1$	$2t_1$	$2t_1$	$2t_1$
t_{12}	MOD delay from FPVDCLK high (maximum)	300 ns	300 ns	300 ns	300 ns	300 ns	300 ns	300 ns

[a] Values are *minimum* unless otherwise specified.
[b] 't_1' is the period for the FPVDCLK.

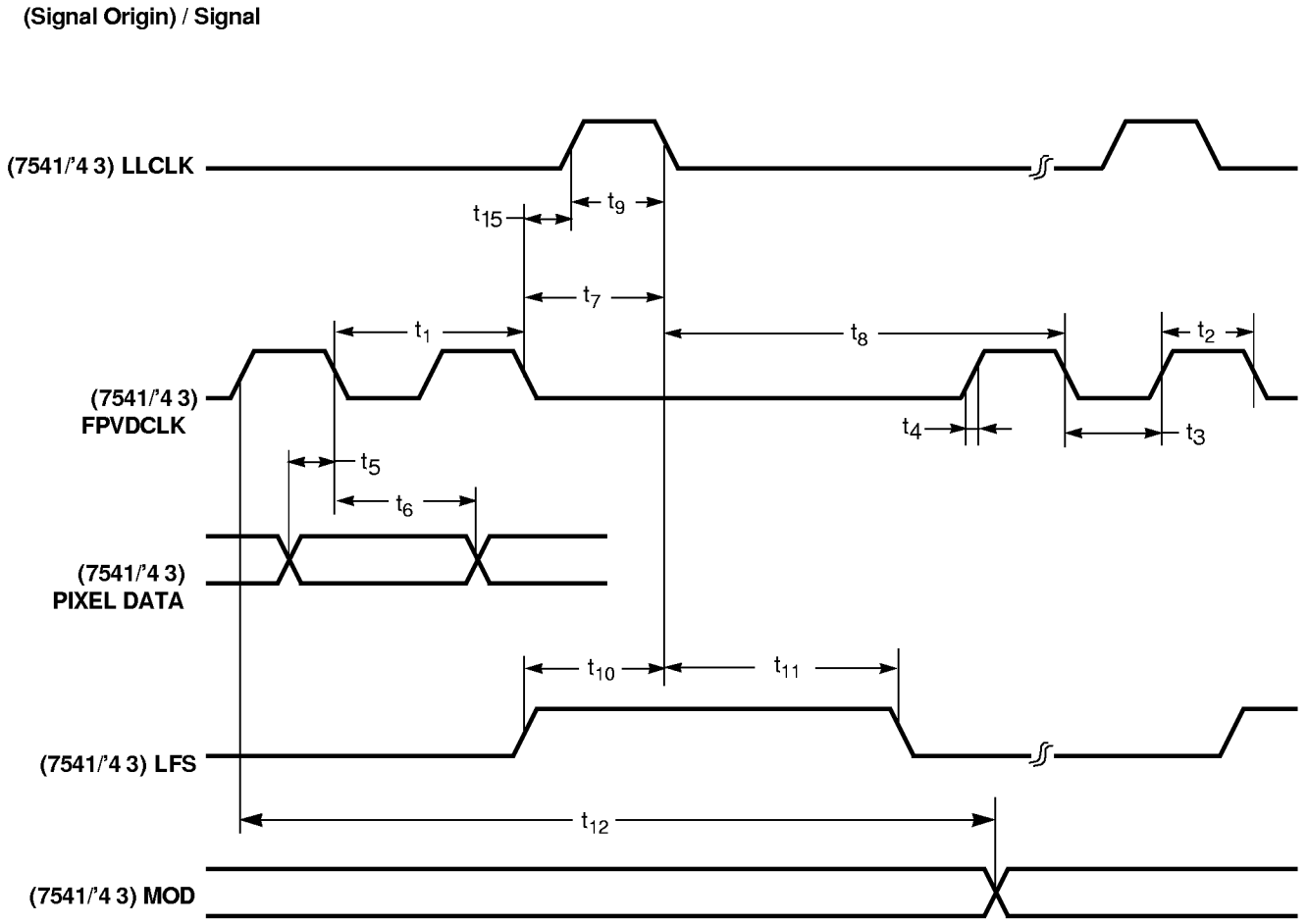
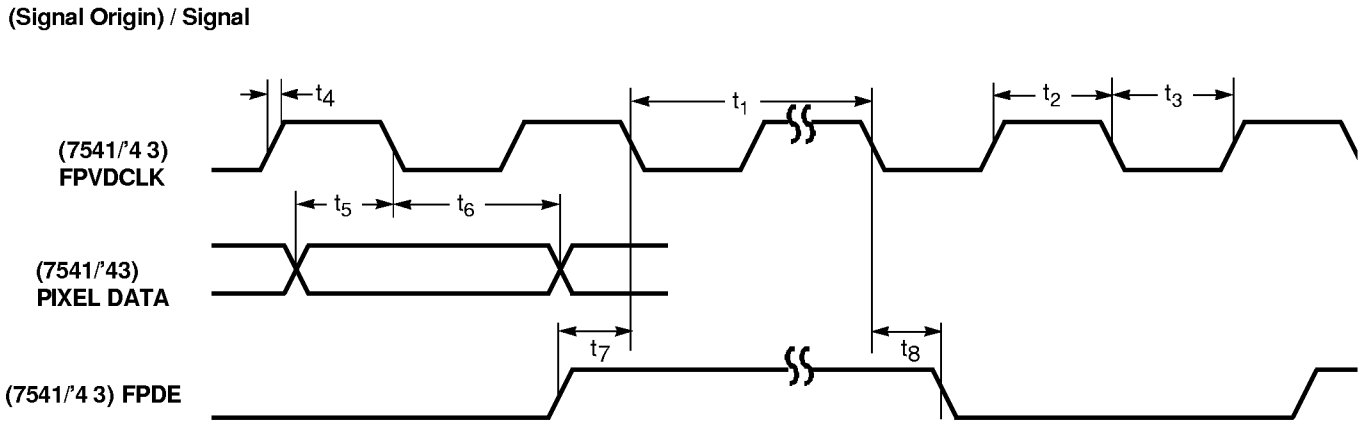


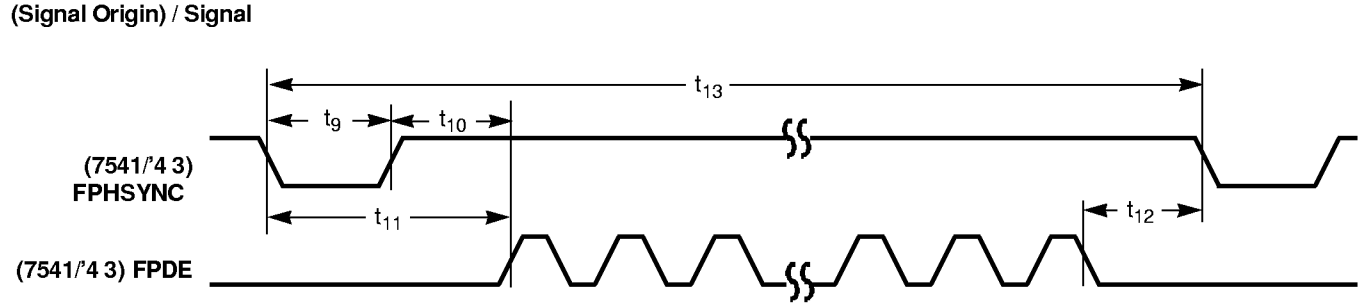
Figure 1 3-20. LCD Interface — Timing for STN Monochrome and Color-Passive LC D

Table 1 3-21. LCD Interface: Timing for TFT Color LCD

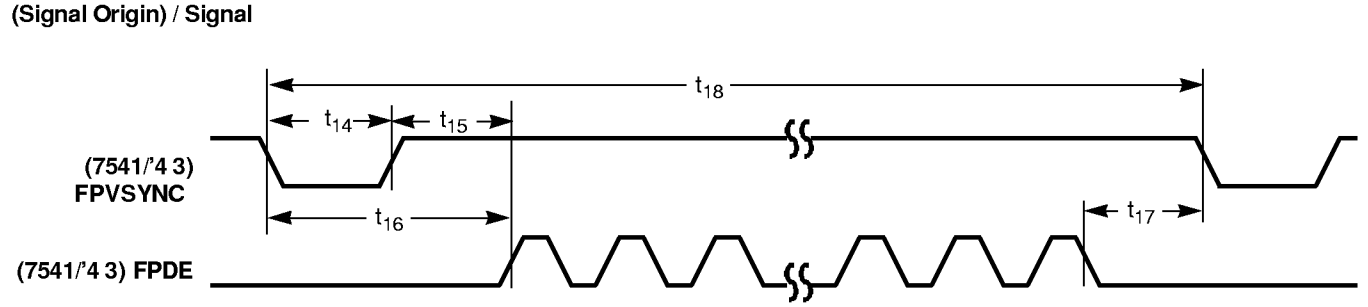
Symbol	Parameter	TFT — C512SS / C4KSS / C256KSS / C16MSS / C64SSI	
		MIN	MAX
t_1	FPVDCLK period	FPVDCLK	
t_2	FPVDCLK high pulse width	$0.5t_1$ – 6 ns	
t_3	FPVDCLK low pulse width	$0.5t_1$ – 6 ns	
t_4	FPVDCLK rise and fall tim e		10 ns
t_5	Data setup time	$0.5t_1$ – 6 ns	
t_6	Data hold time	$0.5t_1$ – 6 ns	
t_7	FPDE setup to FPVDCL K	$0.25t_1$	
t_8	FPDE hold to FPVDCL K	$0.25t_1$	
t_9	FPHSYNC setup to FPVDCL K	$0.25t_1$	
t_{10}	FPHSYNC hold to FPVDCL K	$0.25t_1$	
t_{11}	Horizontal front porc h	0 ns	$96t_1$
t_{12}	Horizontal back porc h	$32t_1$	$128t_1$
t_{13}	FPHSYNC width	$32t_1$	$128t_1$
t_{14}	FPVSYNC setup to FPHSYN C	$1.5t_1$	
t_{15}	FPVSYNC hold to FPHSYN C	$1t_1$	
t_{16}	Vertical front porc h	0 scanlines	30 scanlines
t_{17}	Vertical back porc h	1 scanline	31 scanlines
t_{18}	FPVSYNC width	2 scanlines	2 scanlines



TFT Pixel Data Timing



TFT HSYNC Timing



TFT VSYNC Timing

Figure 1 3-21. LCD Interface — Timing for Single-Scan TFT Color LC D

13.11 Input Timing Diagrams — Frequency Synthesize r

The timing diagram in this section applies to the inputs to the frequency synthesizer. The nominal frequency of the frequency synthesizer is 14.318 MHz, and the nominal period is 69.84 ns

Table 1 3-22. Input Timing — Frequency Synthesize r (14.318 MHz)

Symbol	Parameter	3.30 V		5.00 V	
		MIN	MAX	MIN	MAX
t_1	Input clock rise time	1 ns	7 ns	1 ns	7 ns
t_2	Input clock fall time	1 ns	7 ns	1 ns	7 ns
t_3	Input clock low period	$[t_5 \div 2] - 10\%\ (t_5)$	$[t_5 \div 2] + 10\%\ (t_5)$	$t_5 - 10\%\ (t_5)$	$t_5 + 10\%\ (t_5)$
t_4	Input clock high period	$[t_5 \div 2] - 10\%\ (t_5)$	$[t_5 \div 2] + 10\%\ (t_5)$	$t_5 - 10\%\ (t_5)$	$t_5 + 10\%\ (t_5)$
t_5	Input clock period	69.84 ns – [0.1% of 69.84 ns] = 69.77 ns	69.84 ns + [0.1% of 69.84 ns] = 69.9 ns	69.84 ns – [0.1% of 69.84 ns] = 69.77 ns	69.84 ns + [0.1% of 69.84 ns] = 69.9 ns
V_{IH}	Input high voltage	2.0 V	Vcc	2.0 V	Vcc
V_{IL}	Input low voltage	GND	0.5 V	GND	0.8 V

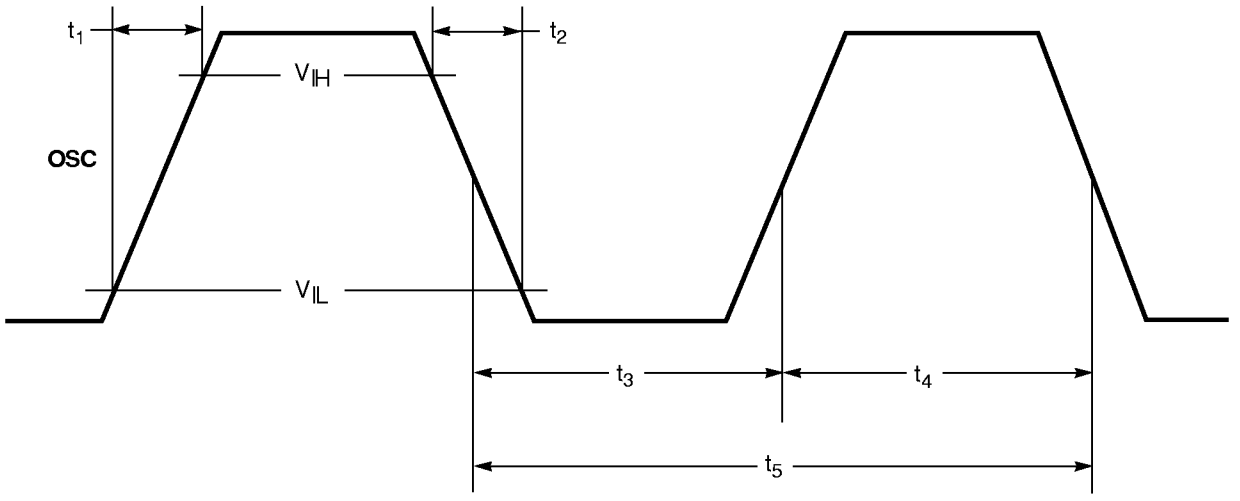
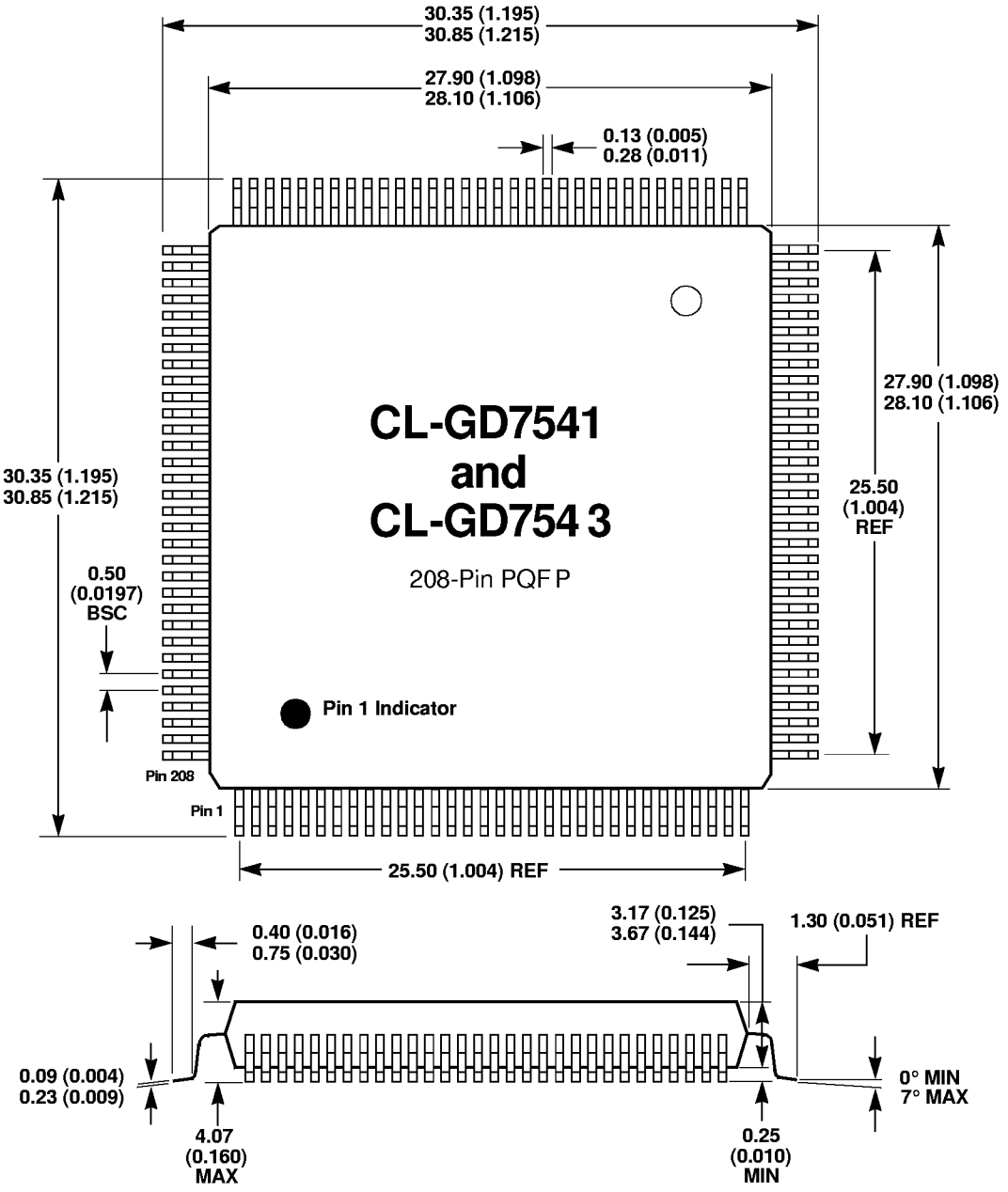


Figure 1 3-22. Frequency Synthesizer — Input Timin g

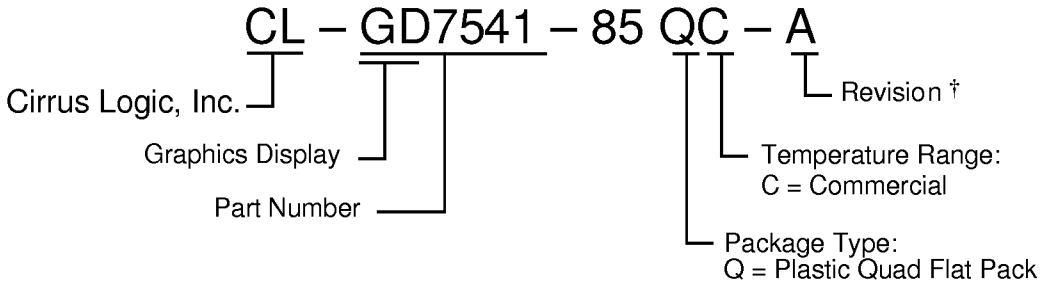
14. PACKAGE SPECIFICATION S



NOTE S:

1) Dimensions are in millimeters (inches), and th e controlling dimension is millimeter .
2) Drawing above does not reflect exact package pin count .
3) Before beginning any new design with this device, please contact Cirrus Logic for the latest package information .

15. ORDERING INFORMATION EXAMPL E



† Contact Cirrus Logic for up-to-date information on revisions.

Appendix A

BitBLT Engine

A.1 Introduction

BitBLT (bit block transfer) is an operation in which one area (source area) of display memory or system memory is copied to another area (destination area) of display memory or system memory.

The CL-GD7541/GD7543 BitBLT engine moves bytes from the source area to the destination area, and it performs 16 logical raster operations to combine the source bytes with the destination bytes. In addition, it can expand a monochrome image into a color image and replicate a single 8-pixel × 8-pixel pattern to fill a large area. These operations are done with minimum CPU intervention.

A.2 Definitions

Source Area:

The source area of a BitBLT is the area from which the data are copied. The source area has the following characteristics:

- Located either in display memory or system memory depending on its address
- May be a monochrome image which is expanded into a color image
- May be a single 8-pixel-by-8-pixel pattern that is replicated to fill a larger area

The source area is never written to except in special cases where the source area and the destination area overlap in display memory.

Destination Area:

The destination area of a BitBLT is the area into which the data are written. The destination area may be in display or system memory.

Width:

The 'width' of a BitBLT refers to the number of bytes (not pixels) in the destination area that are processed before adding the pitch values to the address values. Refer to Figure A-1.

- When the destination area is on the active display screen (that is, when it is a rasterized area that is displayed), then the width is the number of bytes (not necessarily pixels) in each scanline.
- When the destination area is off-screen (or in system memory), the source is a rasterized area, and there is no pattern copy or color expansion, then the width is the number of bytes per scanline of the source.
- When neither the destination nor the source is a rasterized area, then the width is simply the number of bytes that are processed before the pitch values are added to the address values, and it has no special meaning.

Width is specified in the register pair GR20/GR21. The number written into this register pair is one less than the actual desired width. This value is 11 bits, allowing a maximum width of 2048 bytes

Height:

The 'height' of a BitBLT refers to the number of times the pitch values are added to the address values. Refer to Figure A-1.

- When the destination area, source area, or both are on the screen (that is, when either is a rasterized area that is displayed), the height is the number of scanlines in that area.
- When both areas are off-screen, height is simply the number of times the pitch values are added to the address values, and it has no special meaning. In this case, width and height are simply two numbers that are multiplied together to define the number of bytes in the destination.

Height is specified in the register pair GR22/GR23. This value is 10 bits, allowing a maximum height of 1024 scanlines. The number written into the register pair is one less than the actual desired height. The contents of the registers containing the height are not modified during the operation

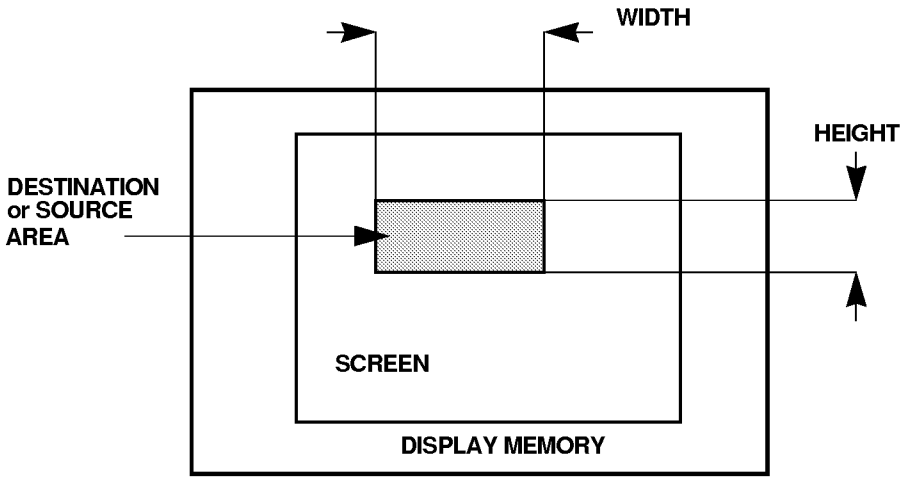


Figure A-1. Width and Height

Pitch:

The 'destination pitch' and 'source pitch' of a BitBLT are the values that are added to the respective addresses after the bytes of each scanline in a destination area have been processed. For the case of a rasterized image, refer to Figure A-2. The destination pitch and the source pitch are specified separately.

- When an area is a rasterized image, the respective pitch is the number of bytes between vertically adjacent pixels. This number is the number of bytes between the (first) pixels of scanline 'n' and scanline 'n+1', that is, the number that is added to the address to get from one scanline to the next.
- When an area is off-screen display memory, the scanlines are often stored in contiguous locations, which minimizes fragmentation. In this case, the respective pitch would be set equal to (width + 1).
- When an area is in system memory, the respective pitch is unused and is a 'don't care'.

When executing BitBLTs with pattern copy or color expansion, the source area is assumed to be linear, and the source pitch is a 'don't care'.

- The source pitch is specified in register pair GR26/GR27.
- The destination pitch is specified in register pair GR24/GR25.

For the CL-GD7541/GD7543, both register pairs are 12-bit values, allowing a pitch of 4095 bytes.

Start:

The 'start' of a BitBLT refers to the address of the first byte of a destination or source area, which is a byte offset from the beginning of display memory. Refer to Figure A-2.

- The destination area start address is specified in register triplet GR28/GR29/GR2A.
- The source area start address is specified in register triplet GR2C/GR2D/GR2E.

Each start address is a 21-bit value, allowing up to 2 Mbytes of display memory. The destination-start address is shown in Figure A-2.

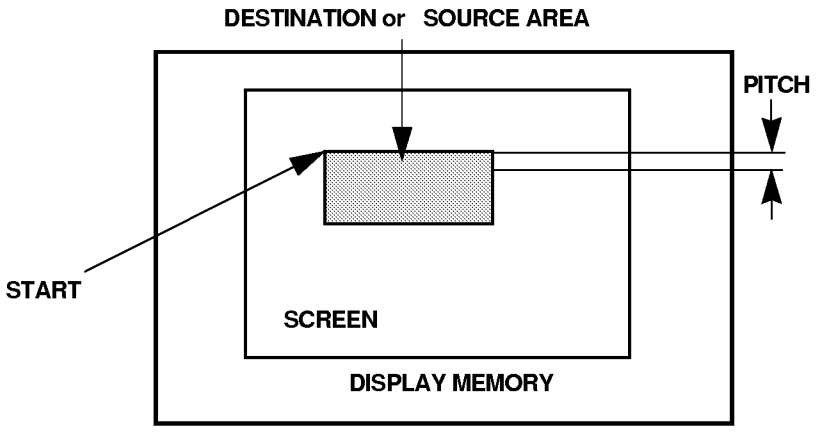


Figure A-2. Pitch and Start

A.3 Example of Display-Memory-to-Display-Memory BitBLT

Table A-1 shows how the BitBLT registers must be programmed for a very simple BitBLT operation of copying a 128-byte × 64-scanline area into display memory. In this example, the CL-GD7541/GD7543 is assumed to be programmed in Video mode 65h (800 × 600, 16 bits per pixel). Therefore, each 128-byte scanline represents 64 pixels. The source area of this operation begins at location 0. The destination area begins at location 160,200 (100 scanlines from the top of the screen, 100 pixels from the left edge).

Table A-1. Register Programming for Source Copy BitBLT Operation

Register(s)	Contents	Field	How Calculated
GR0, GR10	Don't care	Background Color	–
GR1, GR11	Don't care	Foreground Color	–
GR20, GR21	127 (decimal)	Width	(64 × 2) – 1
GR22, GR23	63 (decimal)	Height	64 – 1
GR24, GR25	1,600 (decimal)	Destination Pitch	800 × 2
GR26, GR27	1,600 (decimal)	Source Pitch	800 × 2
GR28, GR29, GR2A	160,200 (decimal)	Destination Start	(100 × 1600) + (100 × 2)
GR2C, GR2D, GR2E	0 (decimal)	Source Start	Beginning of display memory
GR30	00 (hex)	BitBLT Mode	From display to display. No color expansion. No pattern copy.
GR31	02 (hex)	Start/Status	Set bit 1 to '1'
GR32	0D (hex)	Raster Operation	Source copy

This BitBLT is executed as indicated in the following fragment of pseudo-code:

```
sourceAdrs = sourceStartAdrs;
destAdrs = destStartAdrs;
for (i = 0; i < Height; i++)          /*for each scanline*/
    {
    workingSourceAdrs = sourceAdrs
    workingDestAdrs = destAdrs
    for (j =0; j < Width; j++)        /*for each byte*/
         {
         Process one byte of Destination;
         workingDestAdrs++;           /*to next byte*/
         workingSourceAdrs++;
         }
    sourceAdrs = sourceAdrs + sourcePitch; /*next scanline*/
    destAdrs = destAdrs + destPitch;
    }
```

The BitBLT engine processes the bytes of a scanline in a destination area, incrementing temporary source and destination addresses after each byte. Multiple bytes are processed in parallel. At the end of each scanline, the respective pitch values are added to the addresses as they were at the beginning of the scanline, moving on to the next scanline. This operation is iterated for the 'height', the number of times the pitch values are added to the address values.

All BitBLTs are processed in this general manner. However, some variations include the following:

- For color expansion, the source address is incremented as a bit address rather than a byte address.
- For pattern copies, the source address is incremented until the end of the pattern and is returned to the source start address, so that the pattern is used over and over.
- When the decrement bit is set, the address is decremented rather than incremented.

A.4 Raster Operations (ROPs)

In addition to moving bytes from the source area to the destination area, the CL-GD7541/GD7543 BitBLT engine can use various logical raster operations to combine the source or pattern bytes with the destination bytes. Further, bytes in either the source area or the destination area, or both, can be ignored.

Table A-2 enumerates the 16 ways in which the source bit (or the pattern bit) and the destination bit can be logically combined. The same value for GR32 is used regardless of whether the operation uses Source or Pattern.

The CL-GD7541/GD7543 BitBLT engine directly implements all 16 ways of logically combining two operands as shown in Table A-2. Combinations of three operands can be synthesized from these operands in the unusual cases for which this is necessary.

Table A-2. Logical Combinations of Bits Using the BitBLT Engine

Source Operation	Microsoft® Name / Raster Operation	Pattern Operation	Microsoft® Name / Raster Operation	GR32 (Hex)
0	BLACKNESS 00000042	0	BLACKNESS 00000042	00
~S.~D	NOTSRCERASE 001100A6	~P.~D	– 000500A9	90
~S.D	– 00220326	~P.D	– 000A0329	50
~S	NOTSRCCOPY 00330008	~P	– 000F0001	D0
S.~D	SRCERASE 00440328	P.~D	– 00500325	09
~D	DSTINVERT 00550009	~D	DSTINVERT 00550009	0B
S~=D	SRCINVERT 00660046	P~=D	PATINVERT 005A0049	59
~S+~D	– 007700E6	~P+~D	– 005F00E9	DA
S.D	SRCAND 008800C6	P.D	– 00A000C9	05
S=D	– 00990066	P=D	– 00A50065	95
D	– 00AA0029	D	– 00AA0029	06
~S+D	MERGEPAINT 00BB0226	~P+D	– 00AF0229	D6
S	SRCCOPY 00CC0020	S	PATCOPY 00F00021	0D
S+~D	– 00DD0228	P+~D	– 00F50225	AD
S+D	SRCPAINT 00EE0086	P+D	– 00FA0089	6D
1	WHITENESS 00FF0062	1	WHITENESS 00FF0062	0E

NOTE: S = Source, D = Destination, P = Pattern .

A.5 Color Expansion

When GR30[7] is '1', the source input to the ROPS is not actual data from the source area, but is *color-expanded* data. The source area is a monochrome image. Since the source image is a single bit per pixel, substantial performance benefits are possible, especially when the source is being expanded to 16 bits. Color expansion can be used any time a single foreground color, or a single foreground color and a single background color, are to appear in the destination.

The CL-GD7541/GD7543 supports color expansion for 8- and 16-bit-per-pixel modes. The source can be monochrome data from either display memory or system memory. When the source is in display memory, it must be located on a 4-byte boundary. When the source is an 8 × 8 pattern, it must be on an 8-byte boundary.

- A '1' in the source area results in the *foreground* color being written into corresponding byte(s) of the destination area.
- A '0' in the source area results in either the *background* color being written into corresponding byte(s) of the destination area, or no alteration to the destination area (transparency).

For color expansion, the destination must be in the display memory that is displayed and the direction must be incremental. Any ROP may be used, although SRCCOPY is most common when using color expansion.

The most-significant bit of the first source byte is expanded into the ROP source data for the first pixel of the destination. Depending on the contents of GR30[4], it is expanded to 1 or 2 bytes. Table A-3 indicates the registers that contain the expansion colors.

Table A-3. Color Expansion Registers

GR30[4]	Width	Background Expansion (0 in Source Area)		Foreground Expansion (1 in Source Area)	
		GR0	GR10	GR1	GR11
0	8-bit	Color	Don't care	Color	Don't care
1	16-bit	Low byte	High byte	Low byte	High byte

The next bit of source data is processed for the next 1 or 2 bytes of destination, and so on, until the bytes of the scanline in the destination area have been processed. Unused source bits are discarded.

The destination address is modified by the destination pitch. The source pitch is ignored since the source is taken to be a linear string of bytes. The next byte of source is the first 8 pixels for the next scanline.

A.6 Color Expansion with Transparency

When GR30[3] is '1', transparency comparison is enabled. For each pixel, results of a ROP are compared to the contents of the Transparent Color registers (Extension registers GR34 and GR35). When the results are compared in all bit positions for which the Transparent Compare Mask registers (Extension registers GR38 and GR39) are 0, the results are *not* written to display memory. In 8 bits/pixel modes (that is, Extension register GR30[4] = '0'), registers GR34 and GR35 *must* be programmed identically, as must GR38 and GR39.

When color expansion is used with an opaque foreground and a transparent background (analogous to Extended Write mode 4), the transparency feature must be used, and the transparent color must be set to the background color. The registers used for foreground color expansion with transparency are the same as the color expansion registers with '1' in the source.

A.7 Pattern Fills

In some cases it is necessary to fill an area with a repeating pattern. The CL-GD7541/GD7543 BitBLT engine has provisions for pattern replication with or without color expansion. The pattern size is 8 pixels × 8 pixels, chosen for compatibility with Microsoft Windows.

When GR30[6] is '1', the source is defined as an array of 8 × 8 pixels. This array is repeatedly copied to the destination area, with color expansion if necessary. For any scanline, the same eight pixels of source data are used repeatedly. The source pitch is ignored. The number of bytes in the source pattern is a function of the operating mode, as indicated in Table A-4. The starting address boundary of a source pattern is equal to the number of bytes in the source pattern.

Table A-4. Pattern-Fill Data Size

Operating Mode	Number of Bytes in Source Pattern	Starting Address Boundary
Color Expansion	8 bytes of monochrome data for 64 pixels	8 bytes
8-bit pixels	64 bytes of color data for 64 pixels	64 bytes
16-bit pixels	128 bytes of color data for 64 pixels	128 bytes
32-bit pixels	256 bytes of color data for 64 pixels	256 bytes

A.8 BitBLT Direction

If source and destination areas overlap in display memory, as explained below, ensure that the BitBLT operation progresses so that the source area is not overwritten prior to being used.

Refer to Figure A-3. If the BitBLT operation were to begin with the upper-left corner of the source and destination, the contents of the overlapped area would be overwritten before being used.

To avoid this effect, GR30[0] must be set to '1' so that the direction in which the BitBLT operation progresses is reversed. As shown in Figure A-3, the bytes are therefore processed right to left and bottom to top, guaranteeing that bytes of the source are used prior to being changed. Note that in this case, the start addresses are the highest in the areas, not the lowest.

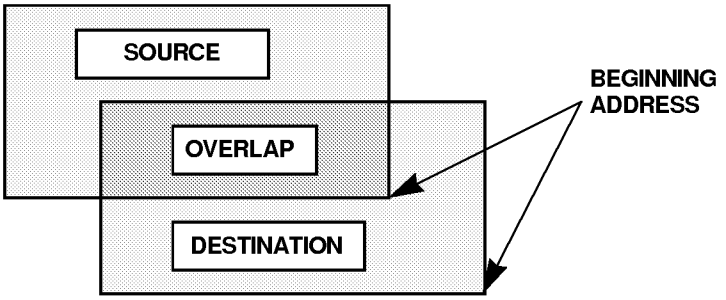


Figure A-3. Source and Destination Memory Area Overlap — Start Address

A.9 System Memory

The source area or the destination area, but not both, of a BitBLT can be in system memory. In either case, the CPU must perform the bus transfers in that the CL-GD7541/GD7543 is never a bus master. For such transfers, the address provided by the CPU is ignored (except it must be in the range being decoded as display memory). The CPU *must* execute DWORD transfers.

- When Extension register GR30[2] is a '1', the BitBLT source is system memory.
  - For system-to-screen BitBLTs, up to 3 bytes of the last transfer for each scanline are ignored (depending on width of the source and the destination areas). The next scanline begins with the next DWORD transfer.
- When Extension register GR30[1] is a '1', the BitBLT destination is system memory.
  - The CL-GD7541/GD7543 pads each scanline with up to 3 indeterminate bytes (depending on width of the source and the destination areas). BitBLTs involving color expansion or pattern copy cannot use this mode.

A.10 Start, Suspend, and Reset Controls

Once the parameters have been loaded into the registers, the BitBLT can be started, suspended, and then resumed. It is also possible to unconditionally reset the BitBLT engine. These functions are controlled by bits in GR31.

- To start a BitBLT, program Extension register GR31[1] to '1'. As long as the BitBLT is in progress, GR31[0] is '1'. When the BitBLT has completed, GR31[0] changes to a '0'.

  Monitoring GR31[0] is the most straightforward way to synchronize with the BitBLT engine. While the BitBLT is in progress, the CL-GD7541/GD7543 display memory and BitBLT registers (except GR31) must not be accessed for read or write.

- To suspend a BitBLT, program GR31[1] to '0'. Register GR31[0] must be monitored to determine when the BitBLT has actually been suspended and it is safe to access display memory. When register GR31[0] is '0', then the BitBLT has been successfully suspended or has been completed.

  When a BitBLT has been suspended, the CPU may access display memory only for write operations. If the program reads display memory during a suspended BitBLT, working registers are overwritten, and the first few bytes of the BitBLT use invalid data when the BitBLT resumes.

  The CPU can determine whether a suspended BitBLT was actually suspended, or gone to completion coincidentally with the suspension, by reading GR31[3].

  — When GR31[3] is '1', the BitBLT was suspended and must be resumed.

  — When GR31[3] is '0', the BitBLT was actually completed and need not be resumed.

- To resume a BitBLT, program GR31[1] to '1'. BitBLTs can be suspended and resumed multiple times.

- To unconditionally stop the current operation and reset the entire BitBLT engine, program GR31[2] to '1'. GR31[3] and GR31[0] are forced to '0' and the operation stops after the next write. This operation may result in partial pixels being written.

NOTE: A BitBLT operation that is reset *cannot* be resumed.

A.11 Complet e BitBLT Register Listin g

Table A-5 lists every register associated with the BitBLT engine.

Table A-5. BitBLT Register Listin g

Register	How Used	Size (Bits)	Modified?
GR0	Background Color byte 0	8	No
GR1	Foreground Color byte 0	8	No
GR10	Background Color byte 1	8	No
GR11	Foreground Color byte 1	8	No
GR20	Width byte 0	8	–
GR21	Width byte 1	3	–
GR22	Height byte 0	8	Yes
GR23	Height byte 1	2	Yes
GR24	Destination Pitch byte 0	8	No
GR25	Destination Pitch byte 1	4	No
GR26	Source Pitch byte 0	8	No
GR27	Source Pitch byte 1	4	No
GR28	Destination Start byte 0	8	Yes
GR29	Destination Start byte 1	8	Yes
GR2A	Destination Start byte 2	5	Yes
GR2B	Reserved		
GR2C	Source Start byte 0	8	Yes
GR2D	Source Start byte 1	8	Yes
GR2E	Source Start byte 2	5	Yes
GR2F	Reserved	–	–
GR30	BitBLT mode	8	No
GR31	Start/Status	4	–
GR32	Raster Operatio n	8	No
GR34	Transparent Color – Low Byt e	8	No
GR35	Transparent Color – High Byt e	8	No
GR38	Transparent Color Mask – Low Byt e	8	No
GR39	Transparent Color Mask – High Byt e	8	No
SR2	Plane Mask	8	No

A.12 BitBLT Registers Modified While BitBLT Is Occurrin g

Some registers associated with a BitBLT are modified while the BitBLT is occurring. Therefore, they must be re-written prior to the next BitBLT, even when the initial values are to be the same.

A.13 Text Expansion Example

Using color expansion, a text string is copied from system memory, resulting in faster text-write operations. The monochrome image of the string is arranged in system memory by scanline. For example, assume that the destination area is 150 pixels × 25 scanlines, 8 bits per pixel. The destination pitch is 1024 pixels. The registers must be loaded as indicated in Table A-6. When the background pixels are not to be written, GR30[3] must be set to '1'.

Table A-6. Typical Register Settings for Color-Text Expansion

Register(s)	Contents	Field	How Calculated
GR0, GR10	'Don't care'	Background Color	–
GR1, GR11	'Don't care'	Foreground Color	–
GR20, GR21	149 (decimal)	Width	150 pixels – 1 pixel = 149 pixels
GR22, GR23	24 (decimal)	Height	25 scanlines – 1 scanline = 24 scanlines
GR24, GR25	1024 (decimal)	Destination Pitch	–
GR26, GR27	Not applicable	Source Pitch	(System memory)
GR28, GR29, GR2A	'Don't care'	Destination Start	–
GR2C, GR2D, GR2E	Not applicable	Source Start	(System memory)
GR30	84 (hex)	BitBLT Mode	Color Expansion, Source = System Memory
GR31	02 (hex)	Start/Status	Set bit 1 to '1'
GR32	0D (hex)	Raster Operation	Source copy

After the registers are loaded, the source bitmap must be transferred.

- The first DWORD write transfers the image for pixels 0 to 31.
- The second write transfers the image for pixels 32 to 63.
- The third transfers the image for pixels 64 to 95.
- The fourth transfers the image for pixels 96 to 127.
- The data sent in the fifth DWORD transfer is shown in Figure A-4.

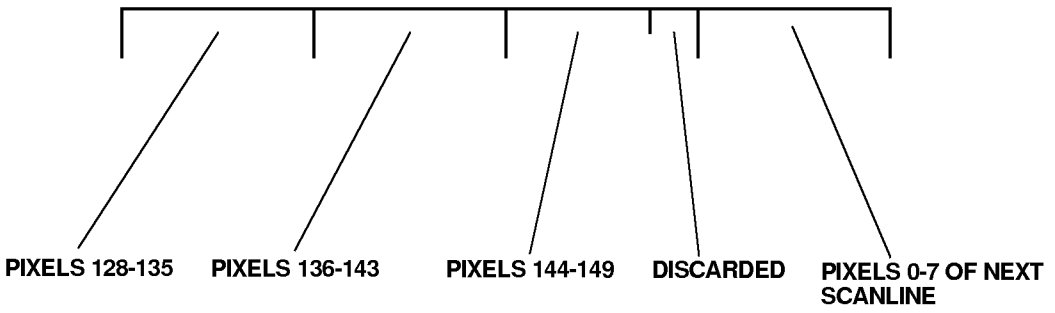


Figure A-4. Color Expand Transfer

A total of 119 DWORD transfers are required. The last 1 byte of the last transfer is discarded.

Appendix B

Hardware Cursor

B.1 Introduction

The CL-GD7541/GD7543 is capable of supporting a 32 × 32 or 64 × 64 hardware cursor (mouse pointer) in 16-color planar, 256-, 32K-, and 64K-color packed-pixel graphics modes.

Multiple hardware cursor patterns can be loaded into the upper display memory area, allowing application programs to select one of the patterns as an active-cursor pattern.

The hardware cursor (mouse pointer) replaces a software mouse pointer commonly used by (GUI)graphics user interface applications. The hardware cursor eliminates the need for application software to save and restore the screen data as the mouse pointer position changes.

After initializing the hardware cursor, the application software need only update the cursor position (x,y) to move the cursor on the screen. Compared to a software cursor, the hardware cursor offers a smooth-moving mouse pointer with improved performance.

B.2 Hardware Cursor Operation

Each pixel in the hardware cursor consists of two bits: bit 1 and bit 0. The following table shows how the 2 bits determine the displayed data of each cursor pixel.

Table B-1. Hardware Cursor Bits

Bit 0	Bit 1	Displayed Data of Hardware Cursor Pixel
0	0	Transparent cursor pixel
0	1	Inverted VGA display data
1	0	Cursor color 0
1	1	Cursor color 1

The cursor colors 0 and 1 are supplied by the internal palette DAC two extra Lookup Table (LUT) locations, which are mapped into the existing LUT indexes 00h and 0Fh, respectively. As a result, the hardware cursor colors are independent of the existing LUT indexes 00h through FFh.

Extension register SR12 can be programmed:

- To enable or disable the cursor
- To select the cursor size
- To enable access to the palette DAC cursor colors
- To enable cursor movement

The hardware cursor data is located in the top 8 Kbytes of the display memory. The number of cursor patterns that can be loaded in the display memory at one time is either 32 (for 32 × 32-bit cursors) or 8 (for 64 × 64-bit cursors). One of the cursor patterns loaded in display memory is selected as the active-cursor pattern by programming Extension register SR13.

The hardware cursor position is controlled by programming the hardware cursor horizontal (X) position and hardware cursor vertical (Y) position. The 11-bit cursor X-location and Y-location values are programmed by initiating two 16-bit I/O writes to:

- Sequencer register SRX (3C4h) and Extension register SR10 (3C5h): Horizontal position
- Sequencer register SRX (3C4h) and Extension register SR11 (3C5h): Vertical position

The SRX[7:5] bits of the Sequencer Index register are the least-significant 3 bits of the 11-bit value. The SRX[4:0] bits of the Sequencer Index register are the index into the horizontal and vertical position registers. Moving the cursor always requires writing to both the horizontal and vertical position registers. The horizontal position is written first, but it does not take effect until the vertical position is updated

NOTE: The horizontal fine-position control requires one more bit for expanded-graphics modes that use 10-dot character clocks. For special cases (for example, if 640 × 480 graphics are expanded for use on 800 × 600 LCDs), the most-significant bit for the fine-position adjustment is in Extension register SR2E[0]. This bit is appended to Sequencer register index bits SRX[7:5]. For standard non-expanded graphics modes, Extension register SR2E[0] is always '0' and can be ignored when moving the cursor.

The following table shows the CL-GD7541/GD7543 registers that are needed for programming the hardware cursor:

Table B-2. Registers for Programming Hardware Cursor

To:	Program:			
	Register	I/O Port Address	Register Bits	Value
Enable hardware cursor	SR12	3C5h	[0]	1
Access graphics palette DAC colors	SR12	3C5h	[1]	1
Set hardware cursor size (32 × 32)	SR12	3C5h	[2]	0
Set hardware cursor size (64 × 64)	SR12	3C5h	[2]	1
Enable hardware cursor movement	SR12	3C5h	[3]	0
Select hardware cursor pattern (32 × 32)	SR13	3C5h	[4:0]	31...0
Select hardware cursor pattern (64 × 64)	SR13	3C5h	[4:2]	7.0
Set hardware cursor horizontal position	SRX/SR10, 30, 50, 70, 90, B0, D0, F0	3C4h/3C5h	[7:5]/[7:0]	2047...0
Set hardware cursor horizontal position fine-position extension (MSB) for expanded graphics	SR2E	3C5h	[0]	0: Non-Expanded 1: Expanded
Set hardware cursor vertical position	SRX/SR11, 31, 51, 71, 91, B1, D1, F1	3C4h/3C5h	[7:5]/[7:0]	2047...0
Enable 64 × 64 hardware cursor memory mapping	SR21	3C5h	[4]	1

B.3 The 32 × 32 Hardware Cursor

Each 32 × 32 cursor pattern requires 256 bytes (128 bytes per cursor pixel bit × 2 cursor pixel bits), which allows for 32 cursor patterns to be loaded into 8 Kbytes of the hardware cursor data area in the display memory. The active cursor pattern is selected by programming Extension register bits SR13[4:0].

The hardware cursor data and the hardware icon data are loaded into the top 16 Kbytes of the display memory as follows:

- The hardware cursor data is loaded into the top 8 Kbytes of the display memory.
- The hardware icon data is loaded into the next 8 Kbytes of the display memory.

For more information about the hardware icon, refer to Appendix C.

The 32 × 32 hardware cursor pattern data from cursor pixel bit 0 and cursor pixel bit 1 is loaded into the display memory as shown in the following figure:

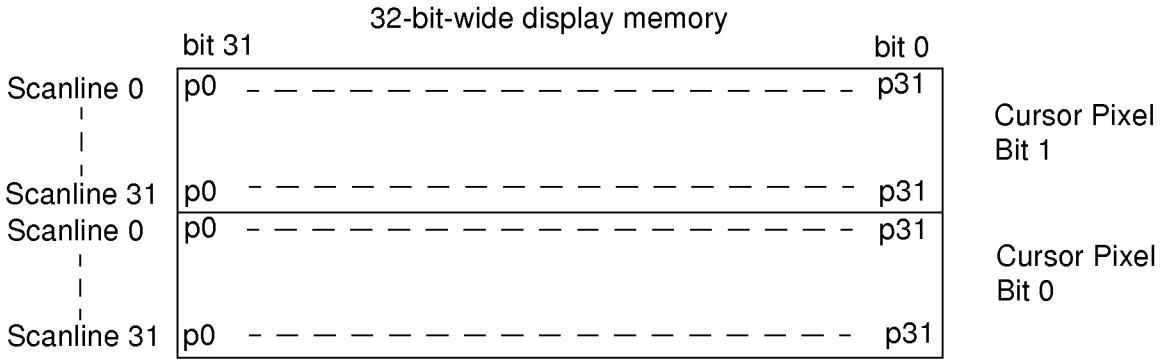


Figure B-1. Mapping of 32 × 32 Hardware Curso r

B.4 The 64 × 64 Hardware Curso r

Each 64 × 64 cursor pattern requires 1024 bytes (512 bytes per cursor pixel bit × 2 cursor pixel bits), which allows for 8 cursor patterns to be loaded into 8 Kbytes of the hardware cursor data area. The active hardware cursor pattern is selected by programming Extension register bits SR13[4:2].

The 64 × 64 hardware cursor pattern data from cursor pixel bit 0 and cursor pixel bit 1 is loaded into display memory one cursor scanline at a time. The same action occurs until all 64 scanlines from cursor pixel bit 0 and cursor pixel bit 1 are loaded into the system memory as shown in the following figure:

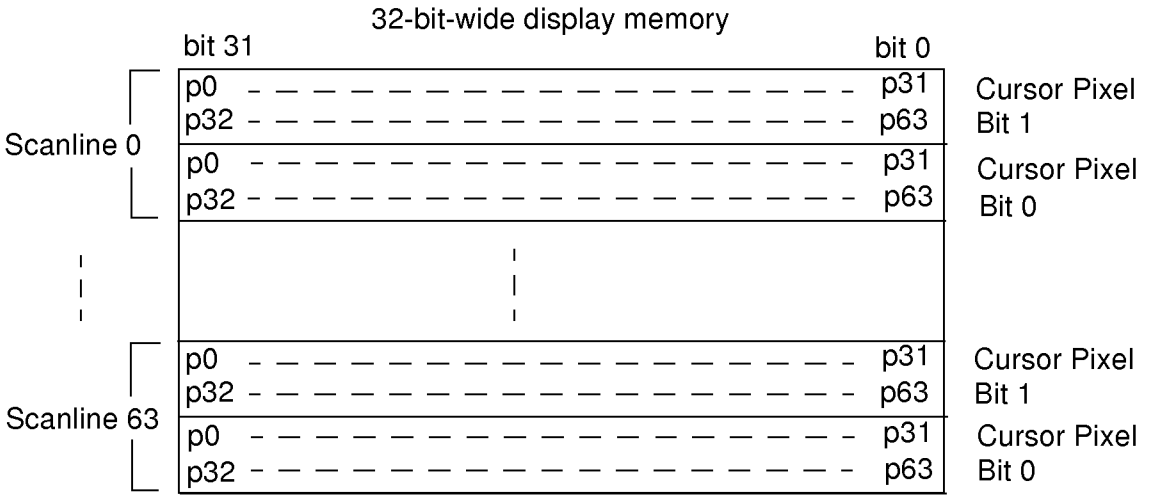


Figure B-2. Mapping of 64 × 64 Hardware Curso r

To obtain proper 64 × 64 hardware cursor mapping, Extension register bit SR21[4] must be set to '1'.

The following table shows the location of the hardware cursor memory map within the display memory.

Table B-3. Hardware Icon Memory Map in 1-Mbyte Display Memory

Address	32 × 32 Hardware Cursor	64 × 64 Hardware Cursor
3FF00–3FFFF	Cursor Map #28 — Cursor Map #31	Cursor Map #7
3FE00–3FEFF	Cursor Map #24 — Cursor Map #27	Cursor Map #6
3FD00–3FDFF	Cursor Map #20 — Cursor Map #23	Cursor Map #5
3FC00–3FCFF	Cursor Map #16 — Cursor Map #19	Cursor Map #4
3FB00–3FBFF	Cursor Map #12 — Cursor Map #15	Cursor Map #3
3FA00–3FAFF	Cursor Map #8 — Cursor Map #11	Cursor Map #2
3F900–3F9FF	Cursor Map #4 — Cursor Map #7	Cursor Map #1
3F800–3F8FF	Cursor Map #0 — Cursor Map #3	Cursor Map #0

NOTE: For the 32 × 32 hardware cursor, four hardware-cursor data patterns occupy 3Fx00 through 3FxFF. Their respective addresses (x = 8 – F) are:
3Fx00–3Fx3F
3Fx40–3Fx7F
3Fx80–3FxBF
3FxC0–3FxFF

The addresses in the table above assume that each location is 32 bits wide.

Appendix C

Hardware Icon

C.1 Introduction

A hardware icon (a hardware-driven icon window), as compared to a software icon, eliminates the need for application software to save and restore the screen data as the icon position changes

In various operational modes, the CL-GD7541/GD7543 is capable of supporting four hardware icons with the following features:

- One to four icons displayed simultaneously on the screen.
- Icon size is 64 × 64 pixels.
- Icon size can be doubled vertically and/or horizontally to the following:
  - 64 × 128 pixels
  - 128 × 64 pixels
  - 128 × 128 pixels
- Up to eight icon maps may be defined in display memory for use and are associated with the displayed hardware icons in two ways:
  - Two maps for each hardware icon
  - All eight maps used with the first hardware icon
- A single location known as a hot spot is used to define the screen position of all of the icons. This 'hot spot' defines the upper left-hand corner of the first icon. All subsequent icons are left-aligned vertically down from the first icon.
- The hot spot is positioned at a resolution of one pixel.
- Each icon independently controls the following:
  - Display Enable
  - Display Mode: 4-color mode, or 3-colors-and-transparency mode
  - Blink Enable: at either blink rate, or at one-half the icon blink rate
  - Horizontal Pixel Doubling
  - Vertical Pixel Doubling
  - Memory Map Selection
- The hardware icons have the second most display priority in the video sub-system. Only the hardware cursor appears on top of the icon.

The hardware icon memory model and programming model are very similar in usage to that of the hardware cursor. The memory used to define the icon maps is at the top of the available display memory space (just below the hardware cursor area), and it is fixed by the CL-GD7541/GD7543.

C.2 Hardware Icon Operation

The CL-GD7541/GD7543 Video Data Path Control register (Extension register SR12), and Hardware Icon Control registers (Extension registers SR2A/SR2B/SR2C/SR2D) can be programmed for the following:

- To enable/disable the icon
- To select the icon size
- To enable access to the palette DAC icon colors
- To enable icon movement.

The hardware icon data is located in the bottom 8 Kbytes of the of the top 16 Kbytes of available display memory. The number of icon patterns that can be loaded in the display memory at one time is eight 64× 64-bit icons (of which four can be simultaneously displayed). These patterns can be defined as either two patterns per icon, or all eight patterns can be displayed on the first icon, allowing all of the patterns to be displayed at the same location without having to update the icon hot spot.

C.2.1 Icon Color

Each hardware icon pixel consists of 2 bits, icon pixel bit 0 and icon pixel bit 1. Table C-1 shows how these 2 bits determine the displayed state of each icon pixel.

Table C-1. Hardware Icon Pixel Bits

Icon Pixel Bit 0	Icon Pixel Bit 1	Displayed Data of Hardware Icon Pixel
0	0	Icon color 0 (Transparent)
0	1	Icon color 1
1	0	Icon color 2
1	1	Icon color 3

The icon colors 0 and 3 are supplied by the internal palette DAC's four extra lookup table (LUT) locations, which are mapped into the existing LUT indexes 03h, 04h, 05h, and 06h, respectively. As a result, the hardware cursor colors are independent of the existing LUT indexes 00h through FFh.

- When Extension register SR12[1] is set to '1', these four additional palette locations are enabled and are accessible the same way as their standard VGA counterparts.
- Clearing Extension register SR12[1] to '0' restores standard VGA operation to the palette locations.

C.2.2 Icon Position

The hardware icon position is controlled by programming the Graphics Icon Horizontal (X) position and Graphics Icon Vertical (Y) position. The position of the hardware icon is programmed in the same way as for the hardware cursor, using the same I/O addresses. The CL-GD7541/GD7543 distinguishes the difference between the two operations by the state of Extension register bit SR12[3].

- When SR12 [3] = '0', writing X and Y position data controls the position of the hardware cursor.
- When SR12 [3] = '1', writing X and Y position data controls the position of the hot spot of the hardware icons.

The 11-bit icon X-and Y-location values are programmed by initiating two 16-bit I/O writes to:

- SRX (3C4h) and SR10 (3C5h): Horizontal position
- SRX (3C4h) and SR11 (3C5h): Vertical position

where SRX[7:5] of the Index register are the least-significant bits of the 11-bit value, and SRX[4:0] is the index into the horizontal and vertical position registers. Moving the icon always requires writing to both the horizontal and vertical position registers. The horizontal position is written first, but it does not take effect until the vertical position is updated.

NOTE: The horizontal fine-position control requires one more bit for those expanded graphics modes that use 10-dot character clocks. For these special cases (for example, 640 × 480 graphics expanded for 800 × 600 panels), the most-significant bit for the fine-position adjustment is in SR2A[6], which is appended to the index bits SRX[7:5]. For standard non-expanded graphics modes, SR2A[6] is always '0' and can be ignored when moving the icon.

Figure C-1 shows the hot spot and vertical alignment of the icons as they appear on the display.

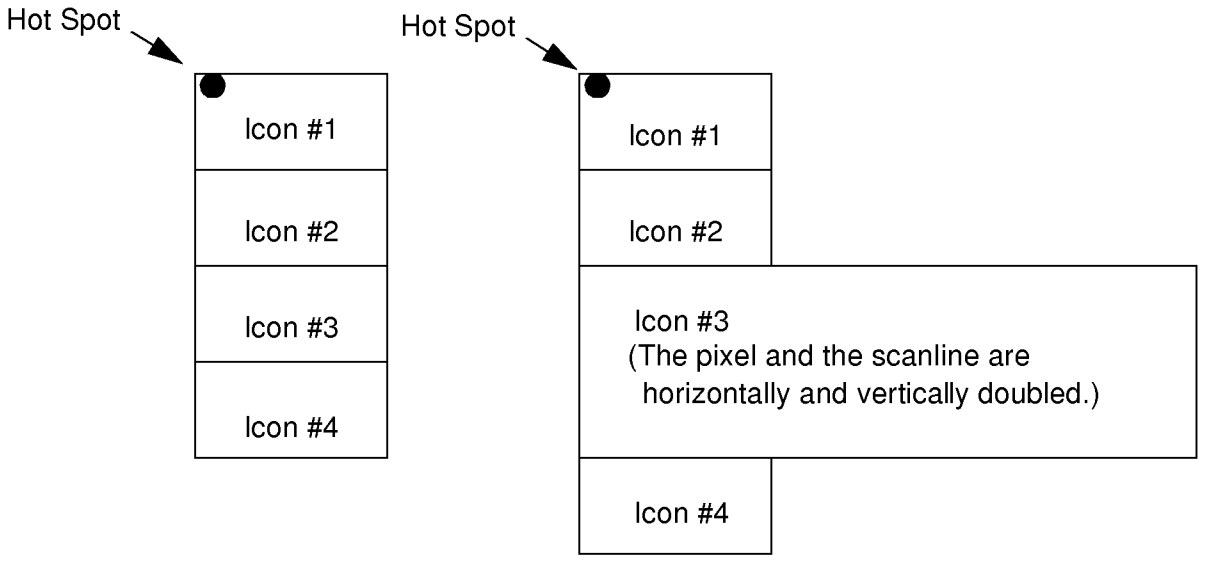


Figure C-1. Hot Spot and Vertical Alignment of the Icons

Table C-2 shows the CL-GD7541/GD7543 Extension register bits for programming the hardware icon.

Table C-2. Extension Register Bits for Programming Hardware Icon

To:	Program:			
	Register	I/O Port Address	Register Bits	Value
Enable hardware icon	SR2x[a]	3C5h	[0]	1
Display 3-colors-and-transparency modes	SR2x[a]	3C5h	[1]	1
Display 4-color modes	SR2x[a]	3C5h	[1]	0
Enable blink	SR2x[a]	3C5h	[2]	1
Double horizontal pixel	SR2x[a]	3C5h	[3]	1
Double vertical scanline	SR2x[a]	3C5h	[4]	1
Select memory map	SR2x[a]	3C5h	[5]	0 or 1
Select icon #0 eight memory maps option	SR2E	3C5h	[2:1]	11, 10, 01, 00
Set hardware icon horizontal position[b]	SRX/SR10, 30, 50, 70, 90, B0, D0, F0	3C4h/3C5h	[7:5]/[7:0]	2047...0
Set icon horizontal position fine-position extension (most-significant bit) for expanded graphics	SR2A	3C5h	[6]	0: Non-Expanded 1: Expanded
Set hardware icon vertical position[b]	SRX/SR11, 31, 51, 71, 91, B1, D1, F1	3C4h/3C5h	[7:5]/[7:0]	2047...0

[a] The x represents the four available icon programming registers; 2Ah, 2Bh, 2Ch, and 2Dh, which correspond to the four hardware icons of the CL-GD7541/GD7543.

[b] The icon position is programmed the same way as the hardware cursor, using the same I/O addresses. The state of SR12[3] determines whether the icon position or the cursor position are to be updated.

C.2.3 Memory Map Option

According to the setting of Extension register SR2E[2:1], the eight CL-GD7541/GD7543 icon maps can be configured in two ways:

- Two maps per icon
- All eight maps available to icon #0

Extension register SR2E[2:1] controls this configuration option as follows:

- When this field is zero, the corresponding map pair that is displayed is icon #0.
- When this field is non-zero:
  - Only icon #0 can be used, and it has accesses to all eight memory maps. The non-zero number points to the corresponding map pair that is displayed as icon #0.
  - Icons #1, #2, and #3 must be disabled.

The member of the map pair that is actually displayed is selected by the state of SR2A[5]. For example, if SR2E[2:1] = '11' and SR2A[5] = '0', then map #6 is displayed as icon #0. For memory map details, refer to Table C-3.

C.3 Hardware Icon Memory Map and Data Format

Table C-3 shows the location of the hardware icon memory maps within the display memory.

Table C-3. Hardware Icon Memory Map in 1-Mbyte Display Memory

Address	Hardware Icon Memory Map
3F700–3F7FF	Icon #3 Map #1 or Icon #0 Map #7
3F600–3F6FF	Icon #3 Map #0 or Icon #0 Map #6
3F500–3F5FF	Icon #2 Map #1 or Icon #0 Map #5
3F400–3F4FF	Icon #2 Map #0 or Icon #0 Map #4
3F300–3F3FF	Icon #1 Map #1 or Icon #0 Map #3
3F200–3F2FF	Icon #1 Map #0 or Icon #0 Map #2
3F100–3F1FF	Icon #0 Map #1
3F000–3F0FF	Icon #0 Map #0

NOTE: The above addresses assume each location is 32 bits wide.

The actual data that is stored in display memory to define the icon is written with two bits of data per pixel, as defined in Section C.2.1. The following figure shows how the 64-pixel-by-64-pixel icon is stored in 32-bit-wide display memory.

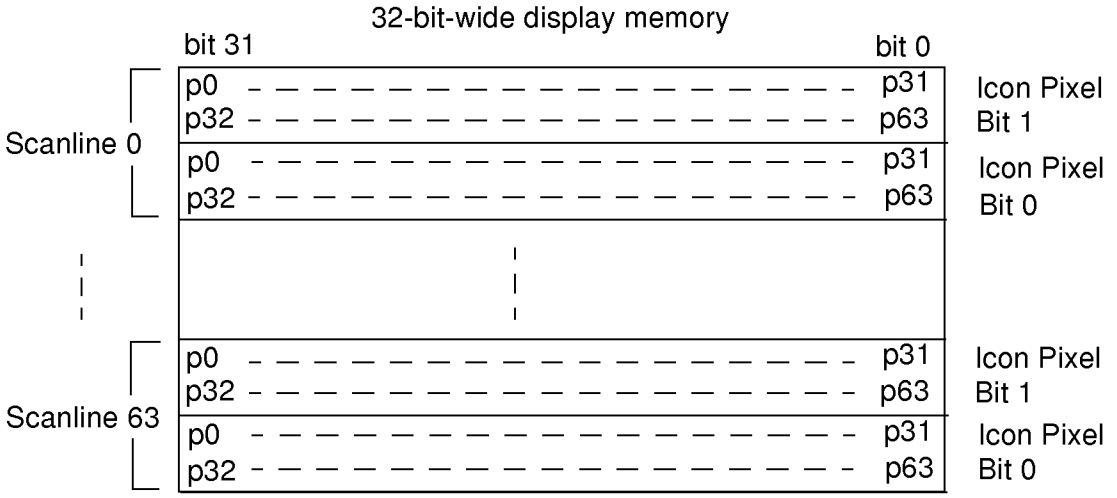


Figure C-2. Icon (64 Pixels × 64 Pixels) Stored in the Display Memory

Appendix D

Color Expansion and Extended Write Modes

D.1 Introduction

The CL-GD7541/GD7543 supports color expansion, which uses extended write modes for faster CPU write performance. In graphics modes, extended write modes can be used for the following operations: faster text write, pattern fill, and block move operations. In 8- or 16-bit-per-pixel graphics modes with packed-pixel addressing, these extended write modes operate on 8 pixels at a time.

D.2 Color Expansion

Color expansion is the automatic conversion of a monochrome bitmap, typically defining a character, icon, or pattern into foreground and background color values that are written into display memory. The foreground and background color values are held in the CL-GD7541/GD7543, and only the monochrome bit maps need to be transmitted across the bus. Each bit of the monochrome map is converted into an 8-bit or 16-bit pixel value: The bus traffic is reduced accordingly.

D.3 Registers Involved in Color Expansion

The following registers are involved in color expansion.

Table D-1. Color Expansion Registers

Register Bit	Function
SR2[7:0]	Enable writing pixels
GRB[2]	'1' enables Extended Write modes
GRB[4]	'1' enhances Extended Write modes to 16-bit pixels
GR5[2:0]	'100' chooses Extended Write mode 4 '101' chooses Extended Write mode 5
GR0[7:0]	Extended Write mode 5, background-color low byte
GR1[7:0]	Extended Write mode 4/5, foreground-color low byte
GR10[7:0]	Extended Write mode 5, background-color high byte
GR11[7:0]	Extended Write mode 4/5, foreground-color high byte

D.4 Extended Write Mode s

The CL-GD7541/GD7543 supports two extended write modes: Extended Write modes 4 and 5. These extended write modes can selectively update up to 8 pixels of 8 or 16 bits each. For more information, refer to Section D.8 and Section D.9.

Extension register GRB, the Graphics Controller Mode Extensions register, bits [4:1] are used in combination to enable the CL-GD7541/GD7543 Extended Write modes.

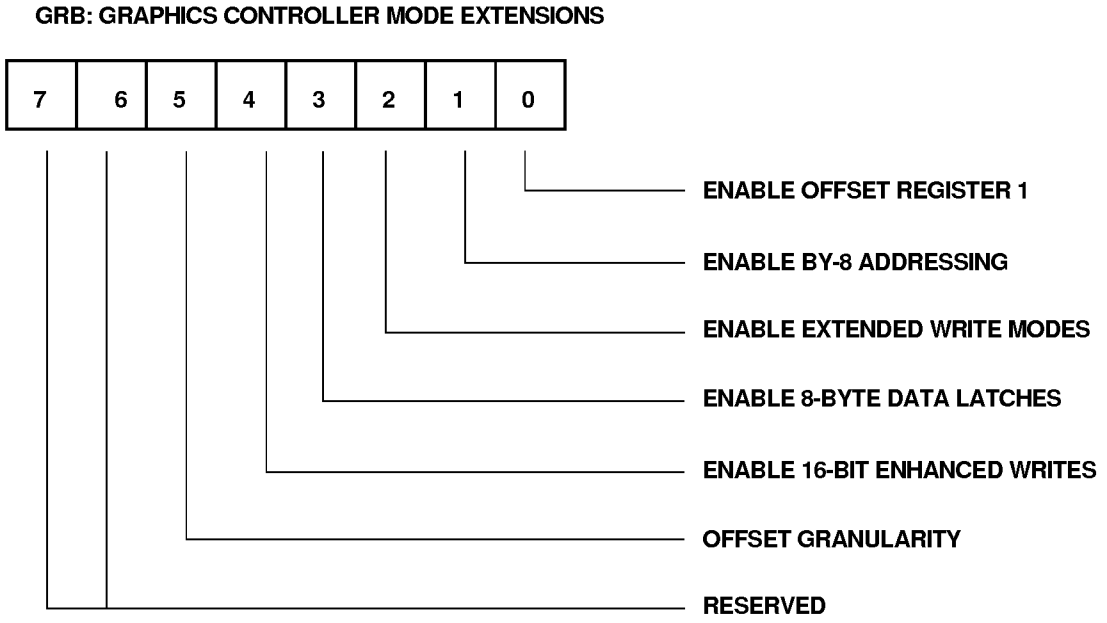


Figure D-1. Extension Register GR B

When Extended Write modes are enabled by setting GRB[2] to '1':

- Up to 8 bytes can be transferred to display memory for every CPU byte transfe r.
- Graphics Controller register GR0[7:0] extends read/write values for Extended Write mode 5, the background color.
- Graphics Controller register GR 1[7:0] extends read/write values for Write mode 4/5, the foreground color.
- Graphics Controller register GR5[2] is enabled to select Extended Write modes 4 and 5 .
- Graphics Controller register GRB[4] is enabled to select enhanced writes for Write modes 4 and 5 .
- Sequencer register SR2[3:0] extends to SR2[7:0] for Write modes 4 and 5.

D.5 By-8 Addressin g

GRB[1], when set to '1', selects By-8 addressing for 8-bit-per-pixel (256-color) graphics modes. The system address is shifted left by 3 bits relative to packed-pixel addressing so that each system byte address points to a different 8-pixel (8 bytes) block in display memory.

This GRB[1] bit, in combination with GRB[2], is used for selecting Extended Write modes. This bit is a 'don't care' when GRB[4] is '1'.

D.6 By-16 Addressin g

GRB[4], in combination with GRB[2], is used to select Write mode 4 and 5 for 16-bits-per-pixel graphics modes (RGB 555 or 565). The system address is shifted left by 4 bits relative to packed-pixel addressing so each system byte address points to a different 8 pixels (16-byte block) in display memory. GRB[4] and GRB[2], when set to '1', select the following Write mode operation:

- Enables By-16 addressing .
- Enables up to 16 bytes (8 pixels) to be transferred for each CPU byte cycle .
- Enables GR10 and GR11 as high-byte data for foreground and background color extensions. (GR0 and GR1 contain the low-byte data.)
- Enables each bit of SR2 to be used as pixel write mask for 2 bytes.

D.7 Data Latche s

When GRB[3] is set to '1', the memory read latches are 8 bytes wide, instead of the normal 4. Eight-byte-wide memory read latches can be used in Write mode 1 to write 8 latched bytes back into display memory. This action allows either 8 pixels in 256-color modes or 4 pixels in 16-bits-per-pixel modes to be updated in a single CPU byte cycle.

D.8 Extended Write Mode 4

The CL-GD7541/GD7543 supports Extended Write mode 4, which is used in combination with By-8 or By-16 addressing modes to operate on 8 pixels of data at a time (8 or 16 bytes, depending on 8- or 16-bit-per-pixel mode).

- In 8-bits-per-pixel mode, the Foreground Color bits GR1[7:0] are used to update each pixel byte in display memory.
  - The 8-bit value is written as the foreground color when the corresponding CPU data is a '1', and the corresponding Map Mask register bit in SR2 is also set to a '1'.
  - When the CPU Data bit is a '0', the corresponding pixel in display memory is not changed by the write.
- In 16-bits-per-pixel mode, the Foreground Color register bits GR11[7:0] (foreground-color high byte) and GR1[7:0] (foreground-color low byte) are used to update each pixel word in display memory .
  - When the corresponding CPU data is '1' and the corresponding Map Mask register bit in SR2 is also '1', the 16-bit value is written as the foreground color.
  - When the CPU Data bit is '0', the corresponding pixel in display memory is not changed by the write.

This mode, for example, can be used to write text to display memory with the foreground color while preserving the background color. This action allows 8 pixels of display data to be updated with a single CPU byte cycle.

D.9 Extended Write Mode 5

The CL-GD7541/GD7543 supports Write mode 5, which is used in combination with By-8 or By-16 addressing mode to operate on 8 pixels of data at a time (8 or 16 bytes, based on 8- or 16-bit-per-pixel mode). This mode can be used to write text to display memory with a selected foreground color and a background color. This action allows 8 pixels of display data to be updated with a single CPU byte cycle.

- In 8-bit-per-pixel mode, the Foreground Color bits GR1[7:0] or the Background Color bits GR0[7:0] are used to update each pixel byte in display memory.
  - When the corresponding CPU data bit is '1', the 8-bit value is written as the foreground color .
  - When the corresponding CPU data bit is '0', the corresponding pixel in display memory is written with the background color.
  - The corresponding Map-Mask register, SR2[7:0], also inhibits writes to selected pixel in display memory .
- In 16-bit-per-pixel mode, the Foreground-Color bits GR11[7:0] (foreground-color high byte) and GR1[7:0] (foreground-color low byte), or the Background Color bits GR10[7:0] (background-color high byte) and GR0[7:0] (background-color low byte), are used to update each pixel word in display memory.
  - When the corresponding CPU data is '1', the 16-bit value is written with the foreground color .
  - When the corresponding CPU data bit is '0', the corresponding pixel in display memory is written with the background color.
  - The corresponding Map-Mask register, SR2[7:0], also inhibits the corresponding pixel value (2 bytes) to be written to display memory .

Appendix E

True-Color Modes

E.1 Introduction

The CL-GD7541/GD7543 has a built-in true-color multi-mode palette DAC that supports the following modes:

- 8 bits per pixel (VGA-standard 256-Color Palette mode)
- 15 bits per pixel (32K color, the 5-5-5 mode)
- 16 bits per pixel (64K color, the 5-6-5 XGA™ mode)
- 24 bits per pixel (16.8-million color, the 8-8-8 True-Color mode)
- Mix mode: Either 15 bits per pixel (5-5-5 mode) or 8 bits per pixel (standard VGA mode)

In the 256-Color Palette mode, the palette DAC is VGA-compatible and provides 256 simultaneous colors from a palette of 256K on the display screen.

E.2 Programming for a True-Color Multi-Mode Palette DAC

Extended Color modes are enabled by the Hidden DAC register (HDR at I/O Port 3C6h). At reset, this register is loaded with 00h, which programs the palette DAC in a VGA-compatible mode. In this mode, the palette DAC is functionally equivalent to the industry-standard Brooktree® BT476 RAMDAC. By writing code to the Hidden DAC register, the palette DAC can be programmed in one of the modes mentioned above. The following method is used to write to the Hidden DAC register.

1. **Read from the Pixel-Mask register (3C6h) four times in succession.**

   No other reads/writes must be directed to that address. After the fourth read, the Pixel-Mask register points to the Hidden DAC register.

2. **Program the Hidden DAC register by writing to it at Port 3C6h.**

   Any read from or write to any address (other than the Pixel-Mask register) resets an internal counter, which 'hides' the Hidden DAC register again. To continue, repeat Step 1.

Table E-1. Extended Color Mode Selected with the Hidden DAC Register

HDR								Function
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	
0	X	X	X	X	X	X	X	Standard VGA-compatible 256-color mode
1	1	1/0	0	0	0	0	0	5-5-5 mode (32K colors)
1	1	1/0	1	0	0	0	0	5-5-5 and 256-Color Mix mode
1	1	X	0	0	0	0	1	5-6-5 mode (64K colors, XGA™)
1	1	X	0	0	1	0	1	8-8-8 mode (16.8-million color, True-Color mode)

NOTE: In 5-5-5 mode, programming HDR[5] to '0' chooses Clocking mode 1 and programming HDR[5] to '1' chooses Clocking mode 2. When using a video overlay feature of the CL-GD7541/GD7543, choose Clocking mode 1.

E.2.1 5-5-5 Mode with 32K Colors

This mode supports the industry-standard 5-5-5 RGB mode with 32,768 colors. Each pixel is represented by 15 bits containing 5 bits of red, green, and blue color information. The input sequence for each pixel is the low byte first, followed by the high byte.

The first low byte is taken on the first rising edge of clock occurring after BLANK# has gone inactive (high).

- In Clocking mode 2 (HDR[5] = '1'), all subsequent bytes are clocked in on the rising edge of the clock.
- In Clocking mode 1 (HDR[5] = '0'), the low bytes are clocked in on the rising edge of the clock and the high bytes are clocked in on the falling edge of the clock .

This mode ignores the palette DAC lookup table.

Table E-2. Pixel Data Format in 5-5-5 Mode

MSB HIGH BYTE								LOW BYTE							LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	4	3	2	1	0	4	3	2	1	0	4	3	2	1	0
X	RED					GREEN					BLUE				

E.2.2 5-6-5 Mode with 64K Colors (XGA™)

This mode supports the XGA™ 5-6-5 RGB mode with 65,536 colors. Each pixel is represented by 16 bits containing 5 bits of red, 6 bits of green, and 5 bits of blue color information. The input sequence for each pixel is the low byte first, followed by the high byte, by using the Clocking mode 1 or 2. The first low byte is taken on the first rising edge of clock occurring after BLANK# has gone inactive (high).

- In Clocking mode 2 (HDR[5] = '1'), all subsequent bytes are clocked in on the rising edge of clock.
- In Clocking mode 1 (HDR[5] = '0'), the low bytes are clocked in on the rising edge of the clock, and the high bytes are clocked in on the falling edge of the clock .

This mode ignores the palette DAC lookup table.

Table E-3. Pixel Data Format in 5-6-5 Mode with 64K Colors

MSB HIGH BYTE								LOW BYTE							LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
4	3	2	1	0	5	4	3	2	1	0	4	3	2	1	0
RED					GREEN						BLUE				

E.2.3 8-8-8 Mode with 16.8 Million Colors (True Color Mode)

This mode supports the industry-standard 8-8-8 RGB mode with 16,777,216 colors. Each pixel is represented by 24 bits containing one byte each of red, green, and blue color information. The input sequence for each pixel is the low byte (blue) first, followed by the middle byte (green), followed by the high byte (red).

This mode uses Clocking mode 2 (HDR[5] = '1'). The first low-byte is taken on the first rising edge of clock occurring, after BLANK# has gone inactive (high). All subsequent bytes are clocked in on the rising edge of clock. This mode ignores the palette DAC lookup table.

Table E-4. Pixel Data Format in 8-8-8 Mode with 16.8 Million Colors

MSB HIGH BYTE								MIDDLE BYTE								LSB LOW BYTE							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
RED								GREEN								BLUE							

E.2.4 Mix Mode

When HDR[4] is set to '1', pixel data bit [15] is used to select between 5-5-5 RGB mode and the standard VGA-compatible, 256-color mode.

Table E-5. Pixel Data Format in 5-5-5 Mode of the Mix Mode

MSB HIGH BYTE								LSB LOW BYTE							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	4	3	2	1	0	4	3	2	1	0	4	3	2	1	0
5-5-5 mode	RED					GREEN					BLUE				

Table E-6. Pixel Data Format in 256-Color Mode of the Mix Mode

MSB HIGH BYTE								LSB LOW BYTE							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	X	X	X	X	X	X	X	7	6	5	4	3	2	1	0
256-Color mode	Ignored							Palette DAC lookup-table input							

Appendix F

Memory Configuration s

F.1 Introductio n

The CL-GD7541/GD7543 supports scalable 32-bit-wide display-memory configurations, from 1 to 2 Mbytes, using the following types of DRAMs.

- 512K × 8
- 256K × 16 — multiple-CAS#
- 256K × 16 — multiple-WE#

F.2 Possible Memory Configuration s

Table F-1 shows the possible memory configurations that the CL-GD7541/GD7543 supports.

For 256K × 16 DRAM configurations, the total display memory can be expanded from 1 to 2 Mbytes. The 512K × 8 DRAM configuration must be 2 Mbytes. Some signals of the CL-GD7541/GD7543 change functions according to the DRAM organization that is used.

For optimum performance, choose multiple-CAS# configurations over multiple-WE# configurations

Table F-1. CL-GD7541/GD754 3 Memory Configuration s

Total Display Memory Size	Memory Bus Width	DRAMs	
		Number	Type
1 Mbyte	32 bits	2	256 Kbytes × 16
2 Mbytes[a]	32 bits	4	512 Kbytes × 8
2 Mbytes[b]	32 bits	4	256 Kbytes × 16

[a] The Extension register SRF[7] = '0'.

[b] The Extension register SRF[7] = '1'.

F.3 Control Signals for Various Memory Configuration s

The following five tables indicate how the CL-GD7541/GD7543 and the DRAMs must be connected.

Table F-2. 2-Mbyte Display Memory: Four 512K × 8 DRAM s

DRAM Pins Connected to CL-GD7541/GD754 3 Pins	CL-GD7541/GD754 3 Pins Connected to the DRA M Pins			
	To DRAM #1	To DRAM #2	To DRAM #3	To DRAM #4
OE#	OE#	OE#	OE#	OE#
WE#	WE#	WE#	WE#	WE#
CAS#	CAS0#	CAS1#	CAS2#	CAS3#
RAS#	RAS0#	RAS0#	RAS0#	RAS0#
ADDR[9:0]	MA[9:0]	MA[9:0]	MA[9:0]	MA[9:0]
DATA	MD[7:0]	MD[15:8]	MD[23:16]	MD[31:24]
Bit planes stored in each DRAM	3	2	1	0

NOTE: This configuration is multiple-CAS#, common-WE# (SRF[0] = '1') .

Table F-3. 1-Mbyte Display Memory: Two 256K × 16 Multipl e-CAS# DRAM s

DRAM Pins Connecte d to CL-GD7541/GD754 3 Pins	CL-GD7541/GD754 3 Pins Connecte d to the DRAM Pin s	
	To DRAM #1	To DRAM #2
LCAS#	CAS2#	CAS0#
UCAS#	CAS3#	CAS1#
OE#	OE#	OE#
RAS#	RAS0#	RAS0#
WE#	WE#	WE#
ADDR[8:0]	MA[8:0]	MA[8:0]
ADDR[9]	Not valid	Not valid
DATA	MD[31:16]	MD[15:0]
Bit planes stored in each DRAM	0,1	2,3

Table F-4. 1-Mbyte Display Memory: Two 256K × 16 Multiple-WE# DRAM s

DRAM Pins Connecte d to CL-GD7541/GD754 3 Pins	CL-GD7541/GD754 3 Pins Connecte d to the DRAM Pin s	
	To DRAM #1	To DRAM #2
LWE#	WE2#	WE0#
UWE#	WE3#	WE1#
OE#	OE#	OE#
RAS#	RAS0#	RAS0#
CAS#	CAS#	CAS#
ADDR[8:0]	MA[8:0]	MA[8:0]
ADDR[9]	Not valid	Not valid
DATA	MD[31:16]	MD[15:0]
Bit planes stored in each DRAM	0,1	2,3

Table F-5. 2-Mbyte Display Memory: Four 256K × 16 Multiple-CAS# DRAM s

DRAM Pins Connecte d to CL-GD7541/GD754 3 Pins	CL-GD7541/GD754 3 Pins Connecte d to the DRAM Pin s			
	To DRAM #1	To DRAM #2	To DRAM #3	To DRAM #4
LCAS	CAS2#	CAS0#	CAS2#	CAS0#
UCAS	CAS3#	CAS1#	CAS3#	CAS1#
OE#	OE#	OE#	OE#	OE#
RAS#	RAS0#	RAS0#	RAS1#	RAS1#
WE#	WE#	WE#	WE#	WE#
ADDR[8:0]	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]
DATA	MD[31:16]	MD[15:0]	MD[31:16]	MD[15:0]
Bit planes stored in each DRAM	0,1	2,3	0,1	2,3

Table F-6. 2-Mbyte Display Memory: Four 256K × 16 Multiple-WE# DRAMs

DRAM Pins Connected to CL-GD7541/GD7543 Pins	CL-GD7541/GD7543 Pins Connected to the DRAM Pins			
	To DRAM #1	To DRAM #2	To DRAM #3	To DRAM #4
LWE#	WE2#	WE0#	WE2#	WE0#
UWE#	WE3#	WE1#	WE3#	WE1#
OE#	OE#	OE#	OE#	OE#
RAS#	RAS0#	RAS0#	RAS1	RAS1
CAS#	CAS#	CAS#	CAS#	CAS#
ADDR[8:0]	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]
DATA	MD[31:16]	MD[15:0]	MD[31:16]	MD[15:0]
Bit planes stored in each DRAM	0,1	2,3	0,1	2,3

Appendix G

Clock Option s

G.1 Introductio n

The dual-frequency synthesizer in theCL-GD7541/GD7543 generates all the clocks needed for the memory timing (for example, RAS#, CAS#), as well as the video clock timing. To derive these internal clock signals, an external reference clock must be provided to the OSC input of theCL-GD7541/GD7543. For all calculations in this document, the external reference clock used is 14.318 MHz± 0.01% with a duty cycle of 50 ± 10%.

G.2 Memory Cloc k

MCLK (the memory clock) is used to generate all of the memory timing signals (for example, RAS# and CAS#).

G.2.1 Default MCLK (Memory Clock)

The CL-GD7541/GD7543 default memory clock frequency is 42.955 MHz. For the equation in the next section, this frequency is equivalent to 18h (24 decimal). Refer to Appendix L for information regarding CL-GD7541/GD7543 configuration.

G.2.2 MCLK Programmin g

For higher performance, the CL-GD7541/GD7543 has a programmable memory clock. The desired MCLK frequency is programmed directly into SR1F[5:0], by using the equation below. The MCLK selected at system reset (19h) is valid until SR1F is written.

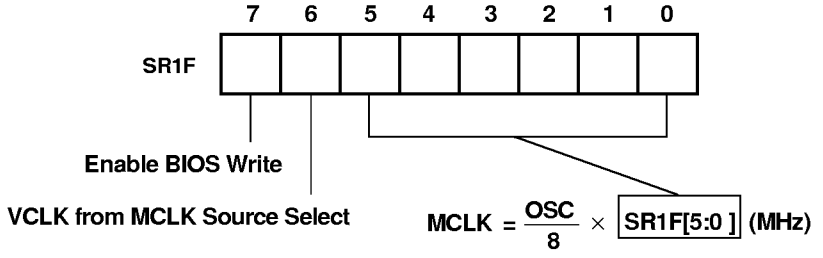


Figure G-1. Programmable Memory Cloc k

Examples of valid MCLK frequencies are shown in Table G-1:

Table G-1. Examples of Valid MCLK Frequencies

SR1F[5:0] (decimal)	SR1F[5:0] (hex)	MCLK Frequency (MHz)
21	15h	37.585
23	17h	41.165
25	19h	44.744
28	1Ch	50.114

G.3 Video Clock

The VCLK (video clock) is the fundamental video timing clock in the system. The CRT monitor timing signals (HSYNC and VSYNC), as well as the LCD clocks, are derived from VCLK

G.3.1 Default Video Clock Source

The VCLK source is determined by a number of factors as indicated in Table G-2. For a default VCLK, either MCLK or MCLK/2 (one-half the frequency of MCLK), as well as four VCLKs, can be used.

Table G-2. VCLK Sources and Frequencies

Extension Register SR1F[6]	Extension Register SR1E[0]	External/General Register MISC 3C2[3:2]	Video Clock (Defaults)	
			Source	Frequency (MHz)
0	X	00	VCLK0	25.180
0	X	01	VCLK1	28.325
0	X	10	VCLK2	41.165
0	X	11	VCLK3	36.082
1	0	XX	MCLK	42.955
1	1	XX	MCLK/2	21.477

G.3.2 VCLK Programmin g

As indicated in Table G-3, the VCLK sources can be programmed with two registers each.

Table G-3. Internal VCLK Source s

Video Clock Source	Default Frequency (MHz)	Numerator			Denominator			Post-scalar
		Extension Register	Decimal	Hex	Extension Register	Decimal	Hex	
VCLK0	25.180	SRB[6:0]	102	66h	SR1B[5:1]	29	3Bh	1
VCLK1	28.325	SRC[6:0]	91	5Bh	SR1C[5:1]	23	2Fh	1
VCLK2	41.165	SRD[6:0]	69	45h	SR1D[5:1]	24	30h	0
VCLK3	36.082	SRE[6:0]	126	7Eh	SR1E[5:1]	25	19h	1

For each VCLK, a 7-bit numerator (N), 5-bit denominator (D), and 1-bit post-scalar (P) determines the frequency according to the equation shown in Figure G-2:

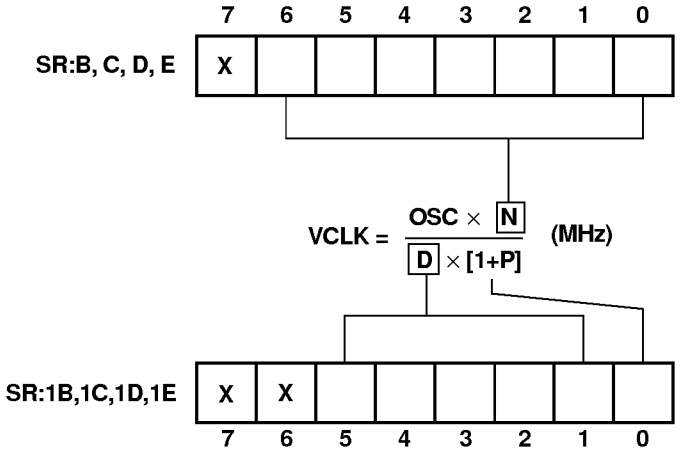


Figure G-2. Programmable Video Cloc k

Typically, a large number of numerator/denominator values can program a common frequency. The choice among these combinations is made empirically. Better results can be obtained if the post-scalar is programmed to '1'.

G.4 Using MCLK as VCLK

When MCLK and VCLK are programmed to frequencies within ≈1% of each other (or to frequencies that are nearly multiples of each other), they can interfere with each other. This interference can show up as 'jitter' on the screen. The solution is to shut down the VCLK oscillator and use MCLK (or MCLK/2) as VCLK. Table G-4 shows examples of frequencies for which this solution must be used.

Table G-4. Memory Clock Used as Video Clock

MCLK	graphics mode	VCLK		Selection Criteria		
		Frequency	Source	SR1F[5:0]	SR1F[6]	SR1E[0]
50.1	64h at 60 Hz	25 MHz	MCLK/2	1Ch	1	1
50.1	66h at 60 Hz	25 MHz	MCLK/2	1Ch	1	1
50.1	58h at 72 Hz	50 MHz	MCLK	1Ch	1	0
50.1	5Ch at 72 Hz	50 MHz	MCLK	1Ch	1	0

Appendix H

Power Management

H.1 Introduction

The CL-GD7541/GD7543 has two LCD power-management modes, Standby and Suspend. The CL-GD7541/GD7543 also manages CRT power consumption through DPMS (display power management signaling) support.

H.2 Power Management

The CL-GD7541/GD7543 provides several intelligent power-management features to enable the power-saving modes. For power-management BIOS calls discussed in this section, refer to the Cirrus Logic "CL-GD754X VGA BIOS External Function Specification" in the *CL-GD754X Application Book*. Table H-1 lists dedicated CL-GD7541/GD7543 pins that facilitate power management.

Table H-1. Dedicated Pins for Power Management

Pin Name (Pin Function)	Pin No.	Pin Type	Pin Function Description	Pin Use
ACTI / FCEVIDEO# / SBYI	86		Activity sense / Feature-Connector enable video# / Standby mode input functions. This pin may be used for one of three functions, depending on the configuration of Extension registers SR23[6] and SR24[7]. Two of the functions are related to power management:	
(ACTI)		I	(1) Activity sense function. When this pin is configured for the activity sense function and the ACTI input pin is connected to another input pin, this pin can be used to sense various types of activity in order to initiate an action. A keyboard interrupt, for example, can be used to reset whatever internal timers have been set.	To use the ACTI function, set Extension register bits SR24[7] = '1' and SR23[6] = '1'. Then, to use any low-to-high activity on the ACTI pin : (1) To reset the internal Standby mode timer, set Extension register bits SR23[6] to '1' and CR2D[6] to '1'. (2) To reset the backlight control for the LCD, set Extension register bits SR23[6] to '1' and CR2D[3] to '1'.
(FCEVIDEO#)		I	(2) FCEVIDEO# function. When this pin is configured for the FCEVIDEO# function, this pin is not utilized for power management. In this case, the Standby mode must be initiated by software methods.	To use the FCEVIDEO# function, set Extension register SR24[7] = '0'.
(SBYI)		I	(3) Standby mode function. To configure this pin to initiate the Standby mode function, set Extension register bits SR24[7] = '1' and SR23[6] = '0'. (There are also two software-based methods of entering the Standby timer mode. For details, refer to Chapter 3.)	To use this pin to enter Standby mode, set Extension register SR23[6] to '0'. If this pin is not used, connect it to ground. When the LCD is on and this input is asserted high, the power-down sequence starts for the Standby mode. Standby mode terminates when this pin goes low (as long as Extension register CR20[4] = '0') and the Standby timer has been reset.

Table H-1. Dedicated Pins for Power Management *(cont.)*

Pin Name (Pin Function)	Pin No.	Pin Type	Pin Function Description	Pin Use
BLI / SUSPI	87		Backlight input / Suspend mode control functions. This pin may be used in one of two ways for power management functions.	
(BLI)		I	(1) LCD backlight input control function. When this pin is configured for the LCD backlight input control function, it turns off the LCD backlight. This function would be used for conditions under which the LCD is off, but CPU accesses are allowed and CRT outputs remain active.	To use the pin to turn off the LCD backlight : (1) Connect the pin to an external source . (2) Set Extension register SR23[5] to '1', in which case a high on this input turns the LCD backlight off.
(SUSPI)		I	(2) Suspend mode control function. When this pin in configured to initiate the hardware-controlled Suspend mode, the CL-GD7541/GD7543 bus is disabled. Consequently, attempts by the CPU to access the CL-GD7541/GD7543 are ignored. In local bus applications, the bus controller must intercept CPU access attempts when the CL-GD7541/GD7543 is in hardware-controlled Suspended mode, or else the local bus hangs. This mode is the most efficient power-saving mode. (The Suspend mode can also be initiated with software commands. For details, refer to Chapter 3.)	To use the pin for hardware-controlled Suspend : (1) Connect the pin to an external source . (2) Set Extension register SR23[5] = '0' to define this pin to function as the hardware-controlled Suspend mode input. (3) Disable software-controlled Suspend mode by setting Extension register CR20[3] to '0' . (4) Set the resolution of the debounce timer: CR20[7] = '1' sets a resolution of 1 sec. CR20[7] = '0' sets a resolution of 32 msec . (5) Initialize the debounce timer by setting Extension register CR23[7:4] to any non-zero value. (6) A stable high signal on this input initiates the hardware-controlled Suspend sequence .
CLK32K	7	I	32-KHz clock input function . This pin is used to provide memory refresh during Suspend mode. **NOTE :** This clock must be present and stable before the CL-GD7541/GD7543 is placed into Suspend mode.	When Extension register CR2D[4] = '0' and the CL-GD7541/GD7543 is in Suspend mode : (1) The OSC input pin is disabled . (2) A 32-kHz clock must be connected to the CLK32K pin. (The 32-kHz clock source for memory refresh in Suspend mode is derived from the CLK32K pin.) (3) To select an external 32-kHz clock for the pin, set Extension register CR29[6] to '1' .

Table H-1. Dedicated Pins for Power Management *(cont.)*

Pin Name (Pin Function)	Pin No.	Pin Type	Pin Function Description	Pin Use
FPBL	105	O	Flat panel backlight power function. This pin can function in three ways: (1) Normal flat panel power sequence functions, including Standby and Suspend modes. (2) For internal backlight timer functions. (3) With a software override bit for various control functions.	(1) This pin is sequenced high or low automatically by the CL-GD7541/GD7543 in three ways: (a) As part of normal power-up/down sequence (b) When switching between a CRT and LCD (c) Entering Suspend/Resume or Standby modes (2) To use this pin with an internal backlight timer: (a) To configure the pin for internal backlight functions, connect the FPBL pin to the input of the LCD backlight control circuit. (b) To use the backlight timer, program Extension register CR21[7:4] for a time-out delay. (c) To reset the backlight timer, use one or more of the following methods: [1] To use any low-to-high activity on the ACTI timer pin to reset the backlight timer, set Extension register CR2D[3] to '1'. [2] To use keyboard activity to reset the backlight timer, set Extension register SR25[0] to '1'. [3] To use any VGA access (memory or I/O) to reset the backlight timer, set Extension register CR2D[2] to '1'. (3) To override power-up/down sequencing and other control functions, set Extension register CR23[3] to '1' and toggle CR23[2] to turn the LCD backlight output on and off. CAUTION: This action is not recommended, as flat panel damage may result.

Table H-1. Dedicated Pins for Power Management *(cont.)*

Pin Name (Pin Function)	Pin No.	Pin Type	Pin Function Description	Pin Use
FPVCC	106	O	Flat panel VCC. This pin is part of the flat panel power sequencing, which includes Standby and Suspend modes. This pin can be controlled with a software override bit.	(1) Connect the pin to the flat panel VCC control circuit. (2) This pin is sequenced high or low automatically by the CL-GD7541/GD7543 in three ways: (a) As part of normal power-up/down sequence (b) When switching between a CRT and LC D (c) Entering Suspend/Resume or Standby modes (3) To override all controls, set Extension register CR23[1] to '1', and toggle CR23[0] to turn FPVCC on or off. **CAUTION:** **This action is *not* recommended, as flat panel damage may result.**
FPVEE	102	O	Flat panel VEE. This pin is part of the flat panel power sequencing, which includes Standby and Suspend modes.	(1) Connect the pin to the flat panel VEE (contrast) control circuitry. (2) This pin is sequenced high or low automatically by the CL-GD7541/GD7543 in three ways: (a) As part of normal power-up/down sequence (b) When switching between a CRT and LC D (c) Entering Suspend/Resume or Standby modes
PROG	148	O	Programmable output function. If a system uses a programmable VDD circuit, this pin must be used by the video BIOS and the circuit to select 3.3-V or 5.0-V core VDD operation. **NOTE:** The programmable VDD circuit is described in the Cirrus Logic application note, "Programmable Core Voltage", in the *CL-GD754X Application Book*.	If Extension register CR30[7]: (1) Is '1', PROG is set high, and the programmable VDD circuit switches the core VDD to 5.0 V. (2) Is '0', PROG is set low, and the programmable VDD circuit switches the core VDD to 3.3 V.

Table H-1. Dedicated Pins for Power Management *(cont.)*

Pin Name (Pin Function)	Pin No.	Pin Type	Pin Function Description	Pin Use
SBYST#	123	O	Standby mode status function. This pin can be configured to perform one of three possible functions: (1) For a power-management function, this pin can be used to indicate the status of Standby mode. (2) For a Feature Connector data function, this pin can be used for pixel data output. (3) For a 24-TFT LCD function, this pin can be used for the 24-bit TFT Green bit [0] LCD data output (that is, FP8).	 (1) If Extension register CR29[4] = '1', then SBYST# remains low, indicating that the CL-GD7541/GD7543 is in Standby mode. (2) If pin 157 (MD [25] / FCPU) is configured for the Feature Connector function and Extension register SR24[7] = '1', this pin functions as FC pixel data output and is not used for power management. (3) If a 24-bit TFT LCD is connected, this pin is used for LCD data output, and the Standby Status function is not available.
SUSPST#	125	O	Suspend mode status. This pin can be configured to perform one of three possible functions. (1) For a power management function, this pin can be used to indicate the status of Suspend mode. (2) For a Feature Connector data function, this pin can be used for pixel data output (FCP1). (3) For a 24-TFT LCD function, this pin can be used for the 24-bit TFT Green bit [1] LCD data output (that is, FP9).	 (1) If Extension register CR29[7:6] = '1', then SUSPST# remains low, indicating that the CL-GD7541/GD7543 is in Suspend mode. (2) If pin 157 (MD [25] / FCPU) is configured for the Feature Connector function and Extension register SR24[7] = '1', this pin functions as FC pixel data output and is not used for power management. (3) If a 24-bit TFT LCD is connected, this pin is used for LCD data output, and the Suspend Status function is not available.

H.2.1 Normal Power Mode

In normal power mode, either the LCD system, the CRT monitor, or both are being used. During normal power mode, the following occurs:

- The active display(s) receive power.
- Full-screen refresh is in effect.
- The CPU has access to the following:
  - Video memory
  - RAMDAC
  - I/O registers
- Refresh is provided to video memory.

H.2.2 Standby Mode

When the system is not being actively used, the CL-GD7541/GD7543 can be set up to automatically enter Standby mode. During Standby mode, the screen goes blank, but application programs the user may have launched continue to run normally. The device can be set up so the user can terminate Standby mode (by pressing a key, for example) and restore the screen.

When the system enters Standby mode, the LCD is turned off using the power-down sequence. As a result, since there is no screen refresh, normal clock rates may be replaced by slower clock rates, further reducing power consumption. When the system is in Standby mode, the following occur.

- The LCD power-up/down sequence occurs automatically when Standby mode is entered or exited.
- The VCLK oscillator is stopped.
- No clock is provided to the CRT controller.
- The RAMDAC is in the low power mode.
- Video display memory refresh occurs (at a slower refresh rate).
- The CPU accesses and modifies the video display memory and palette DAC.

H.2.2.1 Standby Mode: Initiating and Entering

The CL-GD7541/GD7543 provides three methods for entering Standby mode. The transition can be initiated in software by using a hardware timer, or by using the Standby input pin (SBYI).

All methods for entering the Standby mode offer the features itemized above. One or more methods can be used simultaneously to start and/or maintain Standby mode. Standby mode is entered as follows:

1) To use software to start the Standby mode power-down sequence, set Extension register CR20[4] to '1'.
2) To use a hardware and software combination to start the Standby mode, use either of the following methods:
   a) Program the hardware timer in Extension register CR21[3:0] in increments of one minute, up to 15 minutes. If the hardware timer is allowed to count down to zero, the Standby mode power-down sequence is started.
   b) Program Extension register SR24[7] to '0' so that the Standby mode can be entered through hardware control. To select the Standby input function, connect the SBYI pin to an external source and set SR23[6] to '0'. When the SBYI pin is driven high, the Standby mode power-down sequence is started.

The above conditions must be removed to terminate Standby mode and start the power-up sequence.

H.2.2.2 Standby Mode: Status

The status of Standby mode can be obtained by checking the state of the SBYST# pin. If the CL-GD7541/GD7543 is in Standby mode, Standby mode status (CR29[4]) is set high from the time the clocks are stopped until 32 µsec after the clocks are restarted. SBYST# output is low during this time.

Pin 123 is a multi-function pin that cannot be used as SBYST# if the following conditions exist:

1) An external pull-up resistor is connected to pin 157, which configures the chip for Feature Connector functionality. (Pin 123 is then used for pixel data output.)
2) A 24-bit TFT LCD is connected. (Pin 123 is then used for TFT green data output.)

H.2.2.3 Standby Mode: Terminating and Exiting

The LCD power-up sequence occurs automatically when Standby mode is terminated. This sequence occurs when all of the methods initiating it are removed.

1) Reset the Standby-mode timer in one of the following ways:
   — To use activity on the ACTI input to reset the timer, set CR2D[6] to '1'. Since the ACTI pin is multifunctional, enable the ACTI input function by setting SR23[6] to '1'. (SR24[7] must be reset to '0' to enable ACTI.)
   — To use any VGA access (memory or I/O) to reset the timer, set CR2D[5] to '1'.
   — To use any keyboard access to reset the timer, set SR25[1] to '1'.
2) Terminate software-controlled Standby mode by setting CR20[4] to '0'.
3) Terminate hardware-controlled Standby mode by asserting the SBYI pin low.

If a power-up or power-down sequence is in progress when there is a request to terminate or initiate Standby mode, the power-up/down sequence is allowed to complete before the new request is initiated.

H.2.3 Suspend Mode

The CL-GD7541/GD7543 Suspend mode is used to save power when the system is not being actively used for a long period of time.

When the system enters Suspend mode, the following occur:

- The screens turn off.
- Application programs suspend operation.
- The CPU is prohibited from accessing video memory, I/O registers, or the palette DAC, in the case of hardware-controlled Suspend. In hardware-controlled Suspend mode, even though application programs cease to run in either foreground or background, all register states are preserved, and so the environment is maintained when Suspend mode terminates.

H.2.3.1 Suspend Mode: Hardware-Controlled

Hardware-controlled Suspend mode provides the most efficient means of power saving. Hardware-controlled Suspend mode is initiated by using the SUSPI pin. SR23[5] must be set to '0' to enable hardware-controlled Suspend mode. This pin uses a debounce timer to minimize accidental attempts to initiate Suspend mode.

In this mode, the input pads are shut off and the bus interface does not receive power. All I/O pins, except the dedicated Suspend mode input are de-activated, further reducing power consumption. Additional power is saved because CPU host access to video memory is denied. Also, if selected, a slower 32-kHz clock refreshes the video memory by performing CAS#-before-RAS# refresh. This slow clock input, which is recommended for maximum power savings, comes from one of two sources:

- By setting CR2D[4] to '1', a 32-kHz clock output results from dividing the 14.318-MHz clock by 432.
- By setting CR2D[4] to '0', an external 32-kHz clock input can be provided through the 32-kHz input. The 14.318-MHz input can then be removed to save power.

When the system is in hardware-controlled Suspend mode, the following occur:

- The LCD power-down/up sequence occurs automatically when Suspend mode is entered or exited.
- The VCLK and MCLK oscillators automatically shut off when the Suspend sequence occurs.
- No CPU access is allowed to the following:
  - Video memory
  - RAMDAC
  - I/O registers
- Although video display memory cannot by accessed by the CPU during Suspend mode, the contents are preserved. (This action is useful when a system remains inactive for a relatively long time.)
- Register data contents are retained.
- Unless DRAMs are self-refresh, the CL-GD7541/GD7543 internal refresh clock for video memory is set to 32 kHz.

When using self-refresh DRAMs, Refresh Select (CR20[2:1]) must both be set to '1' so that static delays within the chip generate the necessary timings to initiate self-refresh.

H.2.3.2 Suspend Mode: Software-Controlled

Software-controlled Suspend mode is initiated by setting CR20[3] (Activate Suspend mode) to '1'. In contrast to the hardware-controlled Suspend mode, software-controlled Suspend mode allows the CPU to access all the internal registers, which requires an active clock and I/O capability, and therefore more power.

H.2.3.3 Suspend Mode: Initiating and Entering

Hardware-controlled Suspend mode is recommended, in order to minimize power consumption. Hardware-controlled Suspend mode is entered by connecting the SUSPI pin to an external source. When input to SUSPI is high, the Suspend mode is initiated. An internal debounce timer (Extension register CR23[7:4]) selects the time period that an input must remain high and stable before the Suspend mode is activated. Debounce Timer Resolution (in Extension register CR20[7]) determines the resolution of the timer (between 32 µsec and 1 sec).

NOTE: SUSPI / BLI Select (SR23[5]), and Activate Suspend Mode (CR20[3]) must be set to '0' to define the BLI / SUSPI pin function as hardware-controlled Suspend mode.

Software-controlled Suspend mode is entered by setting CR20[3] to '1'. In this mode, CPU access is still active, and the SUSPI pin is disabled.

NOTE: This mode is not recommended, as it requires more power than the hardware-controlled Suspend mode.

H.2.3.4 Suspend Mode: Sequence

The typical Suspend mode sequence is as follows:

1) The system receives a request to suspend.

2) The system interrupts the application. The interrupt routine calls the video BIOS Suspend routine. The video BIOS Suspend routine waits until all CPU cycles already in the CPU write buffer are executed.

A CPU read verifies that the CPU write buffer is empty. When the CPU read is done, the CPU write buffer is empty. If a BitBLT operation is in progress, it suspends automatically at the first memory refresh cycle. After resuming, the BitBLT operation continues from the point of operation that it was suspended.

The Suspend mode can be initiated while the CPU write FIFO contains CPU write cycles waiting to be executed. However, the Suspend mode must not be initiated while the RDY# signal is high and waiting for the completion of a cycle. To prohibit this action from occurring, the Suspend routine executes and then waits for the completion of a CPU read, but only if there are no BitBLT operations in progress. If a BitBLT operation is in progress, the Suspend routine skips to the next step in the Suspend sequence without waiting for the RDY# pin to tristate.

Prior to proceeding with the Suspend mode sequence, the BIOS can execute several I/O reads and writes: If the core VDD (CVDD) was at 5.0 V, CVDD must be switched to 3.3 V as the last I/O executed before proceeding to the next step.

3) Set the SUSPI pin high. Using OEMSI (the OEM BIOS customizing utility provided by Cirrus Logic in the BIOS Development kit), the video BIOS must be customized for the I/O location of the SUSPI pin control. [Note that the SUSPI pin is to be controlled by a spare I/O port (a 1-bit output port) on the motherboard.]

4) SUSPST# output is set low.

5) At the end of the first memory refresh cycles (1, 3, or 5 CAS#-before-RAS# refreshes):

a) The display memory control is switched to 32-kHz refresh cycles. No other types of memory cycles can execute.

b) Pad control is forced to Suspend mode and CPU inputs are disabled.

6) The CL-GD7541/GD7543 executes LCD power-off sequencing. The sequence starts 60 µsec after the SUSPI pin is set high and requires approximately 150 msec to complete.

7) The CL-GD7541/GD7543 stops VCLK and MCLK.

8) The 32-kHz clock can now be stopped and the system can be powered down.

H.2.3.5 Suspend Mode: Status

Suspend mode status can be obtained by checking SUSPST#. If the CL-GD7541/GD7543 is in Suspend mode, Suspend Mode Status (CR29[7:6]) is set high from the time the clocks are stopped until 32 µsec after the clocks are restarted. SUSPST# output is low during this time.

SUSPST#, a multifunction pin, cannot be used for SUSPST# if any of the following conditions exist:

1) An external pull-up resistor is connected to pin 157, which enables FC functionality. (Pin 125 is then used for Feature Connector pixel data output).

2) FC Video Port Enable (SR24[7]) is set high, which enables FC functionality. (Pin 125 is then used for pixel data output.)

3) A 24-bit TFT LCD is connected. (Pin 125 is then used for TFT LCD data G[1].)

H.2.3.6 Suspend Mode: Terminating and Exiting

The Suspend mode must be terminated/exited in the same manner that it was entered.

- When SUSPI is driven low, Suspend mode is terminated.
- In software, Suspend mode is terminated by setting CR20[3] to '0'.

When Suspend mode is terminated, the system returns to the same operational state it was in before Suspend mode was entered. The typical Resume sequence is as follows:

1) The system starts the 32-kHz clock.

2) The Resume Video BIOS call is executed, which sets SUSPI low. SUSPST# remains low.

3) The clock synthesizers start after 60 µsec. To ensure a stable signal before the next step in the sequence is executed, allow 64 msec to elapse.

4) The CPU pins are returned to their operational state after the last slow-refresh cycle is done or after the self-refresh end sequence is completed. Memory control is then passed onto the memory clock. Using the memory clock is the standard method for driving the display memory.

5) After 64 msec, the LCD VDD is on and all I/O registers are restored.

6) The LCD pads are enabled after another 32 msec.

7) After another 32 msec, the LCD backlight and bias are enabled and the system is fully resumed.

H.2.4 CRT-Only Power Mode

During the CRT-only operation, LCD drive signals are all inactive, and the LCD power-off sequence occurs automatically.

H.2.5 Backlight Input Control

The LCD backlight can be turned off through input from an external source. BLI input can be used in situations where reduction of LCD power consumption is necessary, but CPU access is still allowed and CRT outputs remain active. A specific example of this situation is a closed-cover condition where the backlight is not necessary, but CPU access is desired to complete an application task or active CRT outputs are desired to allow an external CRT to run.

To enable the BLI function on pin 87, set SUSP/BLI Select (SR23[5]) to '1'. When this input goes high, the LCD backlight is turned off.

H.2.6 Backlight Timer Power Mode

An additional internal timer allows the CL-GD7541/GD7543 to control the backlight without having to enter a power-down mode. The Backlight timer, CR21[7:4], can be programmed in increments of one minute, up to 15 minutes. If the timer is allowed to count down to zero, the FPBL output goes low to disable the LCD backlight. Programming this register to '0' disables the Backlight timer. This timer can be programmed to be reset by activity on the ACTI input pin, by keyboard input, or by a VGA access

H.2.7 ACTI Function

If the ACTI input is enabled, a low-to-high transition on this pin can be used to reset the internal timers for Standby mode, the backlight, or both. If Extension register SR23[6] is set to '1', it enables the ACTI function on pin 86 and Extension register CR2D[6,3] to control which timers are reset by activity on this pin. For example, this pin can be connected to the keyboard interrupt from the system logic to periodically reset the timer(s).

H.3 Techniques for Reducing Power Consumption

H.3.1 Power Reduction in Suspend Mode

In a CMOS device such as the CL-GD7541/GD7543, power is consumed whenever inputs cross CMOS thresholds. Since the CPU address/data buses are inputs to the CL-GD7541/GD7543, the following alternatives are available to reduce power when the system is in Suspend mode.

- When using the hardware-controlled Suspend mode, set registers SR23[5] = '0' and CR20[3] = '0' to isolate the CL-GD7541/GD7543 from the CPU address/data buses. In this case, the SUSPI pin disables CPU access to the CL-GD7541/GD7543.
- Hold the buses quiescent (program them either a '0' or '1') so that inputs do not cross CMOS thresholds and power is not consumed.
- If the CPU processor allows, shut down the CPU I/O ports and stop the CPU clock connected to the LCLK pin of the CL-GD7541/GD7543.
- A 32-kHz oscillator input must be used and the 14.318-MHz clock must be turned off.

To reduce the power used by the memory interface, use low-power CMOS DRAM(s). When not being accessed, CMOS DRAMs do not draw significant current and are effectively powered-down. Self-refresh DRAMs may be used to further reduce power consumption.

H.3.2 Mode-Dependent Voltage Switching

To minimize operating power consumption but still allow use of specific modes (such as 24-bit color mode) that require 5.0-V operation from the VGA core, the CL-GD7541/GD7543 can utilize an external circuit to allow core voltage switching driven by the graphics desired. Active power consumption is minimized because the graphic subsystem can be set to operate at 3.3 V. A 5.0-V operation would occur only in specific modes. Also, even though the core may be switched to 5.0 V, the DRAM, the CPU host bus interface, and LCD VDD can still be set for 3.3-V operation to further minimize active power.

The video BIOS supports INT 10h and 15h function calls that define the minimum voltage requirements for modes to operate, allowing the system to determine if the set mode must be completed. If the CL-GD7541/GD7543 is running at 3.3 V and requests a mode that requires 5.0 V, an INT 15h function call notifies the system BIOS of the voltage requirement.

If the voltage switching circuit is present, the system allows the set mode to proceed by returning an INT 10h call to the video BIOS. The video BIOS sets CR30[7] to '1'. This action sets the PROG pin output high, signaling the external circuit to supply 5.0 V to the core VDD and allowing the set mode call to be completed.

When the CL-GD7541/GD7543 is switched back to a mode that requires only 3.3-V Core operation, a similar set of INT 15h and INT 10h calls allow CR30[7] to be reset to '0'. This action sets PROG low and signals the circuit to supply 3.3 V to the core VDD.

The external circuit and the BIOS function calls supporting this capability are described in more detail in the Cirrus Logic application notes, "A Programmable Core-Voltage Solution", and "CL-GD754X VGA BIOS External Function Specification", in the *CL-GD754X Application Book*.

H.3.3 Complete Power-Down of the Graphics Controller

The CL-GD7541/GD7543 can support system implementations where the VGA subsystem is powered off, providing maximum power savings. The critical task for the CL-GD7541/GD7543 is to properly execute LCD power-down sequencing before shutting off power. Software tasks are the most critical because the VGA controller register states and the contents of video memory must be saved to a system-specified location and then properly restored upon power-up to the graphics subsystem.

The CL-GD7541/GD7543 BIOS has Save/Restore functions for the VGA and Extension register contents. Cirrus Logic also has sample code available of programs that save the contents of video memory. Both are necessary to support this function. Cirrus Logic can provide source code demonstrating Save/Restore functionality for both display memory and registers, allowing the system designer to ensure proper operation of this implementation.

H.4 Green Computing

The CL-GD7541/GD7543 features comprehensive PC power-management functions that support compliance with the United States Environmental Protection Agency's Energy Star Computer Program.

H.4.1 Display Power Management Signaling (DPMS)

The method by which the greatest power savings can be obtained by putting the monitor into a low-power mode that require the monitor respond to DPMS (display power management signaling).

The VESA (Video Electronics Standards Association) DPMS Proposal defines four levels of display power. Through register control, the CL-GD7541/GD7543 can support each of these four levels. The DPMS modes in the CL-GD7541/GD7543 can operate independently of the power modes that the CL-GD7541/GD7543 supports. The only time the CL-GD7541/GD7543 power management mode is directly tied to the DPMS register setting is in timer-initiated Standby because this mode is a hardware timer-driven mode and there is no opportunity for the BIOS to program any of the CL-GD7541/GD7543 registers. Under this condition, the CRT is internally forced by the controller into the DPMS Standby state (VSYNC is automatically provided with a 32-kHz clock) and it disregards any value in GRE[2:1].

Table H-2 shows DPMS register values (GRE[2:1]) in the CL-GD7541/GD7543, the resultant DPMS states, and the DPMS mode relationship to the power management modes.

Table H-2. CL-GD7541/GD7543 DPMS Register Programming

GRE [2:1] Setting	DPMS State	DPMS Compliance	Conditions				CL-GD7541/GD7543 Power Modes
			VSYNC	HSYNC	DAC Power	CRT Recovery	
00	ON = Full operation	Mandatory	Active	Active	On	N/A	Active
01	STANDBY= Operating state of minimal power reduction	Optional	Active	Inactive	Off	Short	Active, Standby, or Suspend
10	SUSPEND= Significant reduction of power consumption	Mandatory	Inactive	Active	Off	Long	Active, Standby, or Suspend
11	OFF= Lowest level of power consumption	Mandatory	Inactive	Inactive	Off	System-dependent	Active, Standby, or Suspend

H.4.2 Static HSYNC and VSYNC

HSYNC is static if GRE[1] is programmed to a '1', and the sense is as programmed into MISC[6]. VSYNC is static if GRE[2] is programmed to a '1', and the sense is as programmed into MISC[7].

If either GRE[1] or GRE[2] is programmed to a '1', the DAC is powered down. This action satisfies the requirement in the VESA proposal which states, "...host system sets the video image information to the blank level prior to the host transmitting the Stand-by/Suspend/Off signal to the display". This action significantly reduces the power in the CL-GD7541/GD7543.

H.4.3 Optimizing Use of DPMS and Controller Power Management Modes

When the CL-GD7541/GD7543 is in CRT-only mode and the CRT is in DPMS Standby or Suspend mode, power consumption can be minimized by having the BIOS reduce the video clock and the memory clock frequencies. Similarly, to ensure there is no power to the CRT, the BIOSmust set DPMS to 'Off' when the CL-GD7541/GD7543 is in LCD-only mode.

Prior to initiating the CL-GD7541/GD7543 Suspend mode, the BIOS can program GRE[2:1] to any of the DPMS power save states (Standby, Suspend, or Off). The 32-kHz input that the CL-GD7541/GD7543 uses for display memory refresh while in the Suspend mode can also be used as the synchronization pulse required if DPMS Standby or Suspend mode is requested. This action allows a system designer the flexibility to select the CRT recovery time desired when resuming from the CL-GD7541/GD7543 Suspend state. Even in the case of hardware-initiated Suspend mode, it is assumed that some time period is allocated for system housekeeping before Suspend mode is actually initiated, which allows DPMS programming to occur.

H.5 VESA® VBE/PM BIOS Function s

The CL-GD7541/GD7543 is fully compliant with the VESA display power management BIOS extensions, VBE/PM Version 1.0. The following sections describe these calls.

H.5.1 Report VBE/PM Capabilitie s

Input:	AH = 4fh		VESA Extension
	AL = 10h		VBE/PM Services
	BL = 00h		Report VBE/PM Capabilities
	ES:DI		Null pointer, must be 0000:0000h
			Reserved for future use
Output:	AX =		Status
	BH =		Power-saving state signals supported by the controller (Note 1)
			1 = supported, '0' = not supported
		00h	On
		01h	Standby
		02h	Suspend
		04h	Off
		08h	Reduced on (intended for LCD displays)

NOTES:

1) The attached display may not support all power states that can be signaled by the controller. It is the respons i-bility of the power-management program to determine the power-saving states that are offered by the controller. If the controller has a means of determining which power-saving state is implemented in the attached display device, this function reports the power saving states that are supported by both the controller and the display .

2) \REDUCED ON is not defined in VBE/PM Version 1.0 and is not implemented .

H.5.2 Set Display Power Stat e

Input:	AH = 4Fh		VESA Extension
	AL = 10h		VBE/PM Services
	BL = 01h		Set Display Power State
	BH =		Requested Power state
		00h	On
		01h	Standby
		02h	Suspend
		04h	Off
		08h	Reduced on (intended for LCDs)
Output:	AX =		Status: If the requested state is not available, this function returns AX = 014Fh, indicating that the function is supported, but that the call failed. In this case, the BH register and Display Power State are left unchanged.
	BH =		Unchanged

H.5.3 Get Display Power State

Input: AH = 4Fh VESA Extension
AL = 10h VBE/PM Services
BL = 02h Get Display Power State

Output: AX = Status: If this function is not supported by the controller hardware, AX = 014Fh must be returned in the status.
BH = Power state currently requested by the controller
00h On
01h Standby
02h Suspend
04h Off
08h Reduced on (intended for LCDs)

Appendix I

Signature Generator

I.1 Introduction

To automatically test the CL-GD7541/GD7543 video-output logic at full speed, the CL-GD7541/GD7543 has SG (signature generator) logic. With the addition of this feature, it is possible to capture a unique 16-bit signature for any given setup of graphics mode and display memory data. An error in the display memory interface, control logic, or pixel-data manipulation produces a different signature that can be compared to a known good signature value obtained from the same image. This comparison allows a test technician to quickly and accurately test a video screen without having to visually inspect the screen for errors. This method is used extensively in the Manufacturing Test.

I.2 Signature Generator Test

To run the SG, bits must be written in the Extension register SR18 to initialize and arm the SG. A status bit reflects that the SG is running. When the Status bit changes state to 'not running', the signature may be read from Extension registers SR19 and SR1A.

Note that the signature is a function of the displayed pixels, not the display data. If the display screen includes blinking attributes or a blinking cursor, then the signature is different for those frames in which the pixel is blinked off, compared to frames in which the pixel is blinked on.

I.3 Signature Generator Register Definition

The SG register definitions are as follows:

Extension register SR18: Signature Generator Control

SR18[7]	LCD Signature Generator Enable '1' = Enable LCD signature generator '0' = Disable LCD signature generator
SR18[6:5]	Reserved
SR18[4:2]	Pixel Data Select These bits select one of the eight Pixel Data bits to use as SG input: '111' = P(7), 110 = P(6)... '000' = P(0).
SR18[1]	Reset Signature Generator '1' = Reset the signature generator '0' = Allow the signature generator to operate under control of SR18[0]
SR18[0]	Signature Generator Enable/Status '1' = Start generating signature on next VSYNC (write) '0' = Signature generator finished running; signature data ready (read)

NOTE: SR18[0] must be '1' to start the SG and is cleared when the SG is done.

The signature generator low- and high-byte results are read from Extension registers SR19 and SR1A, respectively.

- SR19: Signature Generator Result — low by te. SR19[7:0] is the low byte of the 16-bit result from one video frame of signature dat a.
- SR1A: Signature Generator Result — high by te. SR1A[7:0] is the high byte of the 16-bit result from one video frame of signature dat a.

I.4 Sample Code of Signature Generato r

The following 'C' code example describes how a programmer captures eight signatures for any given screen. It is assumed that the screen is already being displayed and no blinking attributes (in text modes) are being displayed.

```
signature_capture () /*Capture eight signatures for any given mode*/
   {
   unsigned int result,i,SR19,SR1A;
   unsigned int SIG [8];
   union REGS in;

   in.x.ax = 0x0100;   /* shut off the cursor, if in text mode */
   in.x.cx = 0x2000;
   int86x (0x10,&in,&out,&seg);
   outp (0x3c4,6);     /* unlock extended registers */
   for (i = 0;i <= 7; i++) {  /* cycle through all pixel data bits */
    outp (0x3c4,0x18);       /* arm the SG and set for pixel data bit */
    outp (0x3c5, (2 | (i<<2))); /* reset */
    outp (0x3c5, (i << 2));     / *select the data bit*/
    outp (0x3c4,0x18);
    outp (0x3c5, (1 | (i << 2)));/ *and start the SG */
    result = inp (0x3c5);       /* pre-read SG status */
    while ((result & 0x01) != 0) {  /*wait until signature is done */
      outp (0x3c4,0x18);
      result = inp (0x3c5);     /* read the status*/
    }
    outp (0x3c4,0x19);  /* get low signature byte */
    SR19 = inp (0x3c5);
    outp (0x3c4,0x1A);  /* get high signature byte */
    SR1A = inp (0x3c5);
    SIG [i] = (SR1A << 8) + SR19;
  }                             /*end of for */
  }
```

Appendix J

Pin-Scan Testing

J.1 Introduction

Pin-scan testing automatically verifies if CL-GD7541/GD7543 pins have been properly soldered to a circuit board. This test detects pins that are either not connected to the board or shorted to a neighboring pin or trace. A circuit board tester is required when using the CL-GD7541/GD7543 Pin-Scan Test mode. The frequency of the tester must be lower than 100 kHz.

Advantages of Pin-Scan Testing

The advantages of pin-scan testing are:

- Simple test patterns can verify full-board connectivity.
- During the test, the pins are automatically connected sequentially in a single chain around the CL-GD7541/GD7543 so that the value on each output pin depends only on the values applied to all other pins, rather than on the internal state of the VGA processor.
- The pin-scan logic is strictly combinatorial so that no clock pulses are required.

J.2 Performing the Pin-Scan Test

The pin-scan test is performed as follows:

1) To enter the Pin-Scan Test mode, as shown in Figure J-1, drive RESET# low at least 20 ns while TWR# is low and MD[25] is high. Then, drive RESET# high to keep Extension register bit SR24[7] equal to '1'.

2) Drive all the input pins to '0'.

3) Verify that the values on the output pins match the predicted values, which are shown in the third column from the right of Table J-1.

4) On subsequent test cycles, individually drive each input pin to a '1', and verify that all the affected output pins change to the predicted values as shown in the second column from the right of Table J-1. In the table, pin numbers are listed according to the pin-scan order: RDYRTN# is the first input, and INTR is the last output.

NOTE: Pin names in Table J-1 are for VESA® VL-Bus™ implementations. When configuring the CL-GD7541/GD7543 for PCI Bus, a few pins either change pin names or are not connected.

5) To exit the Pin-Scan Test mode, drive the RESET# from low to high while TWR# is high, as shown in Figure J-1.

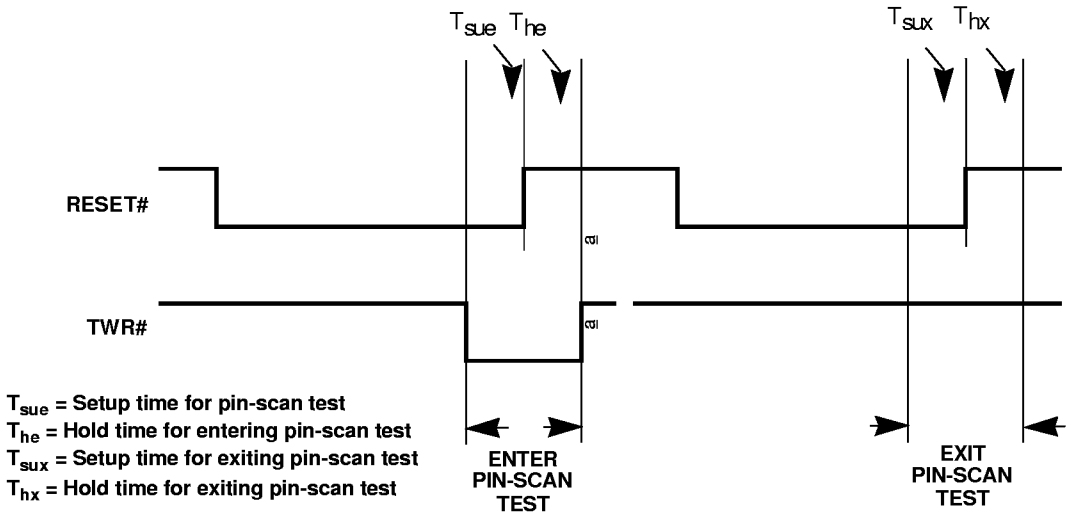


Figure J-1. Entering and Exiting the Pin-Scan Test Mode

Pins Not Tested

In the pin-scan test, the following pins are not tested:

- RESET# and TWR#
- All the power/ground pins and clock filter pins (MFILTER and VFILTER)
- RED, GREEN, and BLUE
- A[7], A[8], LDEV#, RDY#, and LCLK

J.3 Pin-Scan Test Results

During the test, if the value applied to an input pin is changed but none of the affected output pins change to the correct logic level in response, then that input pin is either shorted or not soldered correctly.

If the value applied to an input pin is changed, but *one (or some)* of the affected output pins do not change to the correct logic level in response, then that output pin is either shorted or not soldered correctly.

Table J-1. Pin-Scan Orde r

Pin No.	Pin Name	In/ Out	If all inputs = '0', predicted value of this pin is :	If all inputs except TWR# = '1', predicted value of this pin is:	PCI Pin Name
8	IRDY# / RDYRTN#	In	0	1	IRDY#
9	ADS# / FRAME#	In	0	1	FRAME#
10	IDSEL / W/R#	In	0	1	IDSEL
11	M / IO#	In	0	1	No connection
13	C / BE3#	In	0	1	C / BE3#
14	C / BE2#	In	0	1	C / BE2#
15	C / BE1#	In	0	1	C / BE1#
16	C / BE0#	In	0	1	C / BE0#
17	A2	In	0	1	No connection
18	A3	In	0	1	No connection
19	A4	In	0	1	No connection
20	A5	In	0	1	No connection
21	A6	In	0	1	No connection
24	A9	In	0	1	No connection
25	A10	In	0	1	No connection
26	A11	In	0	1	No connection
27	A12	In	0	1	No connection
28	A13	In	0	1	No connection
29	A14	In	0	1	No connection
30	A15	In	0	1	No connection
31	A16	In	0	1	No connection
32	A17	In	0	1	No connection
33	A18	In	0	1	No connection
34	A19	In	0	1	No connection
35	A20	In	0	1	No connection
37	A21	In	0	1	No connection
38	A22	In	0	1	No connection
39	A23	In	0	1	No connection
40	A[24] / HIMEM0	In	0	1	No connection
41	A[25] / HIMEM1	In	0	1	No connection

Table J-1. Pin-Scan Orde r *(cont.)*

Pin No.	Pin Name	In/ Out	If all inputs = '0', predicted value of this pin is :	If all inputs except TWR# = '1', predicted value of this pin is:	PCI Pin Name
43	AD31 / D31	In	0	1	AD31
44	AD30 / D30	In	0	1	AD30
45	AD29 / D29	In	0	1	AD29
46	AD28 / D28	In	0	1	AD28
48	AD27 / D27	In	0	1	AD27
49	AD26 / D26	In	0	1	AD26
50	AD25 / D25	In	0	1	AD25
51	AD24 / D24	In	0	1	AD24
53	AD23 / D23	In	0	1	AD23
54	AD22 / D22	In	0	1	AD22
55	AD21 / D21	In	0	1	AD21
56	AD20 / D20	In	0	1	AD20
57	AD19 / D19	In	0	1	AD19
58	AD18 / D18	In	0	1	AD18
59	AD17 / D17	In	0	1	AD17
60	AD16 / D16	In	0	1	AD16
61	AD15 / D15	In	0	1	AD15
63	AD14 / D14	In	0	1	AD14
64	AD13 / D13	In	0	1	AD13
65	AD12 / D12	In	0	1	AD12
66	AD11 / D11	In	0	1	AD11
68	AD10 / D10	In	0	1	AD10
69	AD9 / D9	In	0	1	AD9
70	AD8 / D8	In	0	1	AD8
71	AD7 / D7	In	0	1	AD7
72	AD6 / D6	In	0	1	AD6
74	AD5 / D5	In	0	1	AD5
75	AD4 / D4	In	0	1	AD4
76	AD3 / D3	In	0	1	AD3
77	AD2 / D2	In	0	1	AD2

Table J-1. Pin-Scan Orde r *(cont.)*

Pin No.	Pin Name	In/ Out	If all inputs = '0', predicted value of this pin is :	If all inputs except TWR# = '1', predicted value of this pin is:	PCI Pin Name
78	AD1 / D1	In	0	1	AD1
79	AD0 / D0	In	0	1	AD0
81	SLEEP#	In	0	1	SLEEP#
85	OSC / XVCLK	In	0	1	OSC / XVCLK
86	ACTI / FCEVIDEO# / SBYI	In	0	1	SBYI / ACTI / FCEVIDEO#
87	SUSPI / BLI	In	0	1	SUSPI / BLI
89	CLK32K	In	0	1	CLK32k
91	HSYNC	Out	1	0	HSYNC
93	VSYNC	Out	0	1	VSYNC
94	NTSC / PAL	Out	1	0	NTSC / PAL
95	CSYNC	Out	0	1	CSYNC
101	FCBLANK#	In	0	1	FCBLANK#
102	FPVEE<BIAS>	Out	1	1	FPVEE
103	VCLK / FCDCLK	Out	0	0	VCLK / FCDCLK
105	FPBL	Out	1	1	FPBL
106	FPVCC	Out	0	0	FPVCC
108	FPDE	Out	1	1	FPDE
110	LFS	Out	0	0	LFS
112	LLCLK	Out	1	1	LLCLK
113	FPVDCLK	Out	0	0	FPVDCLK
114	FP[0] / FCVCLK	In	0	1	B[0] / FCVCLK
115	FP[1] / OVRW#	Out	0	0	FP[1] / OVRW#
116	FP[2]	Out	1	1	FP[2]
117	FP[3] / MOD	Out	0	0	FP[3] / MOD
118	FP[4}	Out	1	1	FP[4}
119	FP[5]]	Out	0	0	FP[5]]
120	FP[6]	Out	1	1	FP[6]
122	FP[7]	Out	0	0	FP[7]
123	FP[8] / SBYST# / FCP[0]	In	0	1	FP[8] / SBYST# / FCP[0]
125	FP[9] / SUSPST# / FCP[1]	In	0	1	FP[9] / SUSPST# / FCP[1]

Table J-1. Pin-Scan Orde r *(cont.)*

Pin No.	Pin Name	In/ Out	If all inputs = '0', predicted value of this pin is :	If all inputs except TWR# = '1', predicted value of this pin is:	PCI Pin Name
126	FP[10]	Out	1	1	FP[10]
127	FP[11]	Out	0	0	FP[11]
128	FP[12]	Out	1	1	FP[12]
129	FP[13]	Out	0	0	FP[13]
130	FP[14]	Out	1	1	FP[14]
131	FP[15]	Out	0	0	FP[15]
133	FP[16] / FCP[2]	In	0	1	FP[16] / FCP[2]
134	FP[17] / FCP[3]	In	0	1	FP[17] / FCP[3]
135	FP[18]	Out	1	1	FP[18]
136	FP[19]	Out	0	0	FP[19]
137	FP[20]	Out	1	1	FP[20]
138	FP[21]	Out	0	0	FP[21]
139	FP[22]	Out	1	1	FP[22]
140	FP[23]	Out	0	0	FP[23]
141	FCP[4]	In	0	1	FCP[4]
142	FCP[5]	In	0	1	FCP[5]
143	FCP[6]	In	0	1	FCP[6]
144	FCP[7]	In	0	1	FCP[7]
146	TVON / XRDACCS	Out	1	1	TVON / XRDACCS
147	FCESYNC#	In	0	1	FCESYNC#
148	PROG	Out	0	1	PROG
149	SW1	In	0	1	SW1
150	SW2	In	0	1	SW2
151	MD[31]	In	0	1	MD[31]
152	MD[30]	In	0	1	MD[30]
153	MD[29]	In	0	1	MD[29]
154	MD[28]	In	0	1	MD[28]
155	MD[27]	In	0	1	MD[27]
156	MD[26]	In	0	1	MD[26]
157	MD[25] / FCPU	In	0	1	MD[25] / (FC)

Table J-1. Pin-Scan Orde r *(cont.)*

Pin No.	Pin Name	In/ Out	If all inputs = '0', predicted value of this pin is :	If all inputs except TWR# = '1', predicted value of this pin is:	PCI Pin Name
158	MD[24]	In	0	1	MD[24]
159	MD[23] / PCI-MGPU	In	0	1	MD[23] / (PCI-MGE)
160	MD[22]	In	0	1	MD[22]
161	MD[21] / S46PU	In	0	1	MD[21] / (S46)
163	MD[20]	In	0	1	MD[20]
164	MD[19] / XCLKPU	In	0	1	MD[19]
165	MD[18] / FVLPU	In	0	1	MD[18] / (FVL)
166	MD[17]	In	0	1	MD[17]
167	MD[16] / PCIPU	In	0	1	MD[16] / (PCI)
169	CAS[3]# / WE[3]#	In	0	1	CAS[3]# / WE[3]#
170	CAS[2]# / WE[2]#	In	0	1	CAS[2]# / WE[2]#
171	MA[9]	Out	1	0	MA[9]
172	MA[8]	Out	0	1	MA[8]
173	MA[7]	Out	1	0	MA[7]
174	MA[6]	Out	0	1	MA[6]
175	MA[5]	Out	1	0	MA[5]
176	MA[4]	Out	0	1	MA[4]
177	MA[3]	Out	1	0	MA[3]
178	MA[2]	Out	0	1	MA[2]
179	MA[1]	Out	1	0	MA[1]
180	MA[0]	Out	0	1	MA[0]
181	CAS# / WE#	In	0	1	CAS# / WE#
182	OE#	Out	1	1	OE#
183	RAS[0]	Out	0	0	RAS[0]
184	RAS[1]	Out	1	1	RAS[1]
186	MD[15]	In	0	1	MD[15]
187	MD[14]	In	0	1	MD[14]
188	MD[13]	In	0	1	MD[13]
189	MD[12]	In	0	1	MD[12]
190	MD[11]	In	0	1	MD[11]

Table J-1. Pin-Scan Orde r *(cont.)*

Pin No.	Pin Name	In/ Out	If all inputs = '0', predicted value of this pin is :	If all inputs except TWR# = '1', predicted value of this pin is:	PCI Pin Name
191	MD[10]	In	0	1	MD[10]
193	MD[9]	In	0	1	MD[9]
194	CAS[0]# / WE[0]#	In	0	1	CAS[0]# / WE[0]#
195	CAS[1]# / WE[1]#	In	0	1	CAS[1] / WE[1]#
196	MD[8]	In	0	1	MD[8]
197	SW[0] / MCLK / XMCLK	In	0	1	SW[0] / MCLK
202	MD[7]	In	0	1	MD[7]
203	MD[6]	In	0	1	MD[6]
204	MD[5]	In	0	1	MD[5]
206	MD[4]	In	0	1	MD[4]
207	MD[3]	In	0	1	MD[3]
208	MD[2]	In	0	1	MD[2]
1	MD[1]	In	0	1	MD[1]
2	MD[0]	In	0	1	MD[0]
5	INTR / INTR#	Out	0	1	INTR#

Appendix K

Extended Graphics Mode Programmin g

K.1 Introductio n

The CL-GD7541/GD7543 is capable of supporting a wide range of Super VGA high-resolution video graphics modes on both LCDs and CRT monitors. It supports the following graphics modes:

- 1280 × 1024 CRT monitors with up to 16 colors (interlaced)
- 1024 × 768 CRT monitors with up to 256 color s
- 800 × 600 LCDs and CRT monitors with up to 64K color s
- 640 × 480 LCDs and CRT monitors with up to 16.8 million color s

In this appendix, the Extended VGA graphics modes are described in terms of:

- Display memory organizati ons:
  - Planar mode: 16-color [Section K.2.1]
  - Packed-pixel mode: 256-color [Section K.2.2]
  - Packed-pixel mode: Direct-color (32K and 64K colors) [Section K.2.3]
  - Packed-pixel mode: Mix (either 32K-color or 256-color) [Section K.2.4]
  - Packed-pixel mode: True-color 24-bit (16.8 million colors) [Section K.2.5]
- Extended display memory addressing and mapping techniques [Section K.3]
- Programming examples demonstrating how to implement some of these features [Section K.4]

For all the extended graphics modes supported by the CL-GD7541/GD7543, refer to Chapter 4.

K.2 Display Memory Organization s

The following table compares the planar display memory organization to the packed-pixel display memory organization.

Table K-1. Comparison of Planar Mode and Packed-Pixel Mod e

Memory Organizatio n	Planar	Packed Pixe l
The CL-GD7541/GD754 3 register setting	SR7[0] = '0'	SR7[0] = '1'
Number of color s	16	256, 32K, 64K, 16.8 millio n[a]
Bits per pixe l	4 bits	1, 4, 8, 15, 16, 24 bit s[a]
Placement of pixel data in display memory	Each pixel is dispersed across 4 memory bit planes.	Only one memory plane is used. All the pixel data are in this same memory plane .
Address generatio n	Address bits are read across the memory bit plane s.	CL-GD7541/GD754 3 memory controller ha n-dles all address generation. To the CPU, the display memory appears as follows: • In segmented mode, it appears as if it were sequential, with 64 Kbytes of linearly addressable display memory in segmented mode. • In linear addressing mode, the display memory appears as 1 or 2 Mbytes of linearly addressable memory .
Page address mappin g	Resolutions above 102 4 × 768 require page address mapping .	Always requires page address mapping .

[a] When SR7[0] = '1', the 256-color packed-pixel mode (8 bits per pixel) is the default .

K.2.1 Planar Mode: 16-Color

The CL-GD7541/GD7543 16-color planar display memory mode is enabled when Sequencer register bit SR4[2] is set to '1' and bit SR4[3] is set to '0'. This standard IBM VGA display memory mode requires 4 bits per pixel. This VGA mode represents a pixel by dispersing bits of information across 4 display memory planes, with 1 bit per plane. The display memory is organized as bytes, with 8 pixels per byte.

The memory planes are overlaid in the CPU memory address space so that each plane occupies the same CPU address. For read/write operations, the CPU can access any of these planes independently by programming the Sequencer register SR2. Figure K-1 shows the display memory organized in four planes for the 16-color planar mode. The color information for each pixel is stored in corresponding bits across four planes. The figure also depicts how bank 0 and bank 1, which are used in paging, are aligned across each plane.

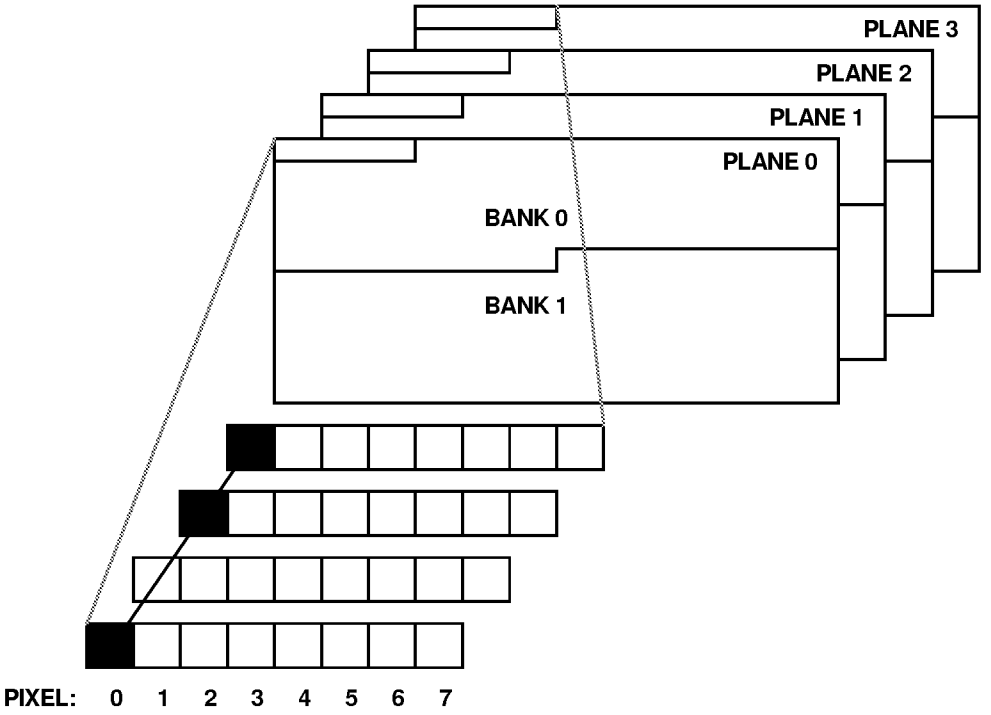


Figure K-1. 16-Color Planar Modes

The standard IBM VGA supports 256 Kbytes of display memory. In 16-color planar mode, the display memory is divided into four planes with 64 Kbytes per plane. Normally, the 64-Kbyte segment of each plane is mapped in A0000h to AFFFFh, and the CPU can easily address each of the display memory planes.

However, a problem arises for those graphics modes that require more than 64 Kbytes of addressable video memory per plane. For example, the 1024×768, 16-color planar mode requires 98,304 bytes, or an additional 32,768 bytes more addressable display memory per plane. The problem of having more than 64 Kbytes of addressable display memory is solved by using the extended display memory addressing techniques discussed in Section K.3.

K.2.2 Packed-Pixel Mode: 256-Color

By setting Extension register bit SR7[0] to '1', the 256-color packed-pixel mode is enabled. When Sequencer register bit SR4[3] is set to '1', this mode becomes Chain-4 mode.

The following figure shows how 8-bit-per-pixel (packed-pixel mode) bytes are stored in terms of the physical plane organization.

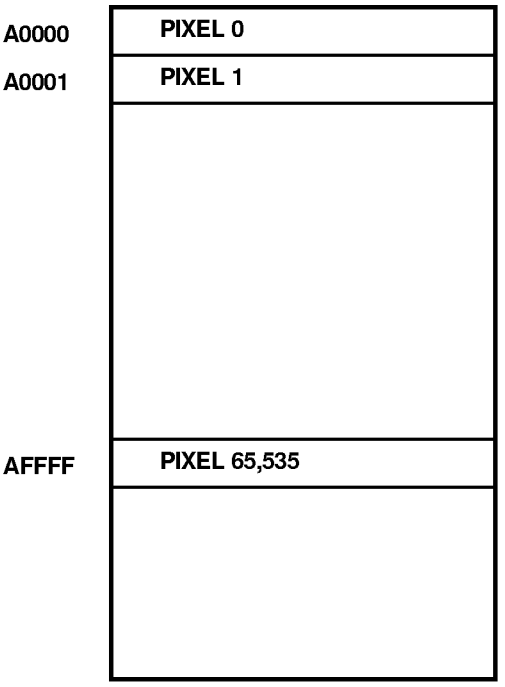


Figure K-2. 256-Color Packed-Pixel Mode

The CL-GD7541/GD7543 on-chip memory controller makes this organization completely transparent. Hence, to the CPU, addressing is sequential. For example, at segment A0000h, pixel 0 resides at offset 0, pixel 1 resides at offset 1, and pixel 65,535 resides at offset 65,535.

To address display memory that is beyond the 64-Kbyte segment boundary, the CL-GD7541/GD7543 supports a display memory paging technique that allows up to 2 Mbytes of display memory to be paged into the CPU address range.

In Linear Memory Addressing mode, display memory paging is not required.

K.2.3 Packed-Pixel Mode: Direct-Color (32K and 64K Colors)

The CL-GD7541/GD7543 supports direct-color packed-pixel modes that are capable of displaying up to either 32,768 (32K) colors or 65,536 (64K) colors simultaneously, at screen resolutions of up to 800×600. Color information used to display these colors simultaneously is:

- 15 bits per pixel for 32K colors
- 16 bits per pixel for 64K colors

To enable direct-color modes, Extension register bit SR7[0] is set to 1, and then the CL-GD7541/GD7543 internal palette DAC is set to direct-color modes by programming Extension register HDR (the Hidden DAC register).

Figure K-3 shows how 15-bit pixel data (for 32K colors) is stored relative to the physical plane organization. The RGB color information is stored in 5-5-5 format (5 bits each for red, green, and blue). Two bytes per pixel are used for storing the color information. The most-significant bit (bit 15) is ignored.

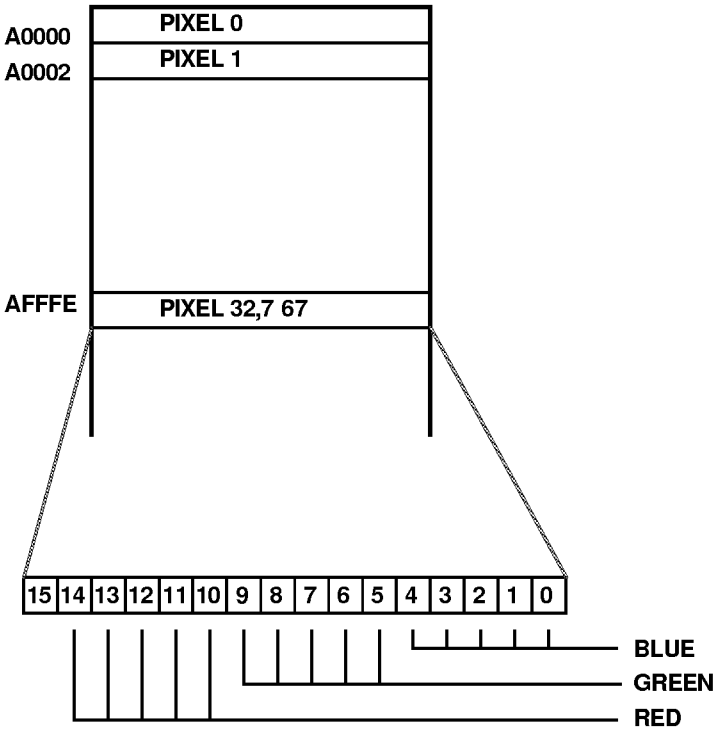


Figure K-3. 32,768 Color (15-Bit) Packed-Pixel Mode

Figure K-4 shows how 16-bit pixel data (for 64K colors) is stored in terms of the physical plane organization. The RGB color information is stored in 5-6-5 format (5 bits of red, 6 bits of green, and 5 bits of blue). Two bytes per pixel are used for storing the color information.

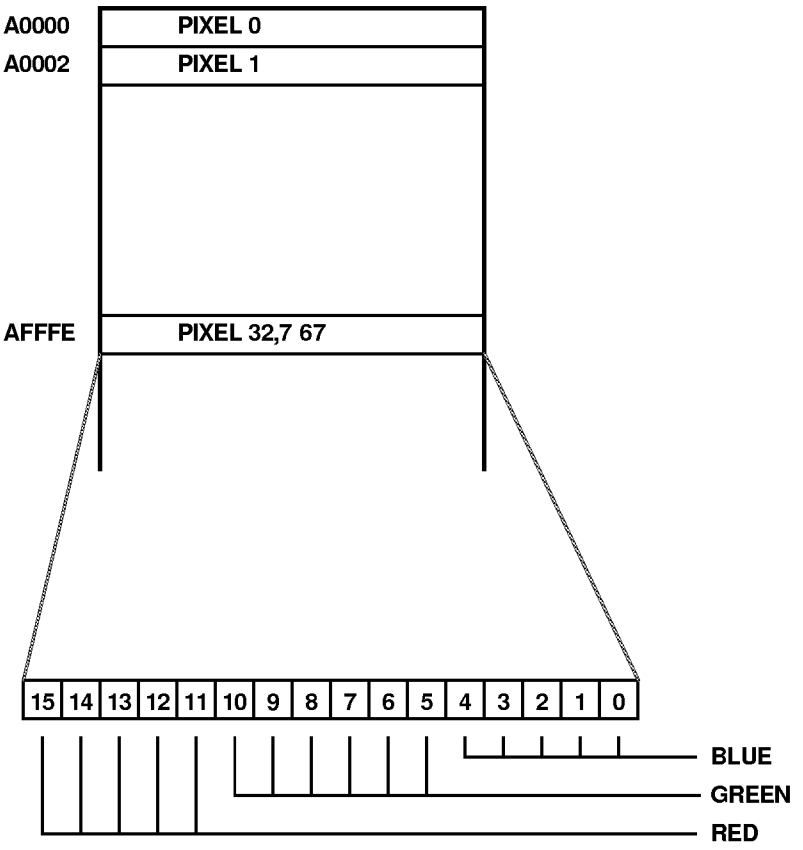


Figure K-4. 65,536 Color (16-Bit) Packed-Pixel Mode

As in the 256-Color Packed-Pixel Graphics mode (refer to Section K.2.2), the CL-GD7541/GD7543 on-chip memory controller makes this organization completely transparent, and so to the CPU, addressing is sequential. For example, at segment A0000h, pixel 0 resides at offset 0 and offset 1; pixel 1 resides at offset 2 and offset 3; and pixel 32,767 resides at offset 65,534 and offset 65,535.

To address display memory that is beyond the 64-Kbyte segment boundary, the CL-GD7541/GD7543 supports a display memory paging technique that allows up to 2 Mbytes of display memory to be paged into the CPU address range.

K.2.4 Packed-Pixel Mode: Mixed (Either 32K-Color or 256-Color)

The CL-GD7541/GD7543 supports a Mixed-Color mode that is capable of combining RGB 5-5-5 format (32K-color packed-pixel mode) and 8-bit-per-pixel format (256-color packed-pixel mode).

To enable the Mixed-Color mode, Extension register SR7[0] is set to '1', and then the CL-GD7541/GD7543 internal palette DAC is set to a mixed-mode format by programming Extension register HDR (the Hidden DAC register).

In the mixed-mode operation, pixel data bit [15] is used to choose between the 32K-color and the 256-color modes as follows:

- If bit[15], the most-significant bit of the 16-bit pixel data, is '0', then bits [14:0] are treated as 5-5-5 RGB data.
- If the most-significant bit is set to '1', then bits [7:0] choose a palette entry in the palette DAC LUT (lookup table) to display 256 colors simultaneously, and bits [14:8] are ignored.

Figure K-5 shows how the mixed-color packed-pixel data is stored in terms of the physical plane organization.

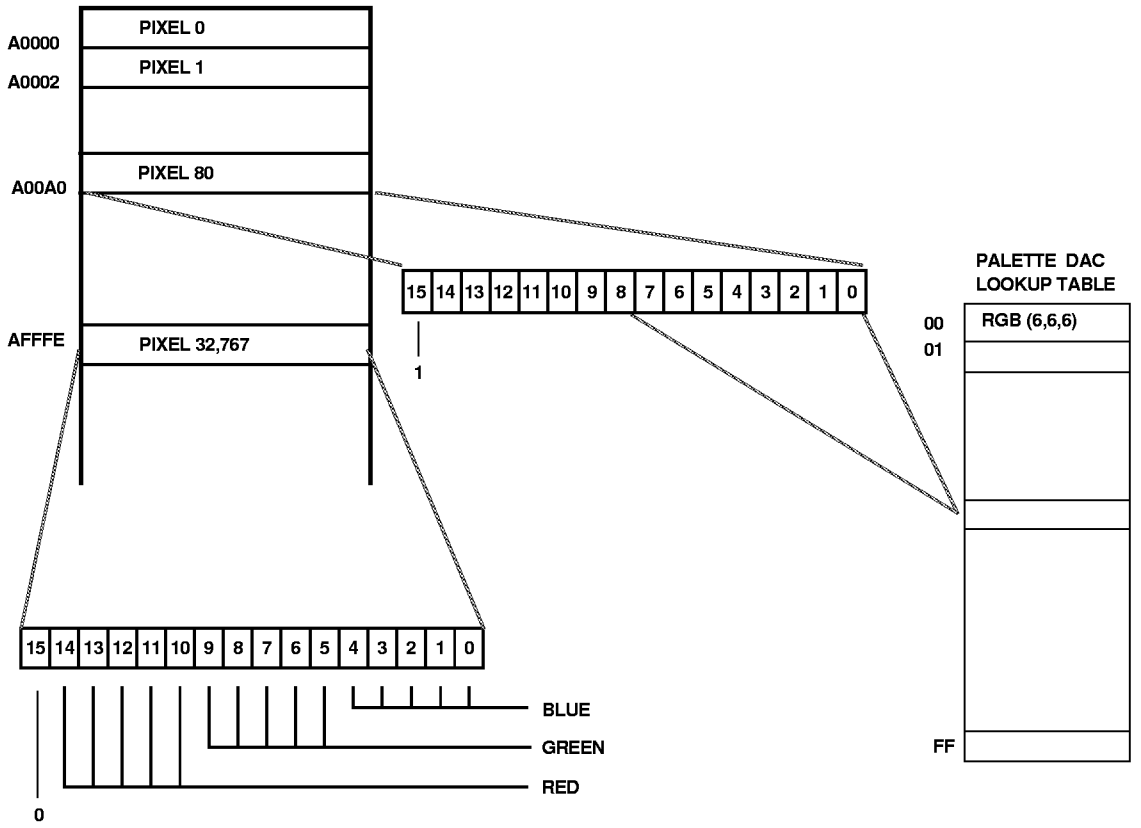


Figure K-5. Mixed-32,768-Color (15-Bit) Packed-Pixel Data Format

The CL-GD7541/GD7543 on-chip memory controller makes this organization completely transparent, and so to the CPU, addressing is sequential. For example, at segment A0000h, pixel 0 resides at offset 0 and offset 1; pixel 1 resides at offset 2 and offset 3; and pixel 32,767 resides at offsets 65,534 and 65,535

To address display memory that is beyond the 64-Kbyte segment boundary, the CL-GD7541/GD7543 supports a display memory paging technique that allows up to 2 Mbytes of display memory to be paged into the CPU address range.

K.2.5 True Color, 24-Bit (16.8 Million Colors) Packed-Pixel Mode

The CL-GD7541/GD7543 supports a True-Color mode capable of displaying 16.8 million colors simultaneously at screen resolutions of up to 640 × 480. To display 16.8 million colors in TARGA™-compatible mode, 24 bits per pixel of RGB color information (8 bits each for red, green, and blue) are used

To enable the Mixed-Color mode, Extension register SR7[0] is set to '1', and the CL-GD7541/GD7543 internal palette DAC is set to a True-Color-mode format by programming the Hidden DAC register (HDR).

Figure K-6 shows how 24-bit pixel data is stored in terms of the physical plane organization. Three bytes per pixel are used for storing the color information.

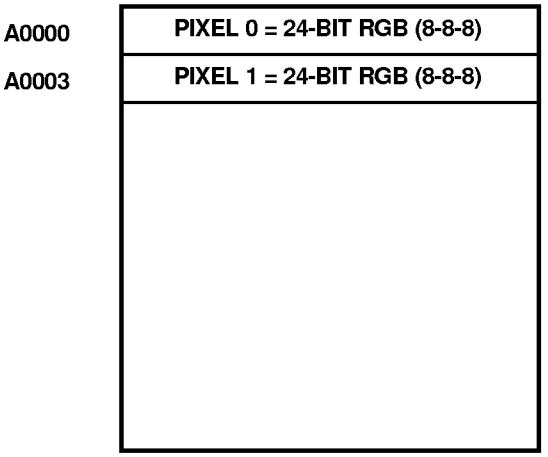


Figure K-6. 24-Bit True Color Packed-Pixel Mode

The CL-GD7541/GD7543 on-chip memory controller makes this organization of the physical plane completely transparent. Hence, to the CPU, the byte addressing is sequential. For example, at segment A0000h, pixel 0 resides at offset 0 to offset 2 as follows:

- Blue color information at offset 0
- Green color information at offset 1
- Red color information at offset 2

Similarly, pixel 1 resides at offset 3 to offset 5; pixel 21,845 resides at offset 65,533 to offset 65,535.

To address display memory beyond the 64-Kbyte-segment boundary, the CL-GD7541/GD7543 supports a display memory paging scheme that allows up to 2 Mbytes of display memory to be paged into the CPU address range.

K.3 Extended Video Display Memory Addressing Techniques

The CL-GD7541/GD7543 addresses up to 2 Mbytes of display memory. However, in the DOS environment, at A0000h–BFFFFh, only 128 Kbytes of address space are reserved for video display memory. As a result, if the CL-GD7541/GD7543 has to share this memory space with MDA, Hercules®, or CGA controllers, it is left with only a single 64-Kbyte segment from A0000h to AFFFFh.

To extend the address space for the display memory, the CL-GD7541/GD7543 supports the techniques shown in Table K-2 for video display memory address mapping.

Table K-2. Video Display Memory Address Mapping Techniques

Mapping Technique	Reference	Description of Mapping Technique
Linear	Section K.3.1	Allows display memory to be mapped to a continuous 2-Mbyte region above the standard 1-Mbyte DOS address space.
Single-Page	Section K.3.2	Allows one 64-Kbyte segment of display memory to be mapped into CPU address space.
Dual-Page	Section K.3.3	Allows two 32-Kbyte segments of display memory to be mapped into CPU address space.

K.3.1 Linear Address Mapping

Linear address mapping allows video display memory to be mapped to a continuous 2-Mbyte region above the standard 1-Mbyte DOS address space. This action allows application programs to access the display memory as a linearly addressed string of up to 2 Mbytes, instead of being constrained to a 64-Kbyte window.

To use the CL-GD7541/GD7543 linear-addressing feature:

- The drivers that are used must be written so as to ensure compatibility with the operating system.
- Extension register GRB[0] must be set to '0'.

K.3.2 Single-Page Address Mappin g

- Single-page address mapping extends the address space for video display memory. As shown in Figure K-7 below, and as described in this section, single-page address mapping allows the following actions :
- Any 64-Kbyte segment (or 'page') of display memory can be mapped into address range A0000h–AFFFFh of the CPU host address.
- The Start Page Address can begin :
  - — At any 4-Kbyte boundary of 1-Mbyte display memor y
  - — At any 16-Kbyte boundary of 2-Mbyte display memor y

After the 64-Kbyte segment of display memory is mapped into the CPU host address range, it can be accessed by the CPU for read and write operations.

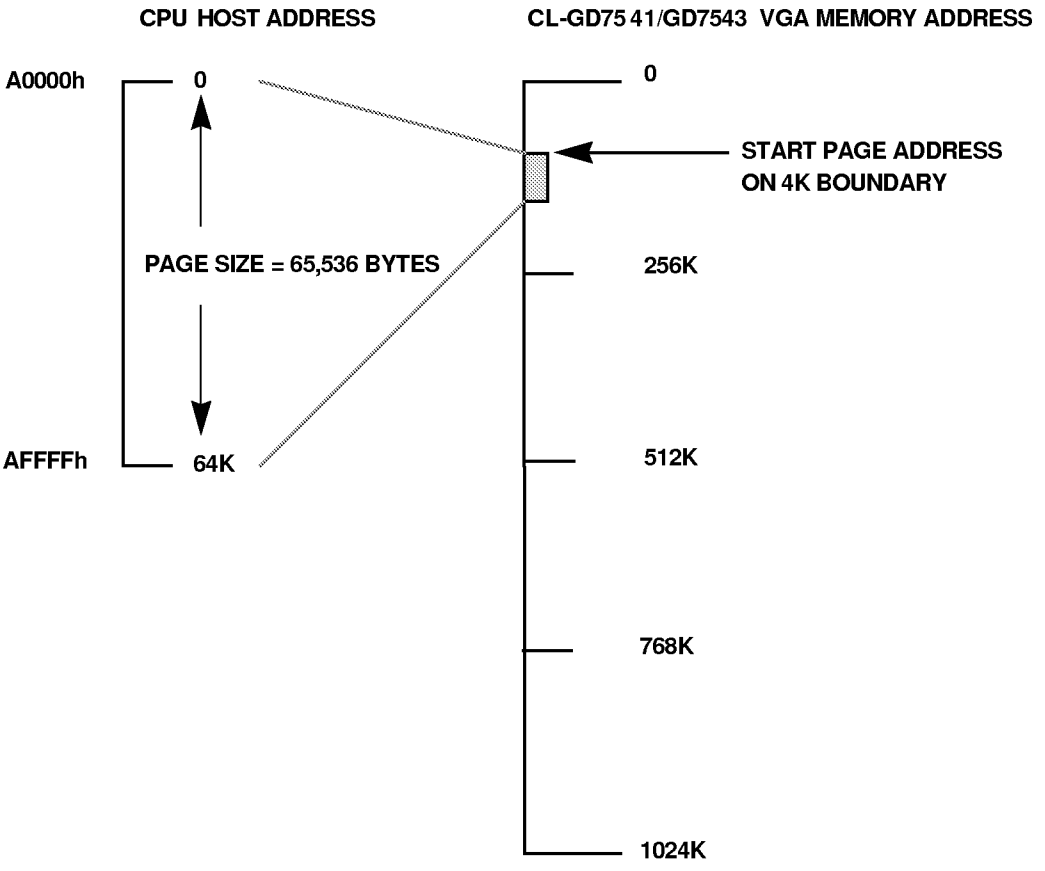


Figure K-7. Single-Page Address Mapping Techniqu e

To select a 64-Kbyte segment of display memory and map it into the CPU host address range, take the following actions:

- To always select only a 64-Kbyte segment of display memory (and never two 32-Kbyte segments), select Offset Register 0 by setting th e Extension register bit GRB[0] to '0'.
- To select the desired address, program Extension register GR9 (Offset register 0). The value that is pr o-grammed into these register bits is then added to CPU address bits to provide the address for mapping the display memory.

Figure K-8 and Figure K-9 show how Offset register 0 and the CPU Address bits are added to generate the display memory address.

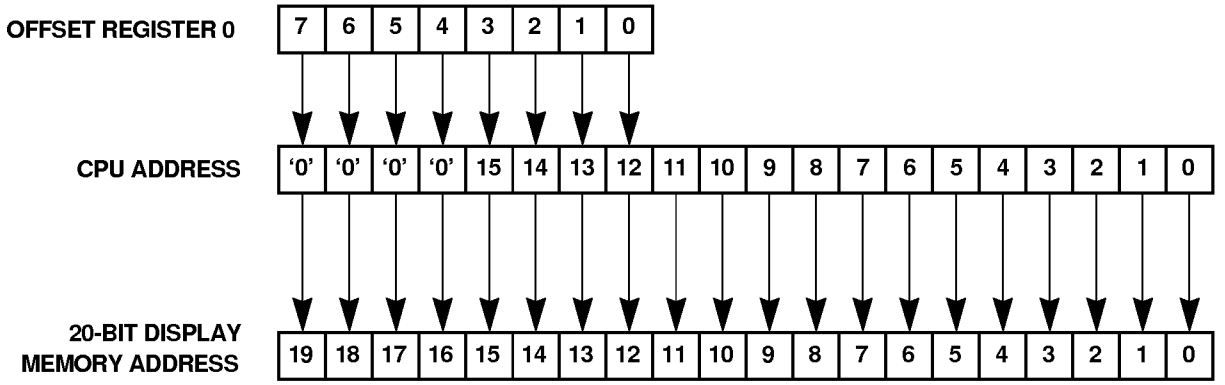


Figure K-8. 64K Page-Mode Remapping Adder Alignment for 1-Mbyte Memor y

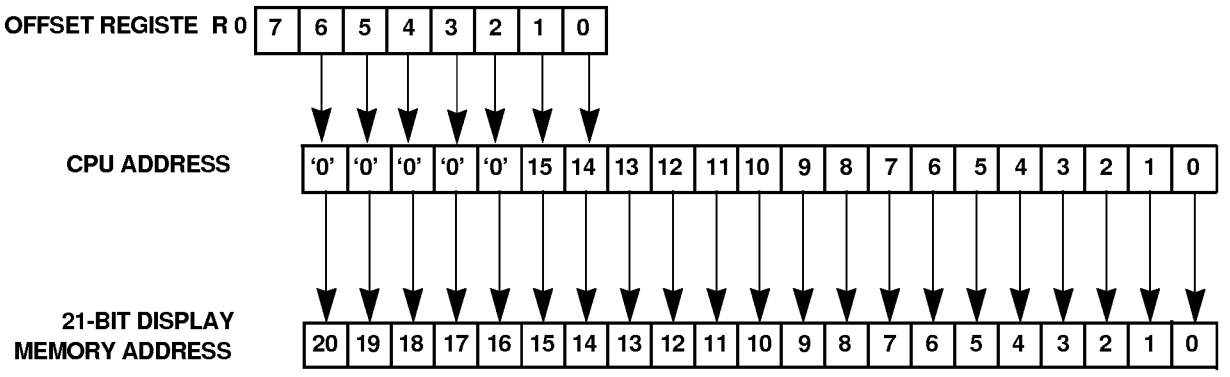


Figure K-9. 64K Page-Mode Remapping Adder Alignment for 2-Mbytes Memory

K.3.3 Dual-Page Address Mapping

Dual-page address mapping is used for read-modify-write operations on large blocks of data. As shown in Figure K-10, and as described in this section, dual-page address mapping allows the following:

- Two 32-Kbyte segments (or 'pages') of display memory can be mapped into address ranges A0000h–A7FFFh and A8000h–AFFFF of the CPU host address.
- The 32-Kbyte segments may be either separate or overlapping.
- The Start Page Address can begin at any 4-Kbyte boundary of display memory.

After the two 32-Kbyte segments of display memory are mapped into the CPU host address range, they can be accessed by the CPU for read and write operations. This action allows for block transfers of data bits, by using repeated 'move string' DMA instructions.

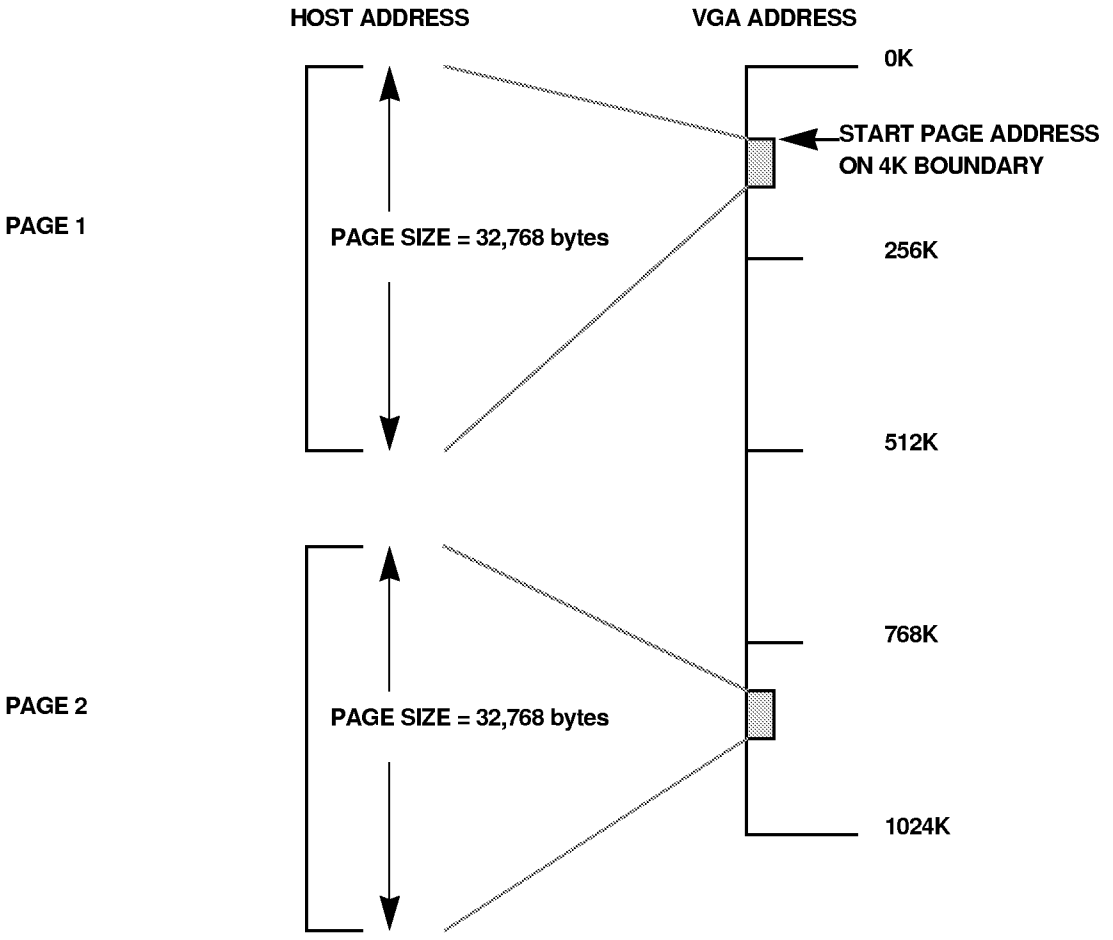


Figure K-10. Dual-Page Address Mapping Scheme

To select any two separate or overlapping 32-Kbyte segments of display memory and then map them into the CPU host address range, perform the following actions:

- Select which one of the two CL-GD7541/GD7543 Offset registers is used to calculate the resulting value of the display memory address as follows:
  - To select Offset register 0, set Extension register GRB[0] to '1'.
  - To select Offset register 1, clear Extension register GRB[0] to '0'.
- Program the start page addresses as follows:
  - To determine the start address of page 1, program Offset register 0 in Extension register GR9[7:0].
  - To determine the start address of page 2, program Offset register 1 in Extension register GRA[7:0].
- The start page address can begin
  - At any 4-Kbyte boundary of 1-Mbyte display memory
  - At any 16-Kbyte boundary of 2-Mbyte display memory

For a page size of 32 Kbytes, Figure K-11 shows how an Offset register (either 0 or 1) and CPU address bits are added to find the resulting display memory address of 1-Mbyte display memory. Note that in the figure, bit 15 of the CPU address selects whether Offset register 0 or Offset register 1 is used for the display memory addressing.

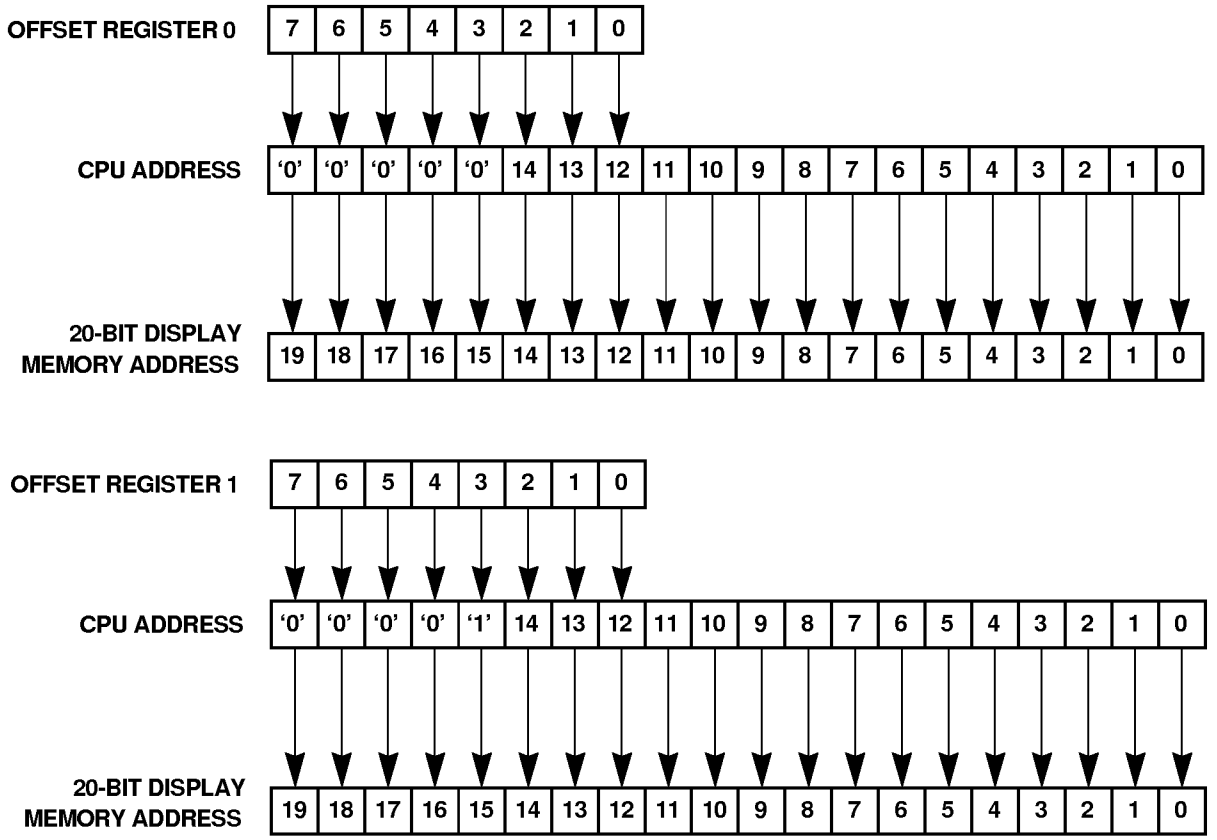


Figure K-11. 32K Page-Mode Remapping Adder Alignment for 1-Mbyte Display Memory

The following table lists the CL-GD7541/GD7543 Extension registers that control the CPU base address and display memory mapping functions:

Table K-3. CL-GD7541/GD754 3 Extension Register s

Function	Name of Extension Register	Port	Index	Bit	Value
Single-page	GRB: Graphics Controller Mode Extension s	3CF	0B	GRB[0]	0
Dual-page	GRB: Graphics Controller Mode Extension s	3CF	0B	GRB[0]	1
Offset register granularit y: 4 Kbyte	GRB: Graphics Controller Mode Extension s	3CF	0B	GRB[5]	0
Offset register granularit y:16 Kbyte	GRB: Graphics Controller Mode Extension s	3CF	0B	GRB[5]	1
Linear addressing	SR7: Graphics Controller Mode Extension s	3C4	07	SR7[7:4]	15...0
Offset register 0	GR9: Offset register 0	3CF	09	GR9[7:0]	255...0
Offset register 1	GRA: Offset register 1	3CF	0A	GRA[7:0]	255...0

K.4 VGA Programming Examples

This section provides the CL-GD7541/GD7543 software programming examples.

K.4.1 Unlocking the CL-GD7541/GD7543 Extension Registers

To identify a CL-GD754X VGA as the VGA that is being used, call the extended VGA BIOS inquiry function by using INT 10h. However, if an extended VGA BIOS is not available, then identify a controller by:

- Programming the Unlock All Extension register (Extension register SR6) to enable the CL-GD7541/GD7543 extension registers.
- Reading the Chip ID register (Extension register CR27).

The following code show the steps to enable/disable CL-GD7541/GD7543 extended register access:

```
Enable Extension Register Macro:
;    Function:
;    Enabling Extensions
;     Calling Protocol:
;    enable_extensions

     enable_extensions macro
     mov    dx,03c4h              ; select Extended register SR6 i/o port
     mov    al,06h                ; unlock All Extension register index
     mov    ah,12h                ; load with xxx1x010 to enable extension
     out    dx,ax                 ; write index and data
     endm


Disable Extension Register Macro:

     ; Function:
     ;      Disabling Extensions

     ; Calling Protocol:
     ;      disable_extensions

     disable_extensions macro
     mov    dx,03c4h              ; select Extended register SR6 I/O port
     mov    al,06h                ; unlock All Extension register index
     mov    ah,00h                ; load with 00 to disable extension
     out    dx,ax                 ; write index and data
     endm
```

K.4.2 Identifying a CL-GD7541/GD754 3 VGA Controlle r

Extension register CR27 (Chip ID register) is used to identify a CL-GD754X VGA controller. The following sample code shows how to program the extension registers to read the chip ID for aCL-GD7541 and how to determine the chip type.

```
;Function: Identify Cirrus Logic CL-GD7541 Super VGA LCD Controlle r
;Input Parameters:;none
;Output Parameters:
;      AL =00    ID FAILED
;      AL =0B    CL-GD7541
; Calling Protocol:
; VGAchip = Id_CL-GD7541()*/

_Id_CL-GD7541 proc far
      mov      dx,03c4h    ; load Unlock All Extensions I/O por t
      mov      al,06       ; load SR6 register inde x
      out      dx,al       ; write index and data registe r
      inc      dx          ;
      in       al,dx       ; read data registe r
      mov      ah,00h      ;
      cmp      al,12h      ; check SR6 read back val ue
      jne      chk29       ; see if this is a CL-GD7541 (no SR6)
exit: mov      al,ah       ; return in AL the chip  ID value
      xor      ah,ah       ; zero AH
      ret
chk29:mov      dx,03d4h    ; load chip ID CR27 I/O port retur n
      mov      al,27h      ; select CR27 inde x
      out      dx,al       ;
      inc      dl          ;
      in       al,dx       ; read chip ID
      shr      al,1        ; shift to discard
      shr      al,1        ; revision level bit s
      mov      ah,0Bh      ;
      cmp      al,2Ch      ; check for CL-GD7541 ID
      je       exit        ; yes it was
      xor      ah,ah       ; no it wasn't
      jmp      exit
_Id_CL-GD7541 endp
```

K.4.3 Initializing the CL-GD7541/GD754 3 Extended Graphics Mode By Using an INT 10h Cal l

The following listing is used to initialize the desired extended graphics mode by calling the Cirrus Logic VGA BIOS set mode function: (This example is for the CL-GD7541.)

```
;Set graphics mode
;set up Extended graphics mode supported by CL-GD7541 VGA LCD BIOS
;
;Calling Protocol
; al = desired CL-GD7541 graphics mode number
;Return
; al = current graphics mode
;
Set_Video_Mode proc near
      mov ah,0 ; VGA BIOS setmode function 0
      int 10H  ; call VGA BIOS interrupt 10 Hex, al = mode number
      mov ah,0Fh; VGA BIOS get current graphics mode number
      int 10h  ;
      ret      ; return current graphics mode number in al
Set_Video_Mode endp
```

K.4.4 Programming Mapping Register s

K.4.4.1 Setting Up Single-Page Mappin g

The following code listing shows how to program Extension register GRB to set up single-page mapping.

```
; Single Page Mapping
; Set up Single-Page Mapping

; Calling Protocol
;     Set_Single_Page

Set_Single_Page proc near
;set up CPU Base Address Control  register for single page, 64K page size
      mov      dx,03ceh     ; select GRB extension register  I/O port
      mov      al,0bh       ; select GRB register index
      out      dx,al        ; write index register
      inc      dx           ; inc dx to read data port
      in       al,dx        ; read data
      and      al,feh       ; apply mask to set GRB[0] = 0
      out      dx,al        ; write I/O port with new data
      ret
Set_Single_Page   endp
```

K.4.4.2 Programming for Single-Page Address Mapping with a 64-Kbyte Segmen t

The following code listing shows how to program Offset Register 0 (GR9) to map a desired page (64 Kbytes) of display memory into the CPU address.

```
;Function:
;Load the Single Page Offset Register 0 with the new start addres s
;of a 64 Kbyte segment
; Input:
; bl = 0..255
; page number for start address of desired 64 Kbyte segment
;
; Calling Protocol:
; Select_Single_Page

Select_Single_Page macro
      mov      dx,3CEh      ; load GR09 extension register  I/O port
      mov      al,09h       ; load Offset Register 0 index
      mov      ah,bl        ; get page number
      out      dx,ax        ; program selected page
Select_Single_Page endm
```

K.4.4.3 Setting Up Dual-Page Address Mappin g

The following code listing shows how to program Extension register GRB to set up dual-page mapping.

```
; Dual Page Mapping
;      Setup Dual-Page Mapping
;
; Calling Protocol
;      Set_Dual_Page

Set_Dual_Page proc far

; set up Graphics Controller Mode Extensions  register for dual page size
      mov      dx,03ceh     ; select extension register  I/O port
      mov      al,0bh       ; select CPU Base Address  register index
      out      dx,al        ; write index register
      inc      dx           ; inc dx to read data port
      in       al,dx        ; read data
      or       al,01h       ; data = enable 32K page size, dual page
      out      dx,al        ; write I/O port with new data
      ret
Set_Dual_Page  endp
```

K.4.4.4 Programming for Dual-Page Address Mapping with a 32-Kbyte Segmen t

The following code listing shows how to program Extension registers GR9 and GRA to set up dual-page remapping with a 32-Kbyte segment.

```
;Function:
;Load the Dual-Page Remapping  registers with the new star address
;at 32 Kbyte segments

; Input:
;bl = 0..255 page number for segment mapped to  A0000h-AFFFFh
;bh = 0..255 page number for segment mapped to  A8000h-AFFFFh

; Calling Protocol:
;Select_Dual_Pages

Select_Dual_Pages macro
mov   dx,3CEh  ; load extension register  I/O port
mov   al,09h   ; load CPU Base Addr. Mapping Register A index
mov   ah,bl    ; get page number for A0000h-A7FFFh mapping
out   dx,ax    ; program selected page
mov   al,0ah   ; load CPU Base Addr. Mapping Register A index
mov   ah,bh    ; get page number for  A8000h-AFFFFh mapping
out   dx,ax    ; program selected page
Select_Dual_Pages endm
```

Appendix L

Hardware Configuration Notes

L.1 Introduction

The CL-GD7541/GD7543 memory data pins are used to program the CL-GD7541/GD7543 for operation. The resistance that appears on the memory data pins is read during the low-to-high transition of the system reset pulse, and the resulting status of the inputs is stored in Extension registers SR22 and SR24.

- If no external pull-up resistor is present on a memory data pin, the pin is read as low because of the CL-GD7541/GD7543 internal pull-down resistor.
- If an external pull-up resistor is present on a memory data pin, the pin is read as high.

The hardware configuration data can be latched into Extension registers SR22 and SR24 by programming software for the high-to-low transition of Extension register bit SR24[3]. This action can be used if the system reset is not long enough to read the hardware configuration data.

NOTE: Some of the software-programmable register bits that are used to select the desired function of some multi-function pins are covered in the Cirrus Logic 'motherboard' application note in the *CL-GD754X Application Book*.

L.2 Configuration Summary

Each of the CL-GD7541/GD7543 MD[25:16] pins has an internal pull-down resistor (nominally 40 kΩ). If no pull-up resistor is attached, the default is '0'. If '1' is to be loaded into the latch associated with a given MD line, an external pull-up resistor (typically 60 kΩ) must be added. The following table provides an overview of the configuration bits. The third column from the left describes the CL-GD7541/GD7543 pin functions when a pull-up resistor is installed on the CL-GD7541/GD7543.

Table L-1. Configuration Bits

CL-GD7541/GD7543 Pin (Memory Data Bit)	Extension Register Latch	Function of CL-GD7541/GD7543 Pin When Pull-up Resistor Is Installed on the Memory Data Pin	Note
MD [25]	SR24[7]	Enable Feature Connector	
MD [24]	–	Reserved	
MD [23]	SR22[7]	Extend PCI bus with Min-grant	a
MD [22]	SR22[6]	Select dynamic-frame buffer sharing (CL-GD7541 only)	
MD [21]	SR22[5]	Select Sleep Address 46E8[3]	
MD [20]	–	Reserved	
MD [19]	SR22[3]	Select external memory and video clocks	
MD [18]	SR22[2]	Select 50-MHz VESA® VL-Bus™	a
MD [17]	–	Reserved	
MD [16]	SR22[0]	Select 32-bit PCI bus	a

[a] Bus select bits in Extension register SR22[7, 2, 0] are mutually exclusive. Only one of them can be high at any time. If no pull-up resistor is supplied, the device is configured for VESA® VL-Bus™ operation ≤ 33 MHz.

L.3 Configuration Details

Select 32-Bit PCI Bus:

- An external pull-up on MD[16] / PCIPU reads back a '1' in Extension register SR22[0], which selects the PCI bus configuration for the CL-GD7541/GD7543.

Select VESA VL-Bus > 33 MHz:

- An external pull-up on MD [18] / FVLPU reads back '1' in Extension register SR22[2], which selects a VESA® VL-Bus™ operation > 33 MHz for the CL-GD7541/GD7543.

External Clock Select:

- An external pull-up on MD [19] / XCLK reads back a '1' in Extension register SR22[3], which powers-down the internal clock synthesizers for MCLK and VCLK and enables the external XMCLK and XVCLK inputs.
- No pull-up reads back '0', and so the internal clocks are used (the default). This configuration is used for manufacturing test.

Sleep Address Select:

- An external pull-up on MD[21] / S46PU reads back a '1' into Extension register SR22[5], which selects I/O address 46E8h as the sleep address.
- No pull-up reads back '0', indicating the selection of sleep address 3C3h, the default.

Dynamic Frame-Buffer Sharing Select (CL-GD7541 Only):

- An external pull-up on MD[22] / DFBSPU reads back a '1' into Extension register SR22[6], which configures the CL-GD7541 for dynamic frame-buffer sharing.

32-Bit PCI Bus Select with Min-Grant Extended:

- An external pull-up on MD[23] / PCI-MGPU reads back a '1' into Extension register SR22[7] and into the PCI Configuration register 3CH offset 2. This action selects the 32-bit PCI bus and extends the Min-grant timing from 8 PCI CLKs (≈ 250 ns at 33 MHz) to 16 PCI CLKs (≈ 500 ns).
- The CL-GD7541/GD7543 drives the STOP# output low under the following conditions:
  - — when the CL-GD7541/GD7543 is at the end of the Min-grant period
  - — when the CL-GD7541/GD7543 is in Burst mode
  - — when the TRDY# output from the CL-GD7541/GD7543 has *not* gone low for more than the Min-grant period (and so the PCI bus controller can start a retry)

Feature Connector Video Port Enable:

- An external pull-up resistor on MD[25] / FCPU reads back a '1' into Extension register SR24[7] on the low-to-high transition of the system reset pulse and configures all appropriate pins for the Feature Connector video port.
- When no pull-up is used, these pins revert to their other functions and are disabled (that is, inputs are ignored and outputs are high-impedance).

BIT NAME INDEX

Numerics

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GENERAL INDEX

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