DATA SHEET

SUNPLUS

SPLC562C

240 COM/SEG Driver for STN LCD

SEP. 17, 2004

Version 1.2

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240 COM/SEG DRIVER FOR STN LCD

1. GENERAL DESCRIPTION

The SPLC562C is a 240-output segment/common driver IC suitable for driving large/medium scale dot matrix LCD panels, and is used in personal computers/work-stations. Through the use of SST (Super Slim TCP) technology, it is ideal for substantially decreasing the size of the frame section of the LCD module. The SPLC562C is good both as a segment driver and a common driver, and it can create a low power consuming, high-resolution LCD.

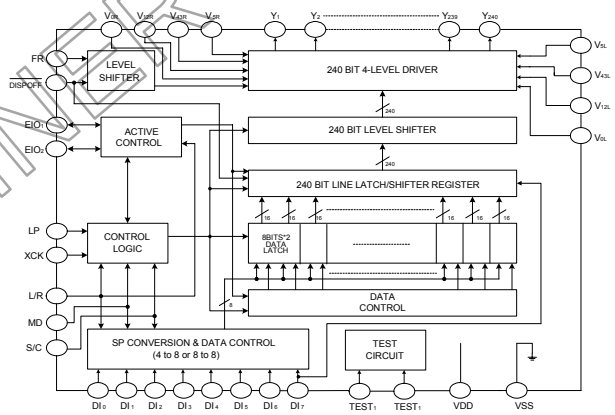
2. FEATURES

■ Both Segment Mode and Common Mode
- ─ Number of LCD drive outputs: 240
- ─ Supply voltage for LCD drive: +15V to +30V
- ─ Supply voltage for the logic system: +2.5V to +5.5V
- ─ Low power consumption
- ─ Low output impedance
- ─ CMOS silicon gate process (P-type silicon substrate)
- ─ Package: 278-pin TCP (Tape Carrier Package) & Au bump chip

■ Segment Mode
- ─ Shift clock frequency:
  1). 20MHz (Max.) (VDD = +5.0V ± 10%)
  2). 15MHz (Max.) (VDD = +3.0V to +4.5V)
  3). 12MHz (Max.) (VDD = +2.5V to +3.0V)
- ─ Adopts a data bus system
- ─ 4-bit / 8-bit parallel input modes are selectable with a mode (MD) pin
- ─ Automatic transfer function of an enable signal
- ─ Automatic counting function which, in the chip select mode, causes the internal clock to be stopped by automatically counting 240 bit of input data
- ─ Line latch circuits are reset when $\overline{\text{DISPOFF}}$ active

■ Common Mode
- ─ Built-in 240 bits bi-directional shift register (divisible into 120-bits X 2)
- ─ Shift clock frequency: 4.0MHz (Max.) (VDD = +2.5V to +5.5V)
- ─ Available in a single mode(240 bits shift register) or in a dual mode (120 bits shift register x 2)
  1). Y_1 -> Y_{240} Single mode
  2). Y_{240} -> Y_1 Single mode
  3). Y_1 -> Y_{120}, Y_{121} -> Y_{240} Dual mode
  4). Y_{240} -> Y_{121}, Y_{120} - Y_1 Dual mode
  The above 4 shift directions are pin-selectable
- ─ Shift register circuit reset function when $\overline{\text{DISPOFF}}$ active

3. BLOCK DIAGRAM



Remark: The TCP's external shape is customized. To order your TCP's external shape, please contact SUNPLUS salesperson.

3.1. Block Function

3.1.1. Active control

In case of segment mode, controls the selection or non-selection of the chip. Following a LP signal, and after the chip select signal is input, a select signal is generated internally until 240 bits of data have been read in. Once data input has been completed, a select signal for cascade connection is output, and the chip is non-selected. In case of common mode, controls the input/output data of bidirectional pins.

3.1.2. SP Conversion & Data Control

In case of segment mode, keep input data which are 2 clocks of XCK at 4-bit parallel mode into latch circuit, or keep input data which are 1 clock of XCK at 8-bits parallel mode into latch circuit, after that they are put on the internal data bus 8 bits at a time.

3.1.3. Data latch control

In case of segment mode, selects the state of the data latch which reads in the data bus signals. The shift direction is controlled by the control logic, for every 16 bits of data read in, the selection signal shifts one bit based on the state of the control circuit.

3.1.4. Control logic

Controls the operation of each block. In case of segment mode, when a LP signal has been input, all blocks are reset and the control logic waits for the selection signal output from the active control block. Once the selection signal has been output, operation of the data latch and data transmission are controlled, 240 bits of data are read in, and the chip is non-selected. In case of common mode, controls the direction of data shift.

3.1.5. Data latch

In case of segment mode, latches the data on the data bus. The latched state of each LCD driver output pin is controlled by the control logic and the data latch control, 240 bits of data are read in 30 sets of 8 bits.

3.1.6. Test circuit

The circuit is for the test. During normal operation, it doesn't act.

3.1.7. Line latch/shift register

In case of segment mode, all 240 bits which have been read into the data latch are simultaneously latched on the falling edge of the LP signal, and output to the level shifter block. In case of common mode, shifts data from the data input pin on the falling edge of the LP signal.

3.1.8. Level shifter

The logic voltage signal is level-shifted to the LCD driver voltage level, and output to the driver block.

3.1.9. 4-level driver

Drives the LCD driver output pins from the line latch/shift register data, selecting one of 4 levels (V_0, V_{12}, V_{43}, V_5) based on the S/C, FR and $\overline{\text{DISPOFF}}$ signals.

3.2. Input/Output Circuits

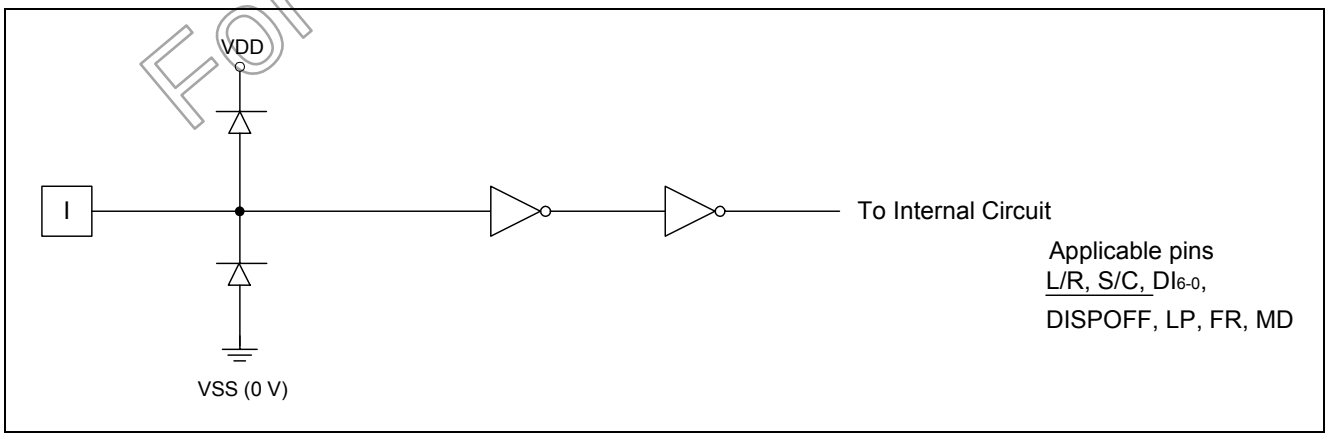


Figure1: Input Circuit (1)

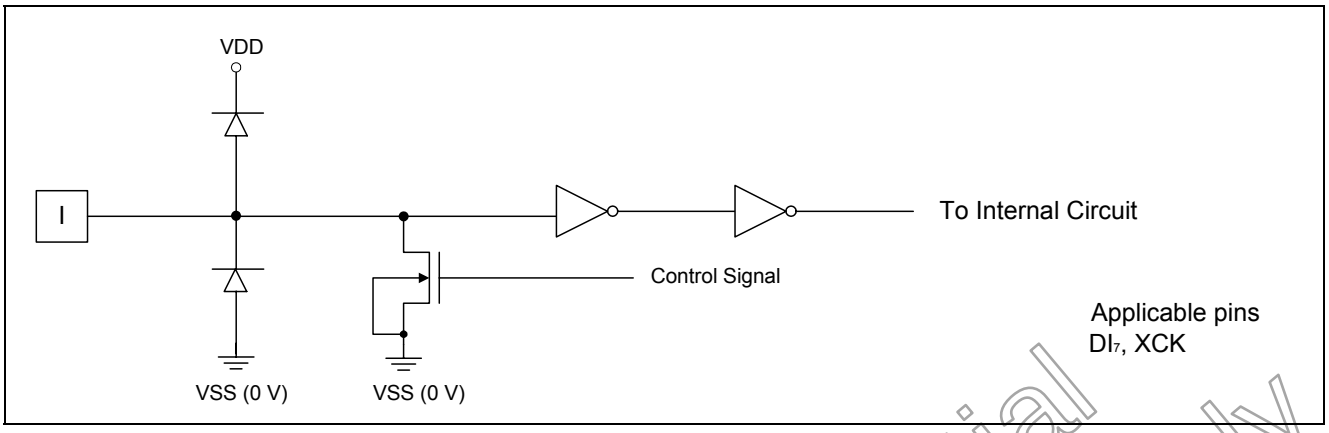


Figure2: Input Circuit (2)

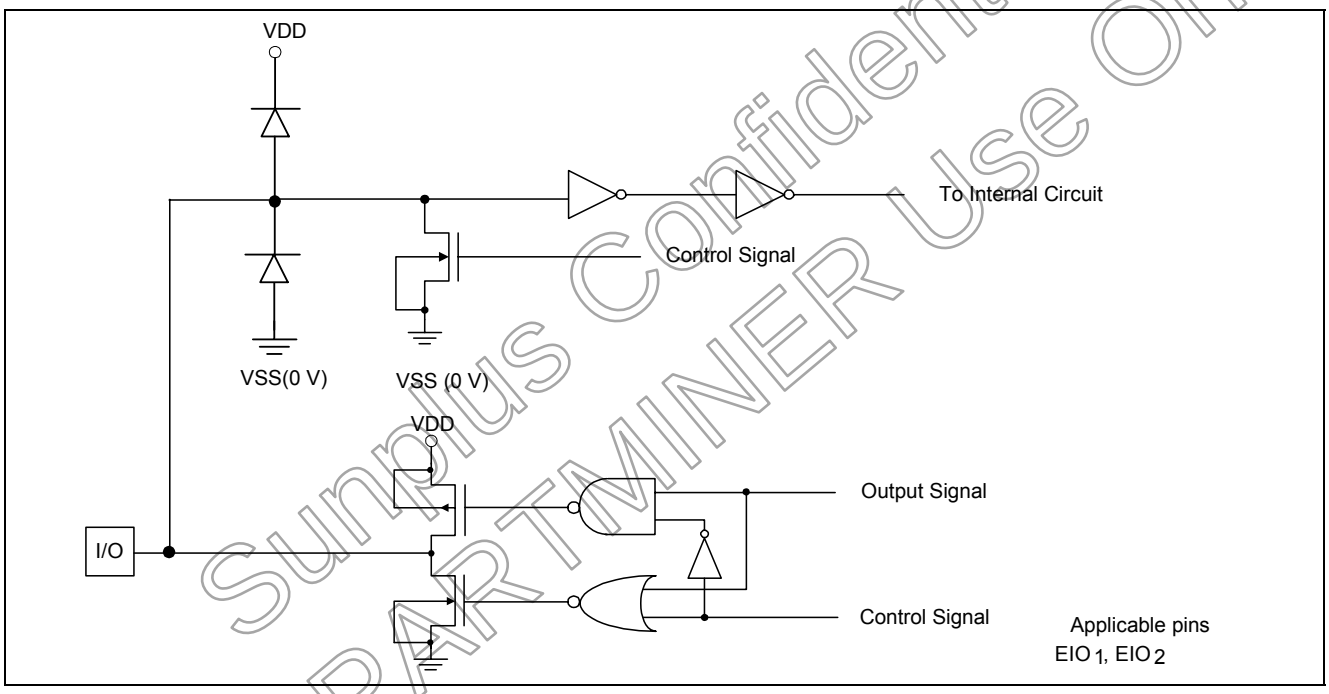


Figure3: Input/Output Circuit

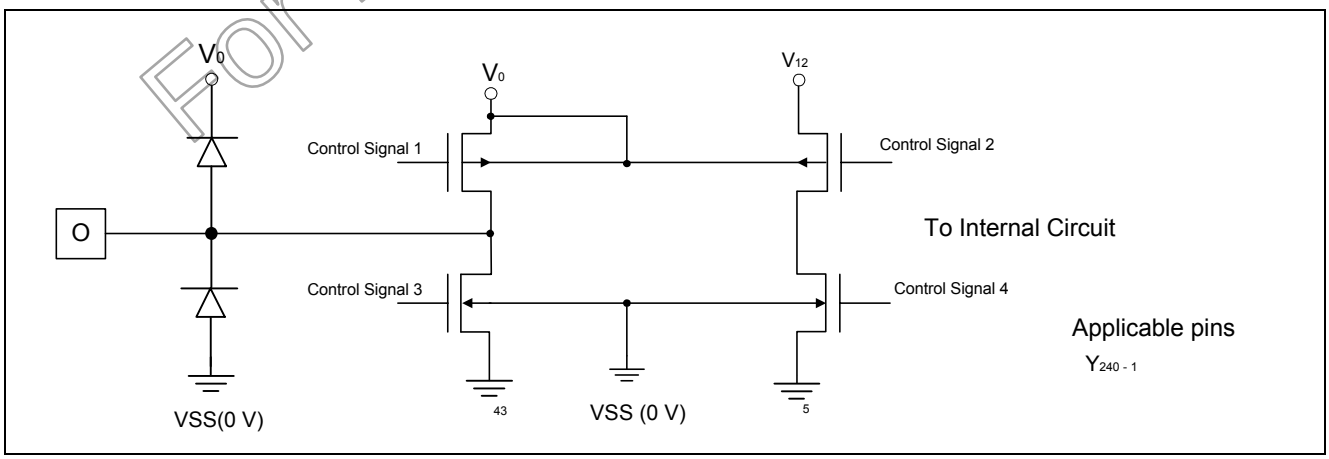
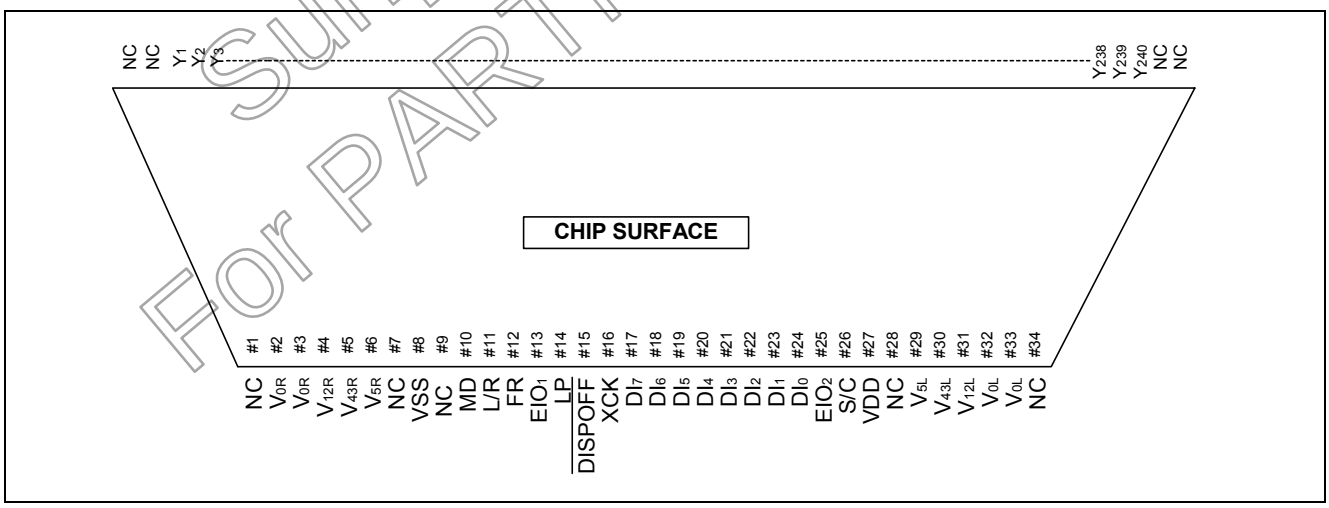


Figure4: LCD Drive Output Circuit

4. SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	Type	Description
Y_{240} - $_1$	-	O	LCD driver output
V_{0L} V_{0R}	#32, #33 #2, #3	-	Power supply for LCD driver
V_{12L}, V_{12R}	#31, #4	-	Power supply for LCD driver
V_{43L}, V_{43R}	#30, #5	-	Power supply for LCD driver
V_{5L}, V_{5R}	#29, #6	-	Power supply for LCD driver
L/R	#11	I	Input for selecting the reading direction of display data at segment mode/Input for selecting the shift direction of shift register at common mode
VDD	#27	-	Power supply for logic system (+2.5V to +5.5V)
S/C	#26	I	Segment mode/common mode selection
EIO_1 EIO_2	#13 #25	I/O	Input/output for chip selection at segment mode/Shift clock input/output for shift register at common mode
DI_{6} - $_0$	#18 - #24	I	Display data input for segment mode
DI7	#17	I	Display data input for segment mode/Dual mode data input at common mode
XCK	#16	I	Clock input for taking display data at segment mode
$\overline{\text{DISPOFF}}$	#15	I	Control input for output of non-select level
LP	#14	I	Latch pulse input for display data at segment mode/Shift clock input for shift register at common mode
FR	#12	I	AC-converting signal input for LCD driver waveform
MD	#10	I	Mode selection input
VSS	#8	-	Ground (0V)

4.1. PIN Connection



Note: Doesn't prescribe TCP outline.

5. FUNCATIONAL DESCRIPTIONS

5.1. PIN Functions

5.1.1. Segment mode

Mnemonic	Description
VDD	Logic system power supply pin connects to +2.5V to +5.5V
VSS	Ground pin connects to 0V
V_{0R}, V_{0L}, V_{12R}, V_{12L}, V_{43R}, V_{43L}, V_{5L}, V_{5R}	Bias Power supply pin for LCD driver voltage 1). Normally, the bias voltage used is set by a resistor divider. 2). Ensure that voltage are set such that VSS $V_5 < V_{43} < V_{12} < V_0$. 3). V_{iL} and V_{iR} ($I = 0, 12, 43, 5$) must connect to an external power supply, and supply regular voltage which is assigned by specification for each power pin. 4). In COG applications, even though VSS and V_5 have the same voltage level, the ITO layout of VSS and V_5 should not be shorted directly on the panel. That is, VSS and V_5 should have individual path and connect-pin.
DI_{7-0}	Input pins for display data 1). In 4-bit parallel input mode, input data into the 4 pins, DI_3 - DI_0. Connect DI_{7-4} to VSS or VDD. 2). In 8-bit parallel input mode, input data into the 8 pins, DI_7-DI_0. 3). Refer to "***5.3 Relationship between the Display Data and Driver Output PINs***" in Functional Operations.
XCK	Clock input pin for taking display data 1). Data is read at the falling edge of the clock pulse.
LP	Latch pulse input pin for display data 1). Data is latched at the falling edge of the clock pulse.
L/R	Input pin for selecting the reading direction of display data 1). When set to VSS level "L", data is read sequentially from Y_{240} to Y_1. 2). When set to VDD level "H", data is read sequentially from Y_1 to Y_{240}. 3). Refer to "***5.3 Relationship between the Display Data and Driver Output PINs***" in Functional Operations.
$\overline{DISPOFF}$	Control input pin for output non-select level 1). The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. 2). When set to VSS level "L", the LCD drive output pins (Y_{240-1}) are set to level V_5. 3). While set to "L", the contents of the line latch are reset, but the display data are read in the data latch regardless of the condition of $\overline{DISPOFF}$. When the $\overline{DISPOFF}$ function is canceled, the driver outputs non-select level (V_{12} or V_{43}), then outputs the contents of the data latch at the next falling edge of the LP. At that time, if $\overline{DISPOFF}$ removal time does not correspond to what is shown in AC characteristics, it can not output the reading data correctly. 4). Table of truth values is shown in "***5.2.1 Truth table***" in Function Operations.
S/C	Segment mode/common mode selection pin 1). When set to VDD level "H", segment mode is set.
FR	AC signal input pin for LCD driving waveform 1). The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls LCD drive circuit. 2). Normally, inputs a frame inversion signal. 3). The LCD driver output pin's output voltage level can be set using the line latch output signal and the FR signal. 4). Table of truth values is shown in "***5.2.1 Truth table***" in Function Operations.

Mnemonic	Description
MD	Mode selection pin 1). When set to VSS level “L”, 8-bit parallel input mode is set. 2). When set to VDD level “H”, 4-bit parallel input mode is set. 3). Refer to "***5.3 Relationship between the Display Data and Driver Output PINs***" in Functional Operations.
EIO_1, EIO_2	Input/output pins for chip selection 1). When L/R input is at VSS Level “L”, EIO_1 is set for output and EIO_2 is set for input. 2). When L/R input is at VDD Level “H”, EIO_1 is set for input and EIO_2 is set for output. 3). During output, set to “H” while LP XCK is “H” and after 240 bits of data have been read, set to “L” for one cycle (from falling edge to falling edge of XCK), after which it returns to “H”. 4). During input, the chip is selected while EI is set to “L” after the LP signal is input. The chip is non-selected after 240 bits of data have been read.
Y_{240-1}	LCD driver output pins 1). Corresponding directly to each bit of the shift register, one level (V_0, V_{12}, V_{43}, or V_5) is selected and output. 2). Table of truth values is shown in “***5.2.1 Truth table***” in Function Operations.

5.1.2. Common mode

Mnemonic	Description
VDD	Logic system power supply pin connects to +2.5V to +5.5V.
VSS	Ground pin connects to 0V
V_{0R}, V_{0L}, V_{12R}, V_{12L}, V_{43R}, V_{43L}, V_{5L}, V_{5R}	Bias Power supply pin for LCD driver voltage 1). Normally, the bias voltage used is set by a resistor divider. 2). Ensure that voltage are set such that VSS $V_5 < V_{43} < V_{12} < V_0$. 3). V_{iL} and V_{iR} ($_{I=0, 12, 43, 5}$) must connect to an external power supply, and supply regular voltage which is assigned by specification for each power pin.
LP	Shift clock pulse input pin for bi-directional shift register 1). Data is shifted at the falling edge of the clock pulse.
EIO_1	Shift data input/output pin for bi-directional shift register 1). Output pin when L/R is at VSS level “L”, input pin when L/R is at VDD level “H”. 2). When L/R = H, EIO_1 is used as input pin, it will be pull-down. 3). When L/R = L, EIO_1 is used as output pin, it won’t be pull-down. 4). Refer to "***5.3 Relationship between the Display Data and Driver Output PINs***" in Functional Operations.
L/R	Input pin for selecting the shift direction of bi-directional shift register 1). Data is shifted from Y_{240} to Y_1 when set to VSS to level “L”, and data is shifted from Y_1 to Y_{240} when set to VDD level “H”. 2). Refer to "***5.3 Relationship between the Display Data and Driver Output PINs***" in Functional Operations.
EIO_2	Shift data input/output pin for bi-directional shift register 1). Input pin when L/R is at VSS level “L”, output pin when L/R is at VDD level “H”. 2). When L/R = L, EIO_2 is used as input pin, it will be pull-down. 3). When L/R = H, EIO_2 is used as output pin, it won’t be pull-down. 4). Refer to "***5.3 Relationship between the Display Data and Driver Output PINs***" in Functional Operations.
S/C	Segment mode / common mode selection pin 1). When set to VSS level “L”, common mode is set.

Mnemonic	Description
FR	AC signal input for LCD driving waveform 1). The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls LCD drive circuit. 2). Normally, input a frame inversion signal. 3). The LCD driver output pin's output voltage level can be set using the shift register output signal and the FR signal. 4). Table of truth values is shown in "***5.2.1 Truth table***" in Functional Operations.
$\overline{DISPOFF}$	Control input pin for output non-select level 1). The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls LCD drive circuit. 2). When set to VSS level "L", the LCD drive output pins (Y_{240-1}) are set to level V_5. 3). While set to "L", the contents of the shift register are reset not reading data. When the $\overline{DISPOFF}$ function is canceled, the driver outputs non-select level (V_{12} or V_{43}), and the shift data is reading at the falling edge of the LP. At that time, if $\overline{DISPOFF}$ removal time does not correspond to what is shown in AC characteristics, the shift data is not reading correctly. 4). Table of truth values is shown in "***5.2.1 Truth table***" in Functional Operations.
MD	Mode selection pin 1). When set to VSS level "L", single mode operation is selected, when set to VDD level "H", dual mode operation is selected. 2). Refer to "***5.3 Relationship between the Display Data and Driver Output PINs***" in Functional Operations.
DI_{6-0}	Not used 1). Connect DI_{6-0} to VSS or VDD, avoiding floating.
XCK	Not used 1). XCK is pull-down in common mode, so connect to VSS or open.
DI_7	Dual mode data input pin 1). According to the data shift direction of the data shift register, data can be input starting from the 121st bit. When the chip is used as dual mode, DI_7 will be pull-down. When the chip is used as single mode, DI_7 won't be pull-down. 2). Refer to "***5.3 Relationship between the Display Data and Driver Output PINs***" in Functional Operations.
Y_{240-1}	LCD driver output pins 1). Corresponding directly to each bit of the shift register, one level (V_0, V_{12}, V_{43}, or V_5) is selected and output. 2). Table of truth values is shown in "***5.2.1 Truth table***" in Functional Operations.

5.2. Function Operations

5.2.1. Truth table

5.2.1.1. Segment mode

FR	Latch data	$\overline{DISPOFF}$	Driver output voltage level (Y_{240-1})
L	L	H	V_{43}
L	H	H	V_5
H	L	H	V_{12}
H	H	H	V_0
X	X	L	V_5

5.2.1.2. Common mode

FR	Latch data	$\overline{DISPOFF}$	Driver output voltage level (Y_{240-1})
L	L	H	V_{43}
L	H	H	V_0
H	L	H	V_{12}
H	H	H	V_5
X	X	L	V_5

Note1: VSS $V_5 < V_{43} < V_{12} < V_0$, L: VSS (0V), H: VDD (+2.5V to +5.5V), X: Don't care

Note2: "Don't care" should be fixed to "H" or "L", avoiding floating.
There are two kinds of power supply (logic level voltage and LCD drive voltage) for the LCD driver.
Supply regular voltage which is assigned by specification for each power pin.

5.3. Relationship between the Display Data and Driver Output PINs

5.3.1. Segment mode

5.3.1.1. 4-bit parallel mode

MD	L/R	EIO_1	EIO_2	Data Input	Figure of clock						
					60 Clock	59 Clock	58 Clock	..	3 Clock	2 Clock	1 Clock
H	L	Output	Input	DI_0	Y_1	Y_5	Y_9	..	Y_{229}	Y_{233}	Y_{237}
				DI_1	Y_2	Y_6	Y_{10}	..	Y_{230}	Y_{234}	Y_{238}
				DI_2	Y_3	Y_7	Y_{11}	..	Y_{231}	Y_{235}	Y_{239}
				DI_3	Y_4	Y_8	Y_{12}	..	Y_{232}	Y_{236}	Y_{240}
H	H	Input	Output	DI_0	Y_{240}	Y_{236}	Y_{232}	..	Y_{12}	Y_8	Y_4
				DI_1	Y_{239}	Y_{235}	Y_{231}	..	Y_{11}	Y_7	Y_3
				DI_2	Y_{238}	Y_{234}	Y_{230}	..	Y_{10}	Y_6	Y_2
				DI_3	Y_{237}	Y_{233}	Y_{229}	..	Y_9	Y_5	Y_1

5.3.1.2. 8-bit parallel mode

MD	L/R	EIO_1	EIO_2	Data Input	Figure of clock						
					30 Clock	29 Clock	28 Clock	..	3 Clock	2 Clock	1 Clock
L	L	Output	Input	DI_0	Y_1	Y_9	Y_{17}	..	Y_{217}	Y_{225}	Y_{233}
				DI_1	Y_2	Y_{10}	Y_{18}	..	Y_{218}	Y_{226}	Y_{234}
				DI_2	Y_3	Y_{11}	Y_{19}	..	Y_{219}	Y_{227}	Y_{235}
				DI_3	Y_4	Y_{12}	Y_{20}	..	Y_{220}	Y_{228}	Y_{236}
				DI_4	Y_5	Y_{13}	Y_{21}	..	Y_{221}	Y_{229}	Y_{237}
				DI_5	Y_6	Y_{14}	Y_{22}	..	Y_{222}	Y_{230}	Y_{238}
				DI_6	Y_7	Y_{15}	Y_{23}	..	Y_{223}	Y_{231}	Y_{239}
				DI_7	Y_8	Y_{16}	Y_{24}	..	Y_{224}	Y_{232}	Y_{240}
L	H	Input	Output	DI_0	Y_{240}	Y_{232}	Y_{224}	..	Y_{24}	Y_{16}	Y_8
				DI_1	Y_{239}	Y_{231}	Y_{223}	..	Y_{23}	Y_{15}	Y_7
				DI_2	Y_{238}	Y_{230}	Y_{222}	..	Y_{22}	Y_{14}	Y_6
				DI_3	Y_{237}	Y_{229}	Y_{221}	..	Y_{21}	Y_{13}	Y_5
				DI_4	Y_{236}	Y_{228}	Y_{220}	..	Y_{20}	Y_{12}	Y_4
				DI_5	Y_{235}	Y_{227}	Y_{219}	..	Y_{19}	Y_{11}	Y_3
				DI_6	Y_{234}	Y_{226}	Y_{218}	..	Y_{18}	Y_{10}	Y_2
				DI_7	Y_{233}	Y_{225}	Y_{217}	..	Y_{17}	Y_9	Y_1

5.3.2. Common mode

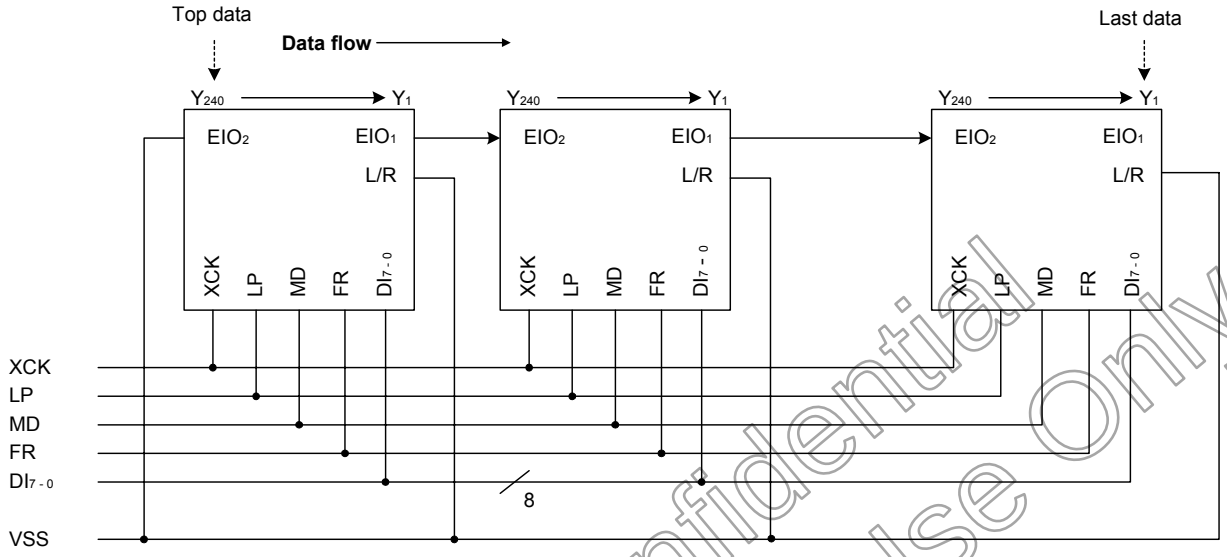
MD	L/R	Data transfer direction	EIO_1	EIO_2	DI_7
L (Single)	L(shift to left)	Y_{240} -> Y_1	Output	Input	X
	H(shift to right)	Y_1 -> Y_{240}	Input	Output	X
H (Dual)	L(shift to left)	Y_{240} -> Y_{121} Y_{120} -> Y_1	Output	Input	Input
	H(shift to right)	Y_1 -> Y_{120} Y_{121} -> Y_{240}	Input	Output	Input

Note1: L: VSS (0V), H: VDD (+2.5V to +5.5V), X: Don't care

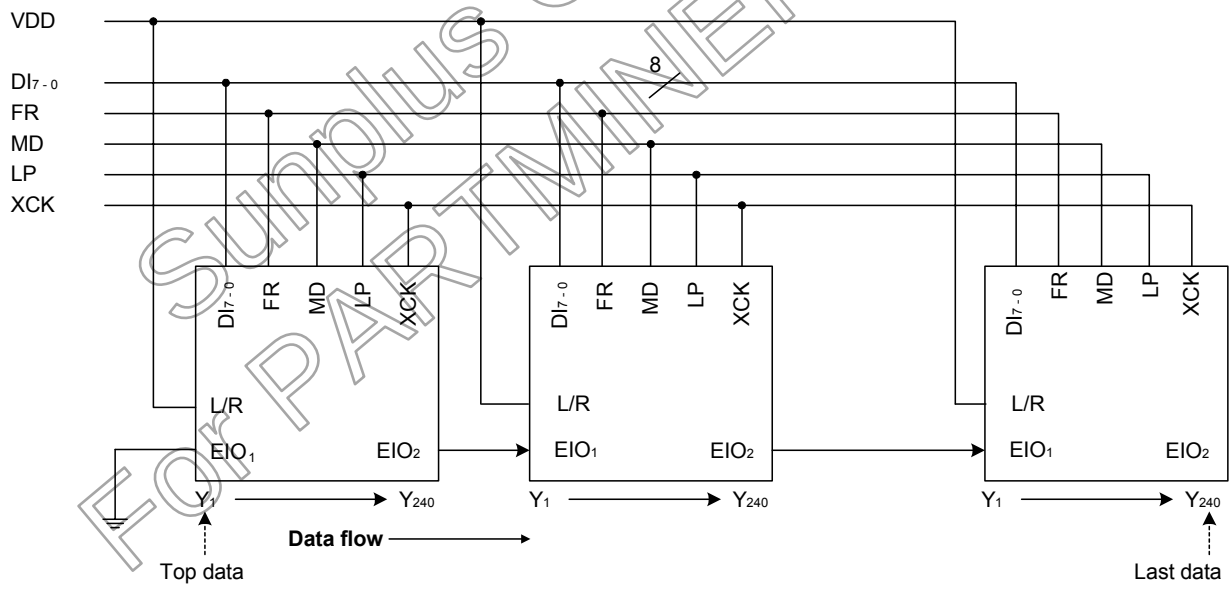
Note2: "Don't care" should be fixed to "H" or "L", avoiding floating.

5.3.3. Connection examples of plural segment drivers

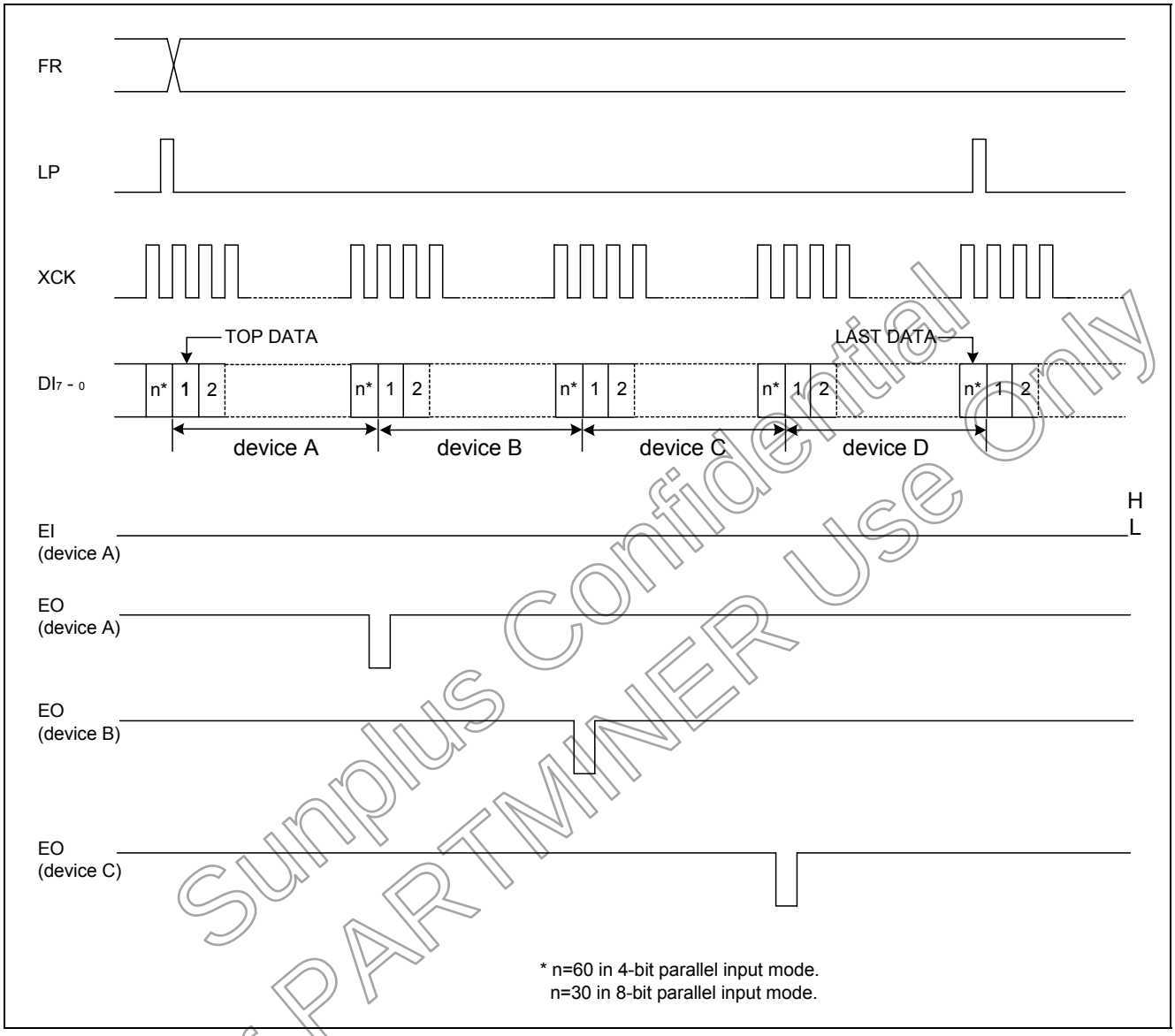
1). CASE OF L/R = "L"



2). CASE OF L/R = "H"

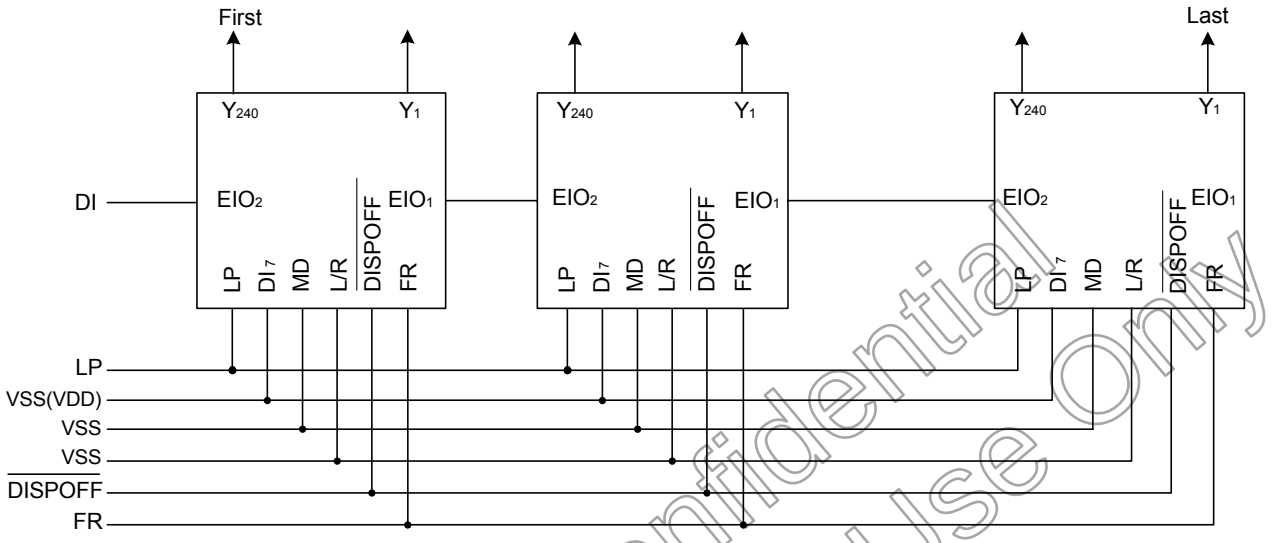


5.3.4. Timing chart of 4-device casecade connection of segment drivers

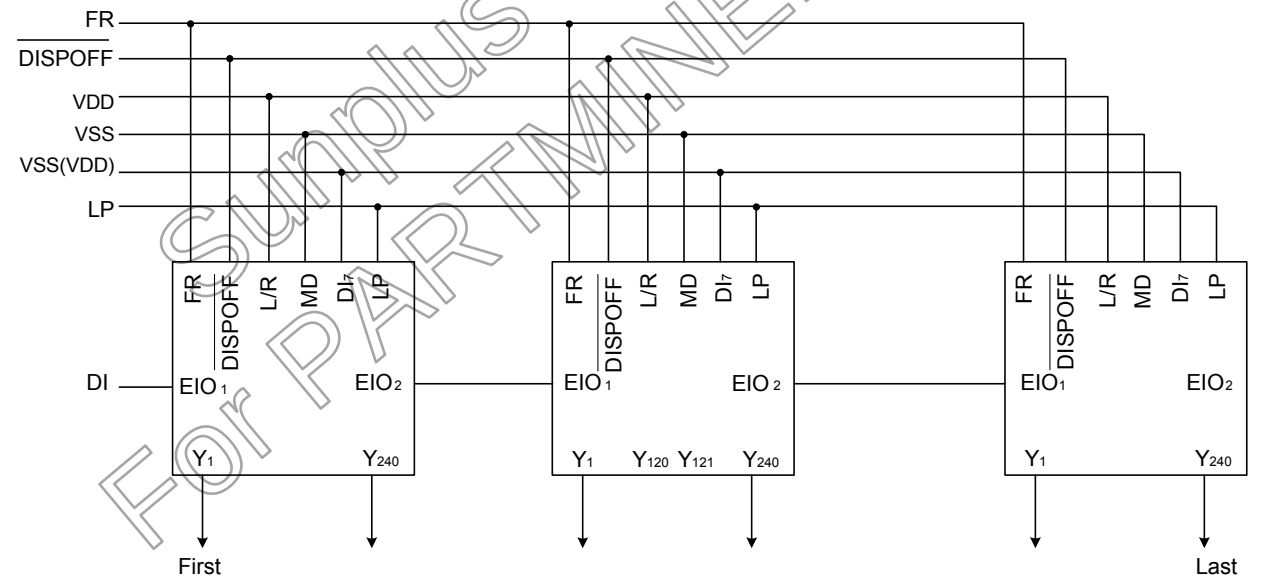


5.3.5. Connection examples for plural common drivers

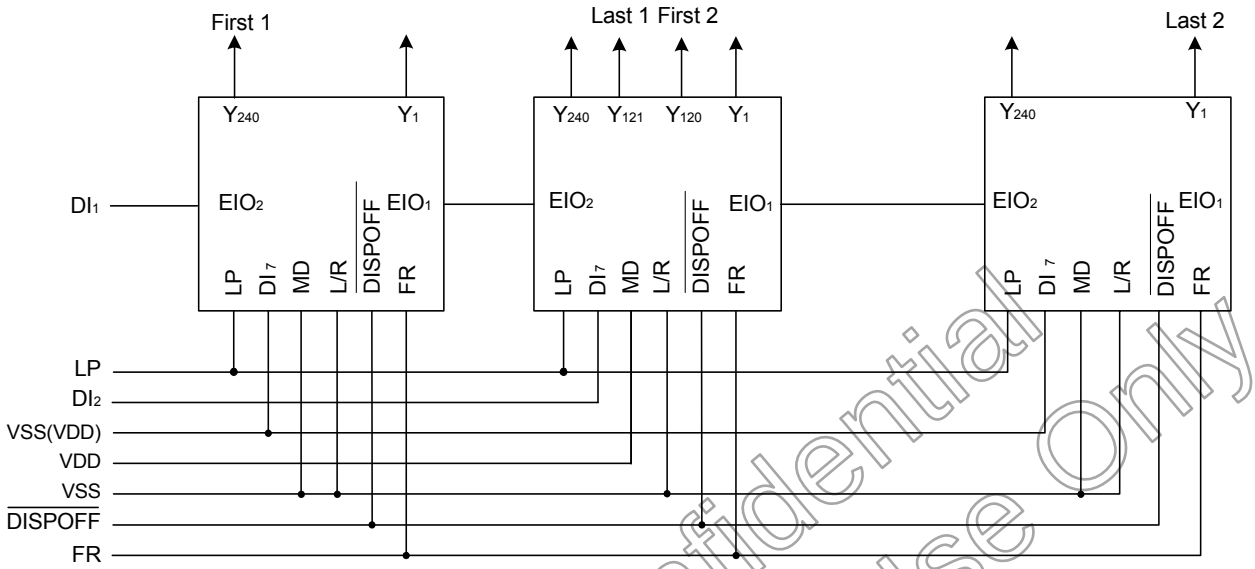
1). Single MODE (L/R = "L")



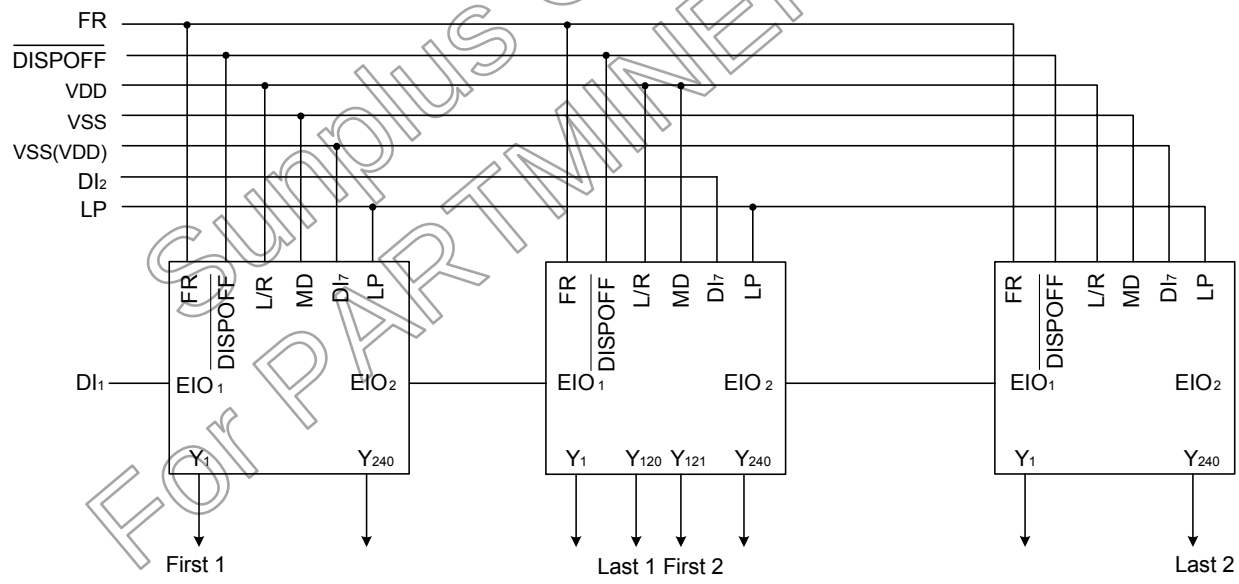
2). Single Mode (L/R = "H")



3). Dual MODE (L/R = "L")



4). Dual MODE (L/R = "H")



5.4. Precautions

5.4.1. Precaution when connecting or disconnecting the power

This LSI has a high-voltage LCD driver, so it may be permanently damaged by a high current which may flow if a voltage is supplied to the LCD driver power supply while the logic system power supply is floating.

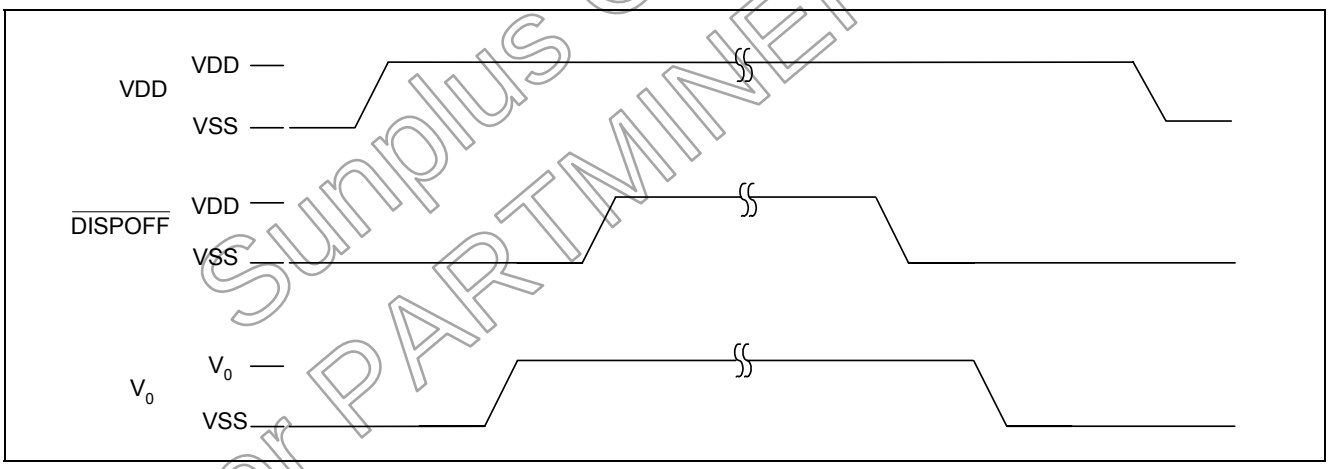
The detail is as follows.

1). When connecting the power supply, connect the LCD drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD driver power.

2). We recommend you connecting the serial resistor (50~100Ω) or fuse to the LCD drive power V_0 of the system as a current limited. And set up a suitable value of the resistor in consideration of LCD display grade.

And when connecting the logic power supply, the logic condition of this LSI inside is insecurity. Therefore connect the LCD driver power supply after resetting logic condition of this LSI inside on $\overline{\text{DISPOFF}}$ function. After that, cancel the $\overline{\text{DISPOFF}}$ function after the LCD driver power supply has become stable. Furthermore, when disconnecting the power, set the LCD drive output pins to level V_5 on $\overline{\text{DISPOFF}}$ function. After that, disconnect the logic system power after disconnecting the LCD drive power.

When connecting the power supply, follow the recommended sequence shown here.



6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Applicable Pins	Ratings	Unit
Supply voltage (1)	VDD	T_A = 25 Referenced to VSS(0V)	VDD	-0.3 to +6.5	V
Supply voltage (2)	V_0		V_{0L}, V_{0R}	-0.3 to +30	V
	V_{12}		V_{12L}, V_{12R}	-0.3 to V0+0.3	V
	V_{43}		V_{43L}, V_{43R}	-0.3 to V0+0.3	V
	V_5		V_{5L}, V_{5R}	-0.3 to V0+0.3	V
Input voltage	V_I		DI_{7-0}, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, $\overline{DISPOFF}$	-0.3 to VDD+0.3	V
Storage temperature	T_{STG}	-	-	-45 to +125	

Note1: T_A = +25

Note2: The maximum applicable voltage on any pin with respect to VSS (0V).

Note3: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

6.2. Recommended Operating Conditions

Parameter	Symbol	Conditions	Applicable Pins	Min.	Typ.	Max.	Unit
Supply voltage (1)	VDD	Referenced to VSS (0V)	VDD	+2.5	-	+5.5	V
Supply voltage (2)	V_0		V_{0L}, V_{0R}	+15	-	+30	V
Operating temperature	T_{OPR}	-	-	-20	-	+85	

Note1: The applicable voltage on any pin with respect to VSS (0V).

Note2: Ensure that voltage are set such that VSS V_5 V_{43} V_{12} V_0.

6.3. DC Characteristics

6.3.1. Segment mode

(VSS = V_5 = 0V, VDD = +2.5V to +5.5V, V_0 = +15V to +30V, T_A = +25)

Parameter	Symbol	Conditions	Applicable Pins	Min.	Typ.	Max.	Unit
Input voltage	V_{IH}	-	DI_{7-0}, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, $\overline{DISPOFF}$	0.8VDD	-	-	V
	V_{IL}	-		-	-	0.2VDD	V
Output voltage	V_{OH}	I_{OH} = -0.4mA	EIO_1, EIO_2	VDD-0.4	-	-	V
	V_{OL}	I_{OL} = +0.4mA		-	-	+0.4	V
Input leakage current	I_{LIH}	V_I = VDD	DI_{7-0}, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, $\overline{DISPOFF}$	-	-	+10	μA
	I_{LIL}	V_I = VSS		-	-	-10	μA
Output resistance	R_{ON}	| V_{ON}| = 0.5V, V_0 = +30V	Y_{240-1}	-	1.5	2.0	KΩ
		| V_{ON}| = 0.5V, V_0 = +20V		-	2.0	2.5	KΩ
Stand-by current	I_{STB}	*1	VSS	-	-	75	μA
Supply current (1) (Non-selection)	I_{DD1}	*2	VDD	-	-	2.0	mA
Supply current (2) (Selection)	I_{DD2}	*3	VDD	-	-	12	mA
Supply current (3)	I_0	*4	V_{0L}, V_{0R}	-	-	1.5	mA

Note1: VDD = +5.0V, V_0 = +30V, V_I = VSS

Note2: VDD = +5.0V, V_0 = +30V, f_{XCK} = 20MHz, No-load, E_I = VDD. The input data is turned over by data taking clock (4-bit parallel input mode)

Note3: VDD = +5.0V, V_0 = +30V, f_{XCK} = 20MHz, No-load, E_I = VSS. The input data is turned over by data taking clock (4-bit parallel input mode)

Note4: VDD = +5.0V, V_0 = +30V, f_{XCK} = 20MHz, f_{LP} = 41.6KHz, f_{FR} = 80Hz, no-load. The input data is turned over by data taking clock (4-bit parallel input mode)

6.3.2. Common mode

(VSS = V_5 = 0V, VDD = +2.5V to +5.5V, V_0 = +15V to +30V, T_A = +25)

Parameter	Symbol	Conditions	Applicable Pins	Min.	Typ.	Max.	Unit
Input voltage	V_{IH}	-	DI_{7-0}, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, $\overline{DISPOFF}$	0.8VDD	-	-	V
	V_{IL}	-		-	-	0.2VDD	V
Output voltage	V_{OH}	I_{OH} = -0.4mA	EIO_1, EIO_2	VDD-0.4	-	-	V
	V_{OL}	I_{OL} = +0.4mA		-	-	+0.4	V
Input leakage current	I_{LIH}	V_I = VDD	DI_{7-0}, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, $\overline{DISPOFF}$	-	-	+10	μA
	I_{LIL}	V_I = VSS		-	-	-10	μA
Output resistance	R_{ON}	| V_{ON}| = 0.5V, V_0 = +30V	Y_{240-1}		1.5	2.0	KΩ
		| V_{ON}| = 0.5V, V_0 = +20V		-	2.0	2.5	KΩ
Input pull-down current	I_{PD}	V_I = VDD	XCK, EIO_1, EIO_2, DI_7		-	100	μA
Stand-by current	I_{STB}	*1	VSS	-	-	75	μA
Supply current (1)	I_{DD}	*2	VDD	-	-	120	μA
Supply current (2)	I_0	*2	V_{0L}, V_{0R}	-	-	240	μA

Note1: VDD = +5.0V, V_0 = +30V, V_I = VSS

Note2: VDD = +5.0V, V_0 = +30V, f_{LP} = 41.6KHz, f_{FR} = 80Hz in case of 1/480 duty operation, no-load.

6.4. AC Characteristics

6.4.1. Segment mode 1

(VSS = V_5 = 0V, VDD = +4.5V to + +5.5V, V_0 = +15V to +30V, T_A = +25)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Shift clock period *1	T_{WCK}	T_R, T_F 10ns	50	-	-	ns
Shift clock “H” pulse width	T_{WCKH}	-	15	-	-	ns
Shift clock “L” pulse width	T_{WCKL}	-	15	-	-	ns
Data setup time	T_{DS}	-	10	-	-	ns
Data hold time	T_{DH}	-	12	-	-	ns
Latch pulse “H” pulse width	T_{WLPH}	-	15	-	-	ns
Shift clock rise to latch pulse rise time	T_{LD}	-	0	-	-	ns
Shift clock fall to latch pulse fall time	T_{SL}	-	30	-	-	ns
Latch pulse rise to shift clock rise time	T_{LS}	-	25	-	-	ns
Latch pulse fall to shift clock fall time	T_{LH}	-	25	-	-	ns
Input signal rise time *2	T_R	-	-	-	50	ns
Input signal fall time *2	T_F	-	-	-	50	ns
Enable setup time	T_S	-	10	-	-	ns
$\overline{DISPOFF}$ removal time	T_{SD}	-	100	-	-	ns
$\overline{DISPOFF}$ “L” pulse width	T_{WDL}	-	1.2	-	-	μs
Output delay time (1)	T_D	C_L = 15pF	-	-	30	ns
Output delay time (2)	T_{PD1}, T_{PD2}	C_L = 15pF	-	-	1.2	μs
Output delay time (3)	T_{PD3}	C_L = 15pF	-	-	1.2	μs

Note1: Take the cascade connection into consideration.

Note2: (T_{WCK} - T_{WCKH} - T_{WCKL}) / 2 is maximum in the case of high speed operation.

6.4.2. Segment mode 2

(VSS = V_5 = 0V, VDD = +3.0V to +4.5V, V_0 = +15V to +30V, T_A = +25)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Shift clock period *1	T_{WCK}	T_R, T_F 10ns	66	-	-	ns
Shift clock “H” pulse width	T_{WCKH}	-	23	-	-	ns
Shift clock “L” pulse width	T_{WCKL}	-	23	-	-	ns
Data setup time	T_{DS}	-	15	-	-	ns
Data hold time	T_{DH}	-	23	-	-	ns
Latch pulse “H” pulse width	T_{WLPH}	-	30	-	-	ns
Shift clock rise to latch pulse rise time	T_{LD}	-	0	-	-	ns
Shift clock fall to latch pulse fall time	T_{SL}	-	50	-	-	ns
Latch pulse rise to shift clock rise time	T_{LS}	-	30	-	-	ns
Latch pulse fall to shift clock fall time	T_{LH}	-	30	-	-	ns
Input signal rise time *2	T_R	-	-	-	50	ns
Input signal fall time *2	T_F	-	-	-	50	ns
Enable setup time	T_S	-	15	-	-	ns
$\overline{\text{DISPOFF}}$ removal time	T_{SD}	-	100	-	-	ns
$\overline{\text{DISPOFF}}$ “L” pulse width	T_{WDL}	-	1.2	-	-	µs
Output delay time (1)	T_D	C_L = 15pF	-	-	41	ns
Output delay time (2)	T_{PD1}, T_{PD2}	C_L = 15pF	-	-	1.2	µs
Output delay time (3)	T_{PD3}	C_L = 15pF	-	-	1.2	µs

Note1: Take the cascade connection into consideration.

Note2: (T_{WCK} - T_{WCKH} - T_{WCKL}) / 2 is maximum in the case of high speed operation.

6.4.3. Segment mode 3

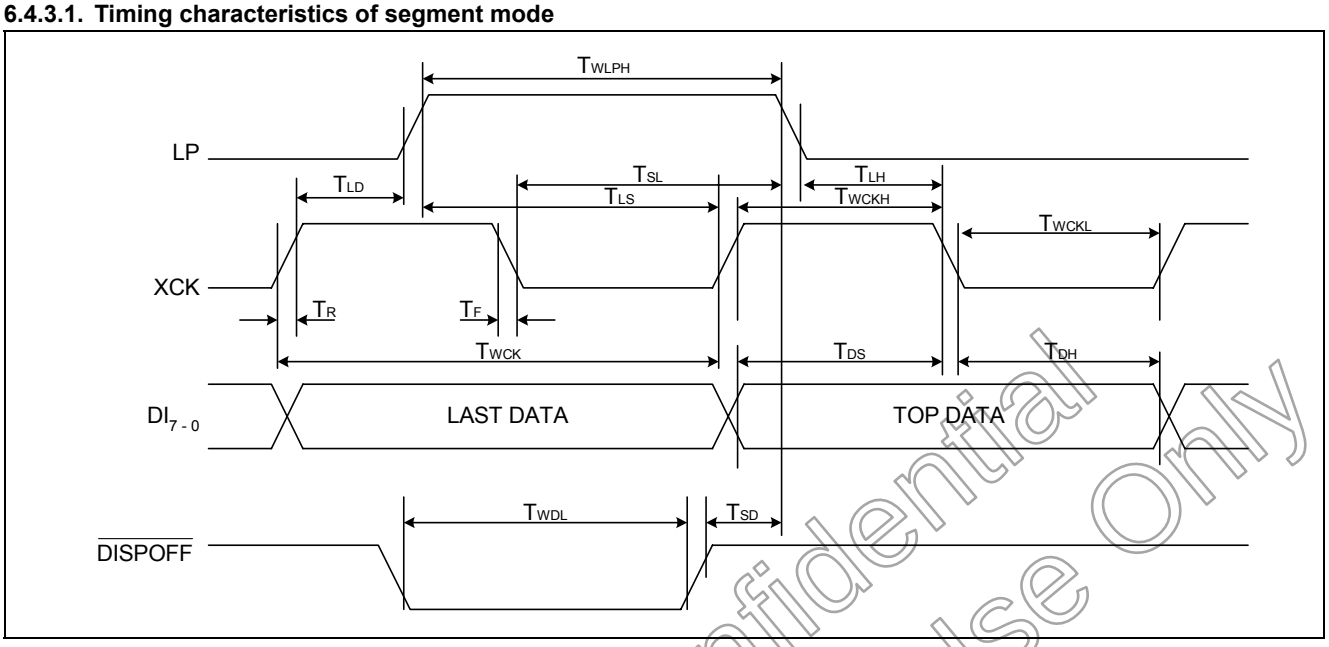
(VSS = V_5 = 0V, VDD = +2.5V to +3.0V, V_0 = +15V to +30V, T_A = +25)

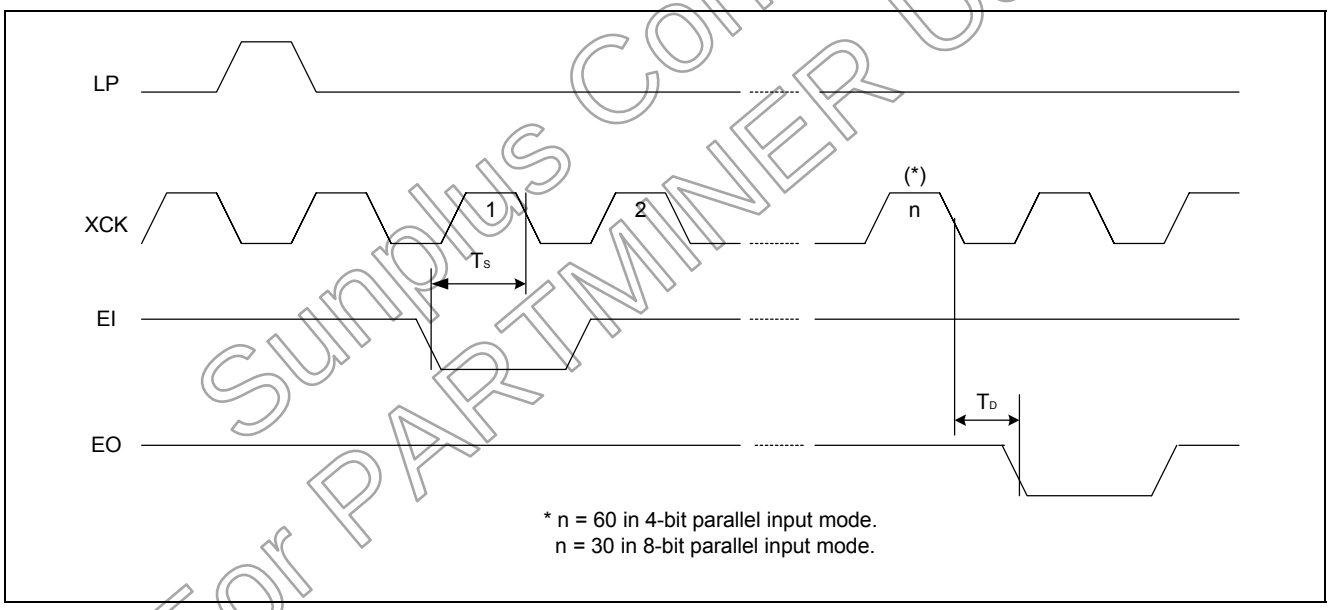
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Shift clock period	T_{WCK}	T_R, T_F 10ns	82	-	-	ns
Shift clock “H” pulse width	T_{WCKH}	-	28	-	-	ns
Shift clock “L” pulse width	T_{WCKL}	-	28	-	-	ns
Data setup time	T_{DS}	-	20	-	-	ns
Data hold time	T_{DH}	-	23	-	-	ns
Latch pulse “H” pulse width	T_{WLPH}	-	30	-	-	ns
Shift clock rise to latch pulse rise time	T_{LD}	-	0	-	-	ns
Shift clock fall to latch pulse fall time	T_{SL}	-	65	-	-	ns
Latch pulse rise to shift clock rise time	T_{LS}	-	30	-	-	ns
Latch pulse fall to shift clock fall time	T_{LH}	-	30	-	-	ns
Input signal rise time	T_R	-	-	-	50	ns
Input signal fall time	T_F	-	-	-	50	ns
Enable setup time	T_S	-	15	-	-	ns
$\overline{\text{DISPOFF}}$ removal time	T_{SD}	-	100	-	-	ns
$\overline{\text{DISPOFF}}$ “L” pulse width	T_{WDL}	-	1.2	-	-	µs
Output delay time (1)	T_D	C_L = 15pF	-	-	57	ns
Output delay time (2)	T_{PD1}, T_{PD2}	C_L = 15pF	-	-	1.2	µs
Output delay time (3)	T_{PD3}	C_L = 15pF	-	-	1.2	µs

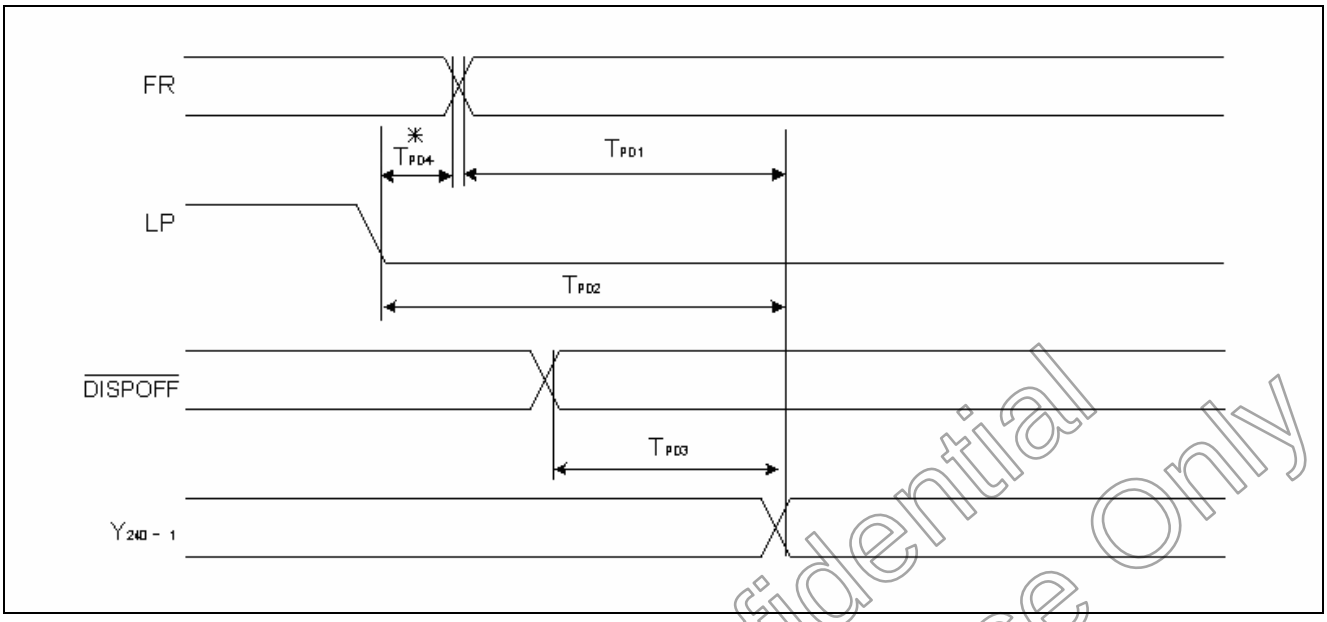
Note1: Take the cascade connection into consideration.

Note2: (T_{WCK} - T_{WCKH} - T_{WCKL}) / 2 is maximum in the case of high speed operation.

6.4.3.1. Timing characteristics of segment mode







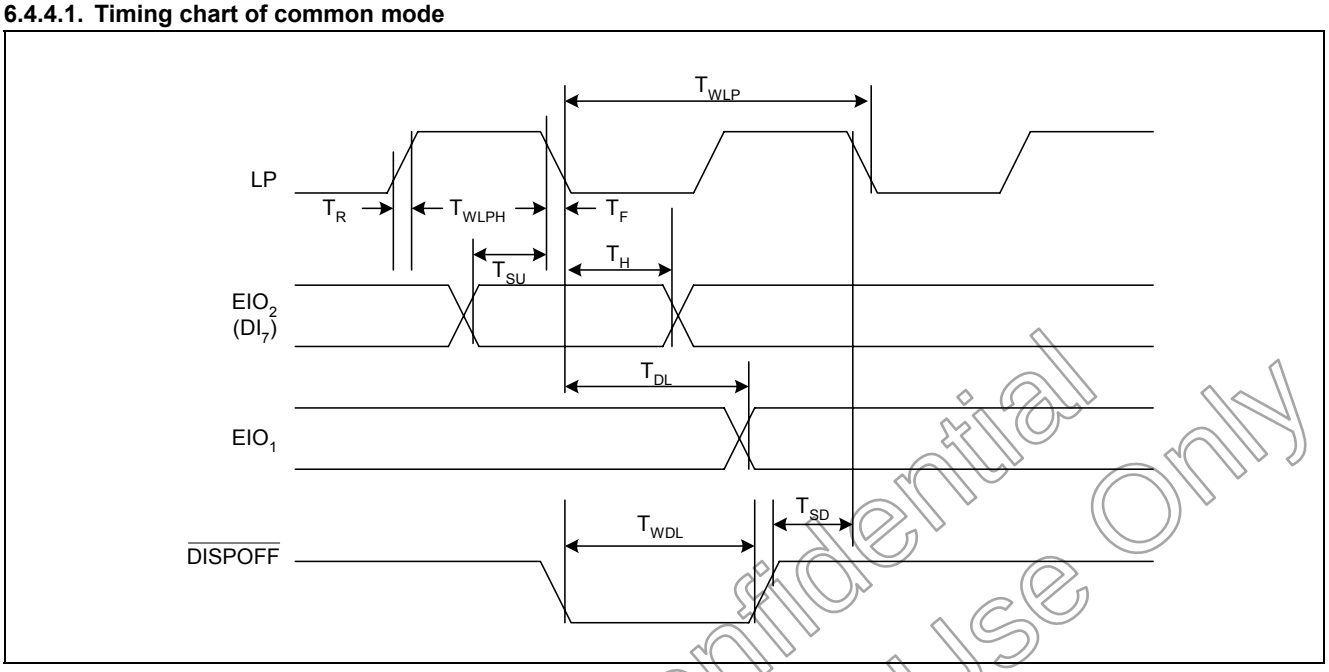
***Note:** Recommand TPD4 > 10ns for COG application which reduce power noise.

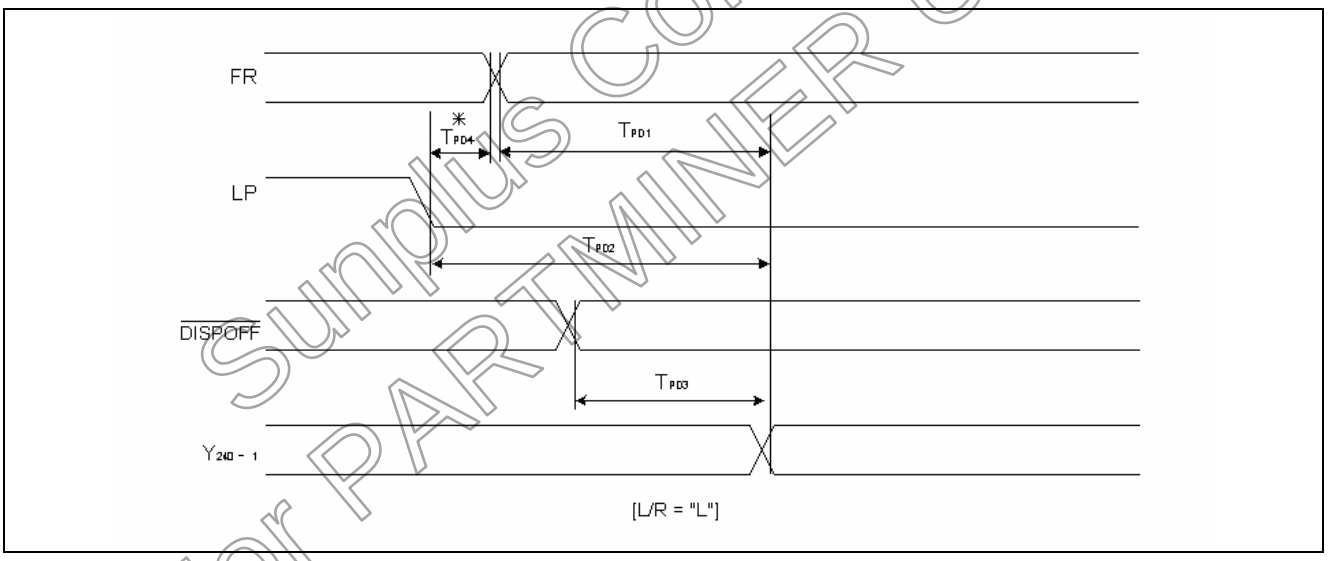
6.4.4. Common mode

(VSS = V_5 = 0V, VDD = +2.5V to +5.5V, V_0 = +15V to +30V, T_A = +25)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Shift clock period	T_{WLP}	T_R, T_F 20ns	250	-	-	ns
Shift "H" pulse width	T_{WLPH}	VDD = +5.0V ± 10%	15	-	-	ns
		VDD = +2.5V ~ +4.5V	30	-	-	ns
Data setup time	T_{SU}	-	30	-	-	ns
Data hold time	T_H	-	50	-	-	ns
Input signal rise time	T_R	-	-	-	50	ns
Input signal fall time	T_F	-	-	-	50	ns
$\overline{\text{DISPOFF}}$ removal time	T_{SD}	-	100	-	-	ns
$\overline{\text{DISPOFF}}$ "L" pulse width	T_{WDL}	-	1.2	-	-	µs
Output delay time (1)	T_{DL}	C_L = 15pF	-	-	200	ns
Output delay time (2)	T_{PD1}, T_{PD2}	C_L = 15pF	-	-	1.2	µs
Output delay time (3)	T_{PD3}	C_L = 15pF	-	-	1.2	µs

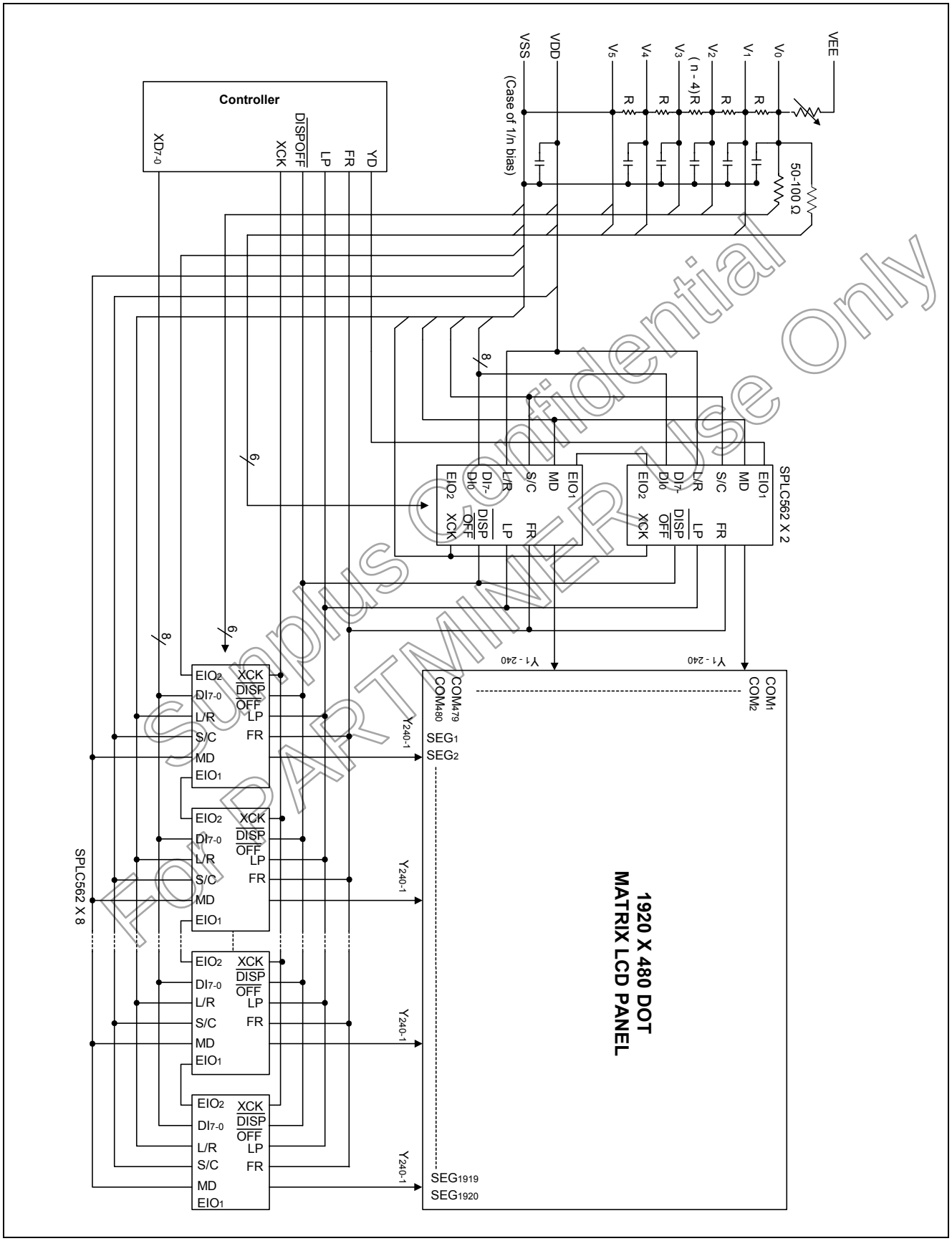
6.4.4.1. Timing chart of common mode





***Note :** Recommand T_{PD4} > 10ns for COG application which reduce power noise.

7. APPLICATION CIRCUIT



8. PACKAGE/PAD LOCATIONS

8.1. PAD Assignment and Locations

Please contact Sunplus sales representatives for more information.

8.2. Ordering Information

Product Number	Package Type
SPLC562C - C	Chip form with Bump
SPLC562C - P*	Package form - TCP

Note: *The TCP's external shape is customized. To order your TCP's external shape, please contact SUNPLUS salesperson.

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10. REVISION HISTORY

Date	Revision #	Description	Page
SEP. 17, 2004	1.2	Correct Timing diagram and Note	21, 22
DEC. 09, 2003	1.1	Remove "*8. PACKAGE/PAD LOCATIONS*"	24
FEB. 12, 2003	1.0	1. Remove "*Preliminary*" 2. Correct Pad pitch in "*8.1 PAD Assignment*"	 24
SEP. 03, 2002	0.2	1. Correct type error 2. Modify: Pad pitch: 50 -> 55 in "*8.1 PAD Assignment*" and "*8.3 COG Align Key Coordinate*"	1 24
APR. 23, 2002	0.1	Original	