SPECIFICATION FOR LCD MODULE

Model No. TM128160GKFWG

Prepared by:	**Date:**
Checked by :	**Date:**
Verified by :	**Date:**
Approved by:	**Date:**

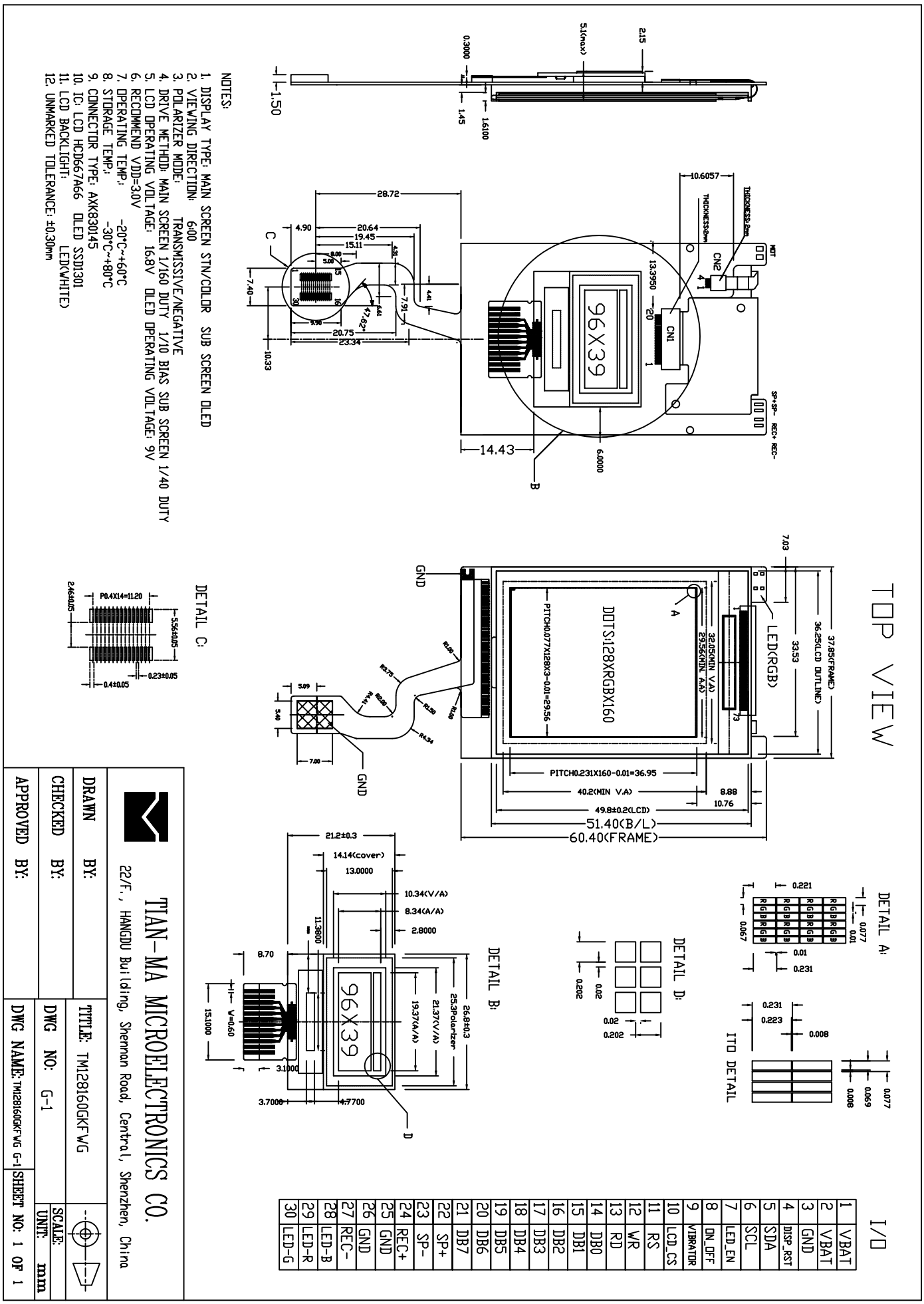
TIANMA MICROELECTRONICS CO., LTD

Ver. 1.0

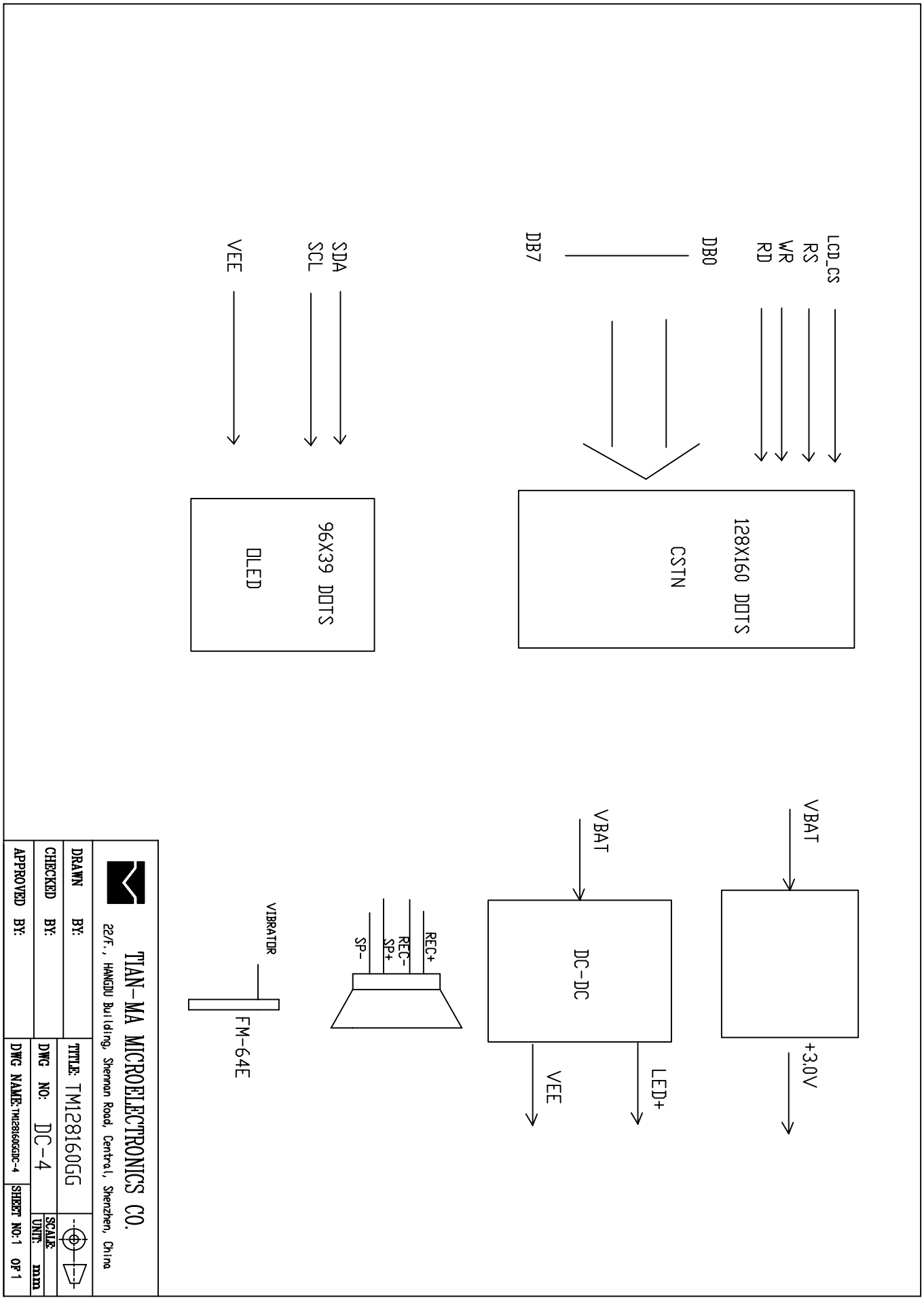
1 General Specifications:

ITEM	CONTENTS		UNIT
	MAIN LCD	SUB LCD	
LCD TYPE	COLOR STN	OLED	---
LCD DUTY	1/160	1/40	---
LCD BIAS	1/10	---	---
VIEWING DIRECTION	6:00	---	O'CLOCK
GLASS AREA(WXH)	36.25X49.80	26.8X21.2	MM
VIEWING AREA(WXH)	32.05X40.20	21.374X10.338	MM
ACTIVE AREA(WXH)	29.56X36.95	19.374X8.338	MM
NUMBER OF DOTS	128(R+G+B)X160	96X32(B)+96X7(Y)	MM
DOTE SIZE(WXH)	0.221X0.221	0.182X0.182	MM
DOT PITCH(WXH)	0.231X0.231	0.202X0.202	MM
CONTROLLER	HD66766	SSD1301	---
VBAT	3.6~4.5V(TYP)		
LCD OPERATING VOLTAGE	16.8	9	V
OUTLINE DIMENSIONS	REFER TO OUTLINE DRAWING ON NEXT PAGE		
BACKLIGHT	LED(WHITE)	---	---
OPERATING TEMPERAT	-20---+70℃	-20---+60℃	---
STORAGE TEMPERATURE	-30---+80℃	-40---+85℃	---
WEIGHT	TBD		---
DATA TRANSFER	8 BIT PARALLEL	I^2C	---
POLARIZER MODE	TRANSMISSIVE /NEGATIVE	---	---

2 OUTLINE


NOTES:
1. DISPLAY TYPE: MAIN SCREEN STN/COLOR SUB SCREEN OLED
2. VIEWING DIRECTION: 6:00
3. POLARIZER MODE: TRANSMISSIVE/NEGATIVE
4. DRIVE METHOD: MAIN SCREEN 1/160 DUTY 1/10 BIAS SUB SCREEN 1/40 DUTY
5. LCD OPERATING VOLTAGE: 16.8V OLED OPERATING VOLTAGE: 9V
6. RECOMMEND VDD=3.0V
7. OPERATING TEMP.: -20°C~+60°C
8. STORAGE TEMP.: -30°C~+80°C
9. CONNECTOR TYPE: AXK830145
10. IC: LCD HCD667A66 OLED SSD1301
11. LCD BACKLIGHT: LED(WHITE)
12. UNMARKED TOLERANCE: ±0.30mm
TOP VIEW
DOTS:128XRGBX160
LED(RGB)
DETAIL A:
DETAIL B:
DETAIL C:
DETAIL D:
ITO DETAIL
I/O
1 VBAT
2 VBAT
3 GND
4 DISP_RST
5 SDA
6 SCL
7 LED_EN
8 DIN_OFF
9 VIBRATOR
10 LCD_CS
11 RS
12 WR
13 RD
14 DB0
15 DB1
16 DB2
17 DB3
18 DB4
19 DB5
20 DB6
21 DB7
22 SP+
23 SP-
24 REC+
25 GND
26 GND
27 REC-
28 LED-B
29 LED-R
30 LED-G
TIAN-MA MICROELECTRONICS CO.
22/F., HANGDU Building, Shennan Road, Central, Shenzhen, China
DRAWN BY:
CHECKED BY:
APPROVED BY:
TITLE: TM128160GKFWG
DWG NO: G-1
DWG NAME: TM128160GKFWG G-1
SCALE:
UNIT: mm
SHEET NO: 1 OF 1

3. Circuit Block Diagram



4 Absolute Maximum Ratings(Ta=25℃)

MAIN_LCD

Item	Symbol	Min.	Max.	Unit	Remark
Power Supply Voltage	VDD－VSS	-0.3	+4.6	V	
LCD Driving Voltage	VLCD	-0.3	+20.0		
Operating Temperature Range	TOP	-20	+70	℃	No Condensation
Storage Temperature Range	TST	-30	+80		

OLED

ITEM	MIN	MAX	UNIT	COMMENT
Supply Voltage (VDD)	-0.3	4	V	Ta=25℃
Supply Voltage (VEE)	0	VDD – 16.5	V	Ta=25℃
Input Voltage (Vin)	Vss - 0.3	Vdd + 0.3	V	Ta=25℃
Operating Temp.	-20	60	℃	
Storage Temp	-40	85	℃	

5. Electrical Specifications and Instruction Code (Vss=0v, Ta=25℃)

5.1 Electrical characteristics

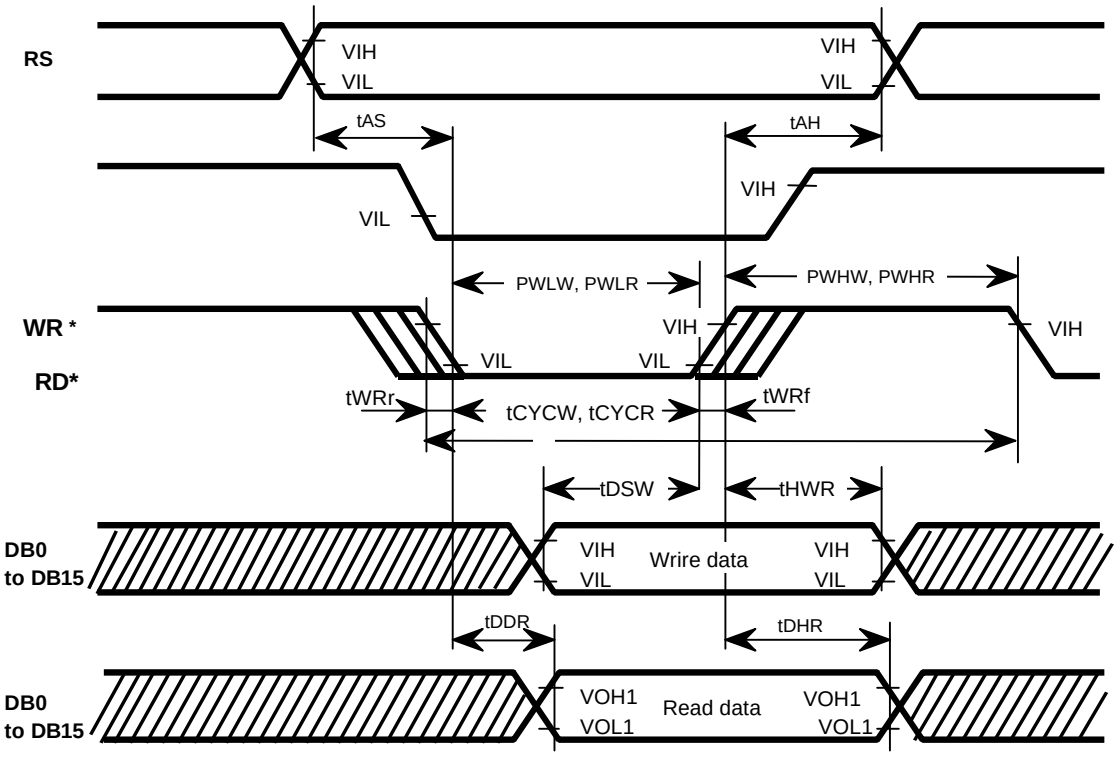
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply voltage for logic	VBAT	---	3.2	3.8	12	V
Supply voltage for main LCD (LCD DRIVE)	VLCD1	---	---	16.8	---	V
Supply voltage for OLED (OLED DRIVE)	VLCD2	---	---	9	---	V
Input voltage'H' Level(V_{IH})	MAIN	VDD=3.0V	0.8VDD	---	VDD	V
	SUB	VDD=3.0V	0.8VDD	---	VDD	
Input voltage'L' Level(V_{IL})	MAIN	VDD=3.0V	0	---	0.2VDD	V
	SUB	VDD=3.0V	0		0.2VDD	
Supply current (Logic) I_{DD}	MAIN	VDD=3.0V	---	---	2.5	mA
	SUB	VDD=3.0V	---	0.5	1	
Supply Voltage (LED)	V_{LED}	---	---	9.9	---	V
Supply current (LED)	I_{LED}	---		15.0	20.0	mA

5.2 Interface Signals

PinNo.	Symbo l	Level	Description
1	VBAT	H	Power supply
2	VBAT	H	Power supply
3	GND	L	GROUND
4	DISP—RST	H/L	Reset pin L: active
5	SDA	H/L	I^2c-BUS Data signal
6	SCL	H/L	I^2c-BUS Clock signal
7	LED-EN	H/L	Led enable pin L:active
8	ON-OFF	H/L	VDD on or off. H: active
9	VIBRATOR	H/L	VIBRATOR control pin.
10	LCD-CS	H/L	LCD Chip select pin
11	RS	H/L	Index select/Data command select
12	WR	H/L	Write operation(8080 system)
13	RD	H/L	Read operation(8080 system)
14	DB0	H/L	Data bus bit 0
15	DB1	H/L	Data bus bit 1
16	DB2	H/L	Data bus bit 2
17	DB3	H/L	Data bus bit 3
18	DB4	H/L	Data bus bit 4
19	DB5	H/L	Data bus bit 5
20	DB6	H/L	Data bus bit 6
21	DB7	H/L	Data bus bit 7
22	SP+	H/L	Speak input pin(+)
23	SP-	H/L	Speak input pin(-)
24	REC+	H/L	Receive input pin(+)
25	GND	L	GROUND
26	GND	L	GROUND
27	REC-	H/L	Receive input pin(-)
28	LED-B	H/L	Blue led control pin
29	LED-G	H/L	Green led control pin
30	LED-R	H/L	Red led control pin

5.3 Interface Timing Chart

HITACH HD66766 INTERFACE PROTOCOL



MPU I²C Interface

The I²C communication interface consists of slave address bit SA0 (D_5), I²C-bus data signal SDA (D_0 for output and D_1 for input) and I²C-bus clock signal SCL (D_4). Both the data and clock signals must be connected to pull-up resistors. There are also five input signals including, RES#, CS1#, P/S#, CS2, SP#, which is used for the initialization of device.

a) Slave address bit (SA0)

SSD1301 has to recognize the slave address before transmitting or receiving any information by the I²C-bus. The device will respond to the slave address following by the slave address bit ("SA0" bit) and the read/write select bit ("R/W#" bit) with the following byte format,

b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0

0 1 1 1 1 0 SA0 R/W#

"SA0" bit provides an extension bit for the slave address. Either "0111100" or "0111101", can be selected as the slave address of SSD1301.

"R/W#" bit is used to determine the operation mode of the I²C-bus interface. R/W#=1, it is in read mode. R/W#=0, it is in write mode.

b) I²C-bus data signal (SDA)

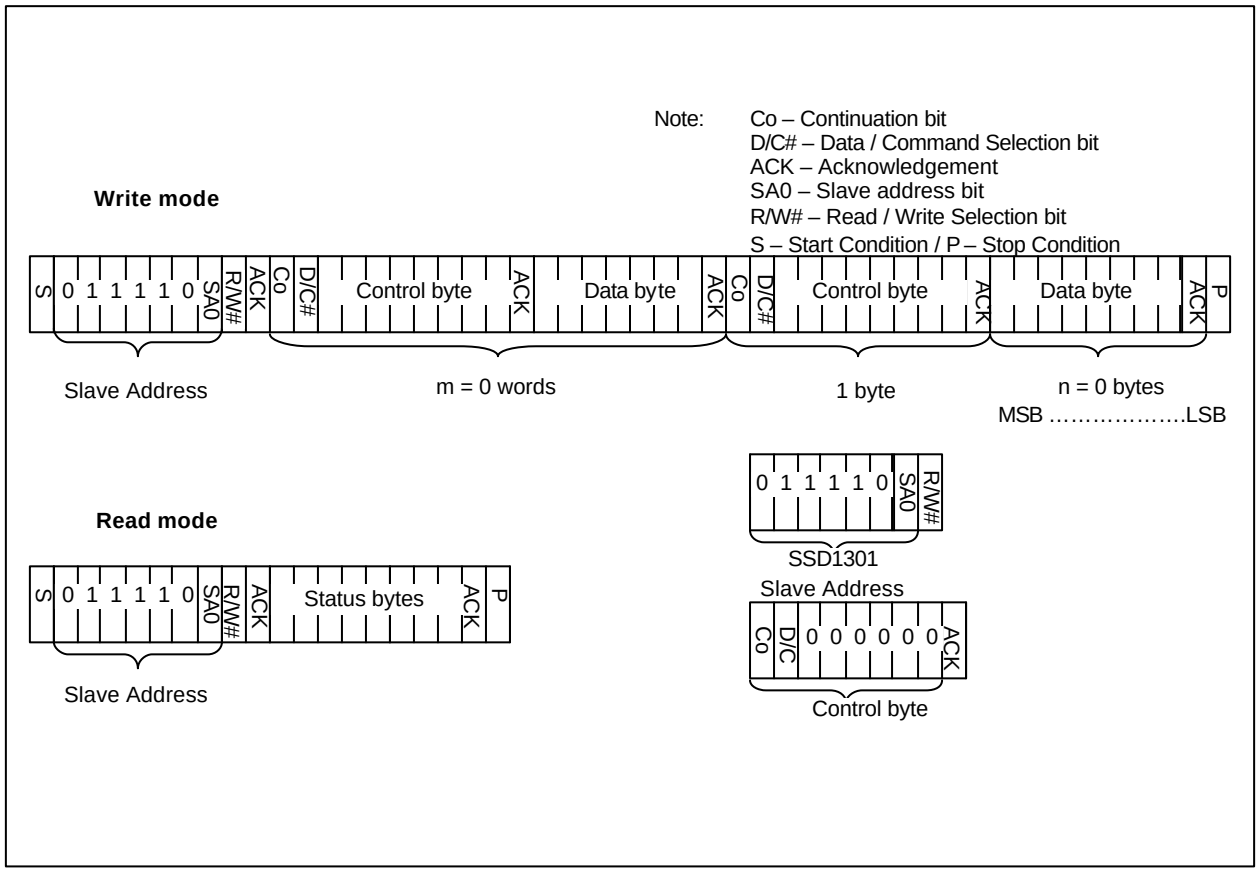
SDA acts as a communication channel between the transmitter and the receiver. The data and the acknowledgement are sent through the SDA. If SDA in is connected to the "SDA out", the device becomes fully I²C bus compatible. It should be noticed that the ITO track resistance and the pulled-up resistance at "SDA" pin becomes a voltage potential divider. As a result, the acknowledgement would not be possible to attain a valid logic 0 level in "SDA". The "SDA out" pin may be disconnected from the "SDA in" pin. With such arrangement, the acknowledgement signal will be ignored in the I²C-bus.

c) I²C-bus clock signal (SCL)

The transmission of information in the I²C-bus is following a clock signal, SCL. Each transmission of data bit is taken place during a single clock period of SCL.

I²C-bus Write data and read register status

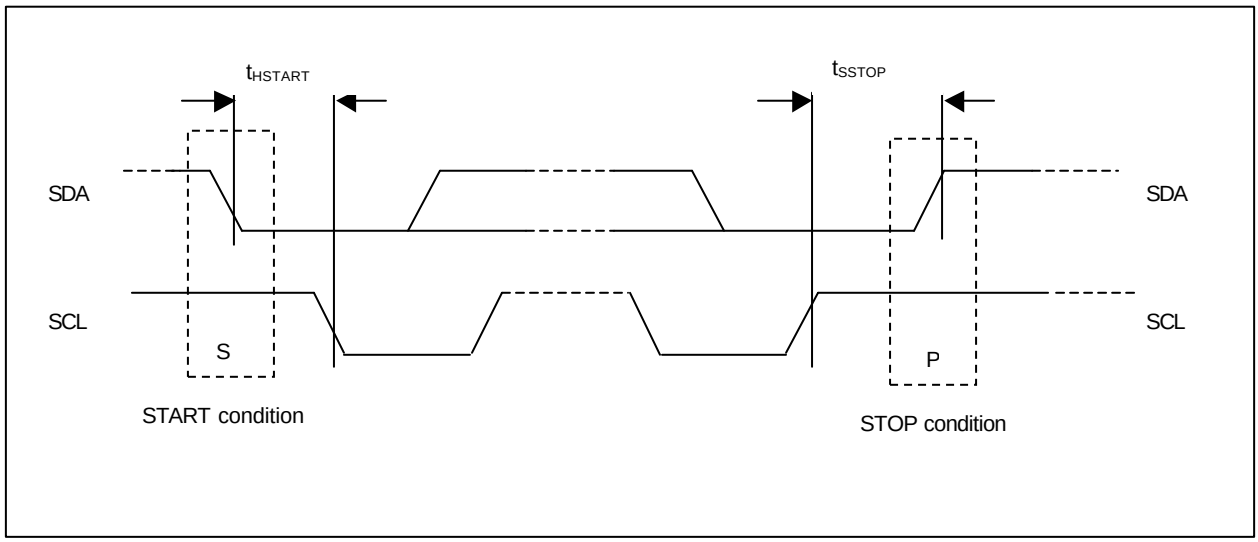
The I²C-bus interface gives access to write data and command into the device. Please refer to Figure 8 for the write mode of I²C-bus in chronological order.



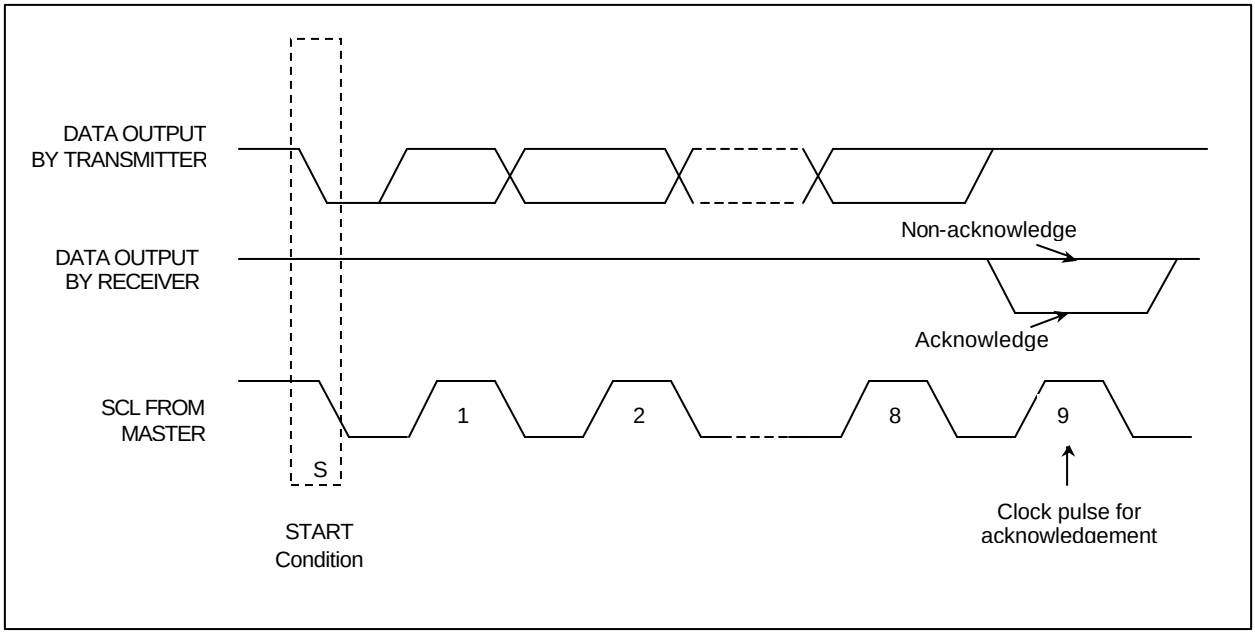
I²C-bus data format

Write mode for I^2C

1) The master device initiates the data communication by a start condition. The definition of the start condition is shown in Figure 9. The start condition is established by pulling the SDA from high to low while the SCL stays high.
2) The slave address is following the start condition for recognition use. For the SSD1301, the slave address is either "b0111100" or "b0111101" by changing the SA0 to high or low.
3) The write mode is established by setting the R/W# bit to logic "0".
4) An acknowledgement signal will be generated after receiving one byte of data, including the slave address and the R/W# bit. Please refer to the Figure 10 for the graphical representation of the acknowledge signal. The acknowledge bit is defined as the SDA line is pulled down during the high period of the acknowledgement related clock pulse.
5) After the transmission of the slave address, either the control byte or the data byte may be sent across the SDA. A control byte mainly consists of Co and D/C# bits following by six "0"'s.
    a. If the Co bit is set as logic "0", the transmission of the following information will contain data bytes only.
    b. The D/C# bit determines the next data byte is acted as a command or a data. If the D/C# bit is set to logic "0", it defines the following data byte as a command. If the D/C# bit is set to logic "1", it defines the following data byte as a data which will be stored at the GDDRAM. The GDDRAM column address pointer will be increased by one automatically after each data write.
6) Acknowledge bit will be generated after receiving each control byte or data byte.
7) The write mode will be finished when a stop condition is applied. The stop condition is also defined in Figure 9. The stop condition is established by pulling the "SDA in" from low to high while the "SCL" stays high.



Definition of the start and stop condition



Definition of the acknowledgement condition

5.4 Instruction code

Instruction List(HD66766)

Reg. No.	Register Name	R/W	RS	Upper Code DB15	DB14	DB13	DB12	DB11	DB10	Lower Code DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution Cycle	
IR	Index	0	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0	Sets the index register value.	0	Note1
SR	Status read	1	0	L7	L6	L5	L4	L3	L2	L1	L0	0	C6	C5	C4	C3	C2	C1	C0	Reads the driving raster-row position (L7–0) and contrast setting (C6–0).	0	
R00h	Start oscillation	0	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1	Starts the oscillation mode.	10 ms	Note1
	Device code read	1	1	0	0	0	0	0	1	1	1	0	1	1	0	0	1	1	0	Reads 0766H.	0	
R01h	Driver output control	0	1	0	0	0	0	0	0	CMS	SGS	0	0	0	NL4	NL3	NL2	NL1	NL0	Sets the common driver shift direction (CMS), segment driver shift direction (SGS) and driving duty ratio (NL4–0).	0	
R02h	LCD-driving-waveform control	0	1	0	0	0	0	0	RST	B/C	EOR	0	0	NW5	NW4	NW3	NW2	NW1	NW0	Sets LCD drive AC waveform (B/C), and EOR output (EOR) or the number of n-raster-rows (NW5–0) at C-pattern AC drive.	0	
R03h	Power control 1	0	1	BS3	BS2	BS1	BS0	BT3	BT2	BT1	BT0	0	DC2	DC1	DC0	AP1	AP0	SLP	STB	Sets the sleep mode (SLP), standby mode (STB), LCD power on (AP1–0), boosting cycle (DC2–0), boosting output multiplying factor (BT2–0), operation of voltage inverting circuit (BT3) and LCD drive bias value (BS3–0).	0	
R04h	Contrast control	0	1	0	0	0	0	0	VR2	VR1	VR0	0	CT6	CT5	CT4	CT3	CT2	CT1	CT0	Sets the regulator adjustment (VR2–0) and contrast adjustment (CT6–0).	0	
R05h	Entry mode	0	1	SPR	0	0	0	0	0	HWM	0	0	0	I/D1	I/D0	AM	LG2	LG1	LG0	Specifies AC counter mode (AM), increment/decrement mode (I/D1–0), high-speed write mode (HWM).	0	Note2
R06h	Compare Resister	0	1	CP15	CP14	CP13	CP12	CP11	CP10	CP9	CP8	CP7	CP6	CP5	CP4	CP3	CP2	CP1	CP0	Specifies the compare resister (CP15-0),	0	
R07h	Display control	0	1	0	0	0	0	0	VLE2	VLE1	SPT	0	0	0	0	B/W	REV	D1	D0	Specifies display on (D1-0), black-and-white reversed display (REV), pixel on/off mode (ALB), screen division driving (SPT) and vertical scroll .(VLE2-1)	0	
R0Bh	Frame frequency control	0	1	0	0	0	0	0	0	DIV1	DIV0	0	0	0	0	RTN3	RTN2	RTN1	RTN0	Specifies the line retrace period (RTN3–0) and operating clock frequency division ratio (DIV1–0).	0	
R0Ch	Power control 2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VC2	VC1	VC0	Sets the adjustment factor for the Vci voltage (VC2–0).	0	
R11h	Vertical scroll control	0	1	VL27	VL26	VL25	VL24	VL23	VL22	VL21	VL20	VL17	VL16	VL15	VL14	VL13	VL12	VL11	VL10	Sets the 1st screen display start raster- row (VL17-10) and 2nd screen display start raster-row (VL27-20).	0	
R14h	1st screen driving position	0	1	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10	Sets the 1st screen driving start position (SS17–10) and 1st screen driving end position (SE17–10).	0	
R15h	2nd screen driving position	0	1	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20	Sets 2nd screen driving start position (SS27–20) and 2nd screen driving end position (SE27–20).	0	
R16h	Horizontal RAM address position	0	1	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0	Sets start (HSA7–0) and end (HEA7–0) of the horizontal RAM address range.	0	
R17h	Vertical RAM address position	0	1	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	Sets start (VSA7–0) and end (VEA7–0) of the vertical RAM address range.	0	
R20h	RAM write data mask	0	1	WM15	WM14	WM13	WM12	WM11	WM10	WM9	WM8	WM7	WM6	WM5	WM4	WM3	WM2	WM1	WM0	Specifies write data mask (WM15–0) at RAM write.	0	

Instruction List (cont.)

				Upper Code								Lower Code									
Reg. No.	**Register Name**	**R/W**	**RS**	**DB 15**	**DB 14**	**DB 13**	**DB 12**	**DB 11**	**DB 10**	**DB 9**	**DB 8**	**DB 7**	**DB 6**	**DB 5**	**DB 4**	**DB 3**	**DB 2**	**DB 1**	**DB 0**	**Description**	**Execution Cycle**
R21h	RAM address set	0	1	AD15–8 (upper)										AD6–0 (lower)						Initially set the RAM address to the address counter (AC).	0
R22	RAM data write	0	1	Write data (upper)										Write data (lower)						Writes data to the RAM.	0
	RAM data read	1	1	Read data (upper)										Read data (lower)						Reads data from the RAM.	0
R30h	Grayscale palette control (1)	0	1	0	0	PK15	PK14	PK13	PK12	PK11	PK10	0	0	PK05	PK04	PK03	PK02	PK01	PK00	Specifies the grayscale palette.	0
R31h	Grayscale palette control (2)	0	1	0	0	PK35	PK34	PK33	PK32	PK31	PK30	0	0	PK25	PK24	PK23	PK22	PK21	PK20	Specifies the grayscale palette.	0
R32h	Grayscale palette control (3)	0	1	0	0	PK55	PK54	PK53	PK52	PK51	PK50	0	0	PK45	PK44	PK43	PK42	PK41	PK40	Specifies the grayscale palette.	0
R33h	Grayscale palette control (4)	0	1	0	0	PK75	PK74	PK73	PK72	PK71	PK70	0	0	PK65	PK64	PK63	PK62	PK61	PK60	Specifies the grayscale palette.	0
R34h	Grayscale palette control (5)	0	1	0	0	PK95	PK94	PK93	PK92	PK91	PK90	0	0	PK85	PK84	PK83	PK82	PK81	PK80	Specifies the grayscale palette.	0
R35h	Grayscale palette control (6)	0	1	0	0	PK 115	PK 114	PK 113	PK 112	PK 111	PK 110	0	0	PK 105	PK 104	PK 103	PK 102	PK 101	PK 100	Specifies the grayscale palette.	0
R36h	Grayscale palette control (7)	0	1	0	0	PK 135	PK 134	PK 133	PK 132	PK 131	PK 130	0	0	PK 125	PK 124	PK 123	PK 122	PK 121	PK 120	Specifies the grayscale palette.	0
R37h	Grayscale palette control (8)	0	1	0	0	PK 155	PK 154	PK 153	PK 152	PK 151	PK 150	0	0	PK 145	PK 144	PK 143	PK 142	PK 141	PK 140	Specifies the grayscale palette.	0
R38h	Grayscale palette control (9)	0	1	0	0	PK 175	PK 174	PK 173	PK 172	PK 171	PK 170	0	0	PK 165	PK 164	PK 163	PK 162	PK 161	PK 160	Specifies the grayscale palette.	0
R39h	Grayscale palette control (10)	0	1	0	0	PK 195	PK 194	PK 193	PK 192	PK 191	PK 190	0	0	PK 185	PK 184	PK 183	PK 182	PK 181	PK 180	Specifies the grayscale palette.	0
R3Ah	Grayscale palette control (11)	0	1	0	0	PK 215	PK 214	PK 213	PK 212	PK 211	PK 210	0	0	PK 205	PK 204	PK 203	PK 202	PK 201	PK 200	Specifies the grayscale palette.	0
R3Bh	Grayscale palette control (12)	0	1	0	0	PK 235	PK 234	PK 233	PK 232	PK 231	PK 230	0	0	PK 225	PK 224	PK 223	PK 222	PK 221	PK 220	Specifies the grayscale palette.	0
R3Ch	Grayscale palette control (13)	0	1	0	0	PK 255	PK 254	PK 253	PK 252	PK 251	PK 250	0	0	PK 255	PK 244	PK 243	PK 242	PK 241	PK 240	Specifies the grayscale palette.	0
R3Dh	Grayscale palette control (14)	0	1	0	0	PK 275	PK 274	PK 273	PK 272	PK 271	PK 270	0	0	PK 265	PK 264	PK 263	PK 262	PK 261	PK 260	Specifies the grayscale palette.	0
R3Eh	Grayscale palette control (15)	0	1	0	0	PK 295	PK 294	PK 293	PK 292	PK 291	PK 290	0	0	PK 285	PK 284	PK 283	PK 282	PK 281	PK 280	Specifies the grayscale palette.	0
R3Fh	Grayscale palette control (16)	0	1	0	0	PK 315	PK 314	PK 313	PK 312	PK 311	PK 310	0	0	PK 305	PK 304	PK 303	PK 302	PK 301	PK 300	Specifies the grayscale palette.	0

Note: 1. "*" means doesn't matter.
2. High-speed write mode is available only for the RAM writing.

COMMAND TABLE (SSD1301)

Command table (D/C# =0, R/W#(WR#)=0, E (RD#)=1)

Bit Pattern	Command	Description
$0000X_3X_2X_1X_0$	Set Lower Column Address	Set the lower nibble of the column address register using $X_3X_2X_1X_0$ as data bits. The initial display line register is reset to 0000b after POR.
$0001X_3X_2X_1X_0$	Set Higher Column Address	Set the higher nibble of the column address register using $X_3X_2X_1X_0$ as data bits. The initial display line register is reset to 0000b after POR.
$01X_5X_4X_3X_2X_1X_0$	Set Display Start Line	Set display RAM display start line register from 0-63 using $X_5X_4X_3X_2X_1X_0$. Display start line register is reset to 000000 during POR.
10000001 $X_7X_6X_5X_4X_3X_2X_1X_0$	Set Contrast Control Register	Double byte command to select 1 out of 256 contrast steps. Contrast increases as $X_7X_6X_5X_4X_3X_2X_1X_0$ is increased from 00000000b to 11111111b. $X_7X_6X_5X_4X_3X_2X_1X_0$ =10000000b after POR
$1010000X_0$	Set Segment Re-map	X_0=0: column address 00H is mapped to SEG0 (POR) X_0=1: column address 83H is mapped to SEG0
$1010010X_0$	Set Entire Display On/Off	X_0=0: normal display (POR) X_0=1: entire display on
$1010011X_0$	Set Normal/Inverse Display	X_0=0: normal display (POR) X_0=1: inverse display
$1010111X_0$	Set Display On/Off	X_0=0: turns off OLED panel (POR) X_0=1: turns on OLED panel
$1011X_3X_2X_1X_0$	Set Page Address	Set GDDRAM Page Address (0~8) for read/write using $X_3X_2X_1X_0$
$1100X_3$ * * *	Set COM Output Scan Direction	X_3=0: normal mode (POR) X_3=1: remapped mode. COM0 to COM[N-1] becomes COM[N-1] to COM0 in Multiplex ratio is equal to N.
11100000	Set Read-Modify-Write Mode	Read-Modify-Write mode will be entered in which the column address will not be increased during display data read. After POR, Read-modify-write mode is turned OFF
11100010	Software Reset	Initialize internal status registers
11101110	Set End of Read-Modify-Write Mode	Exit Read-Modify-Write mode. RAM Column address before entering the mode will be restored. After POR, Read-modify-write mode is OFF.
11100011	NOP	Command for No Operation
1111 * * * *	Set Test Mode	Reserved for IC testing. Do NOT use.
10101110 10100101	Set Sleep Mode	Sleep mode will be entered with two commands: Command 1: Turns off OLED panel Command 2: Set entire display on

Bit Pattern	Command	Description
10101000 **$X_5X_4X_3X_2X_1X_0$	Set Multiplex Ratio	To select multiplex ratio N from 2 to the maximum multiplex ratio (POR value) (including icon line). Max. mux ratio: 65 N= $X_5X_4X_3X_2X_1X_0$+2, e.g. N=001111b+2=17
10101010 *10$X_4X_3X_2X_1X_0$	Set Frame Frequency	Frame frequency is set by the following formula: $X_4X_3X_2X_1X_0$=00001: frame frequency = $\frac{F_{osc}}{4xN}$ $X_4X_3X_2X_1X_0$ =00010: frame frequency = $\frac{F_{osc}}{6xN}$ $X_4X_3X_2X_1X_0$ =00011: frame frequency = $\frac{F_{osc}}{8xN}$ where N is mux ratio set by the "set Multiplex Ratio" command. POR values are $\frac{F_{osc}}{6x65}$ for N=65, and $\frac{F_{osc}}{8x49}$ for N= 49
10101011 10$X_5$0$X_3$00X_0	Set Bias Current Mode	Set bias current level of segment output cell X_5=0 and X_3=1 and X_0=0: Normal (POR) X_5=1 and X_3=0 and X_0=1: Set low bias current level
1101000X_0	Set Icon Mode	X_0=0: icon mode off (POR) X_0=1: icon mode on
11010011 **$X_5X_4X_3X_2X_1X_0$	Set Display Offset	$X_5X_4X_3X_2X_1X_0$:000000=no scroll by row (POR) . . . . . . 111111=scroll by 63 rows
11011000 00000$X_2$0X_0	Set Low Power Display Mode	X_2=0 and X_0=0: Normal (POR) X_2=1 and X_0=1: Set low power consumption
11011001 $X_7X_6X_5X_4X_3X_2X_1X_0$	Set Precharge Period	$X_7X_6X_5X_4$: Set precharge period (POR=1000) [Invalid entry for $X_7X_6X_5X_4$=0001 or 0000] $X_3X_2X_1X_0$=1000: Normal (POR) $X_3X_2X_1X_0$=0011: For low precharge period usage
11011010 ***1**$X_1$0	Set Current Mode	X_1=0: Select half range current mode (POR) X_1=1: Select full range current mode

Note: Remark "*" stands for "Don't Care"

Read command table (D/C#=0, R/W#(WR#)=1, E(RD#)=1 for 6800 or E(RD#)=0 for 8080)

Bit Pattern	Command	Description
$D_7D_6D_5D_4D_3D_2D_1D_0$	Status Register Read	D_7=0: indicates the driver is ready for command. D_7=1: indicates the driver is Busy. D_6=0: indicates reverse segment mapping with column address D_6=1: indicates normal segment mapping with column address D_5=0: indicates the display is ON D_5=1: indicates the display is OFF D_4=0: initialization is not in progress D_4=1: initialization is in progress after RES# or software reset

Note: Patterns other than that given in Command Table are prohibited to enter to the chip as a command; otherwise, unexpected result will occur.

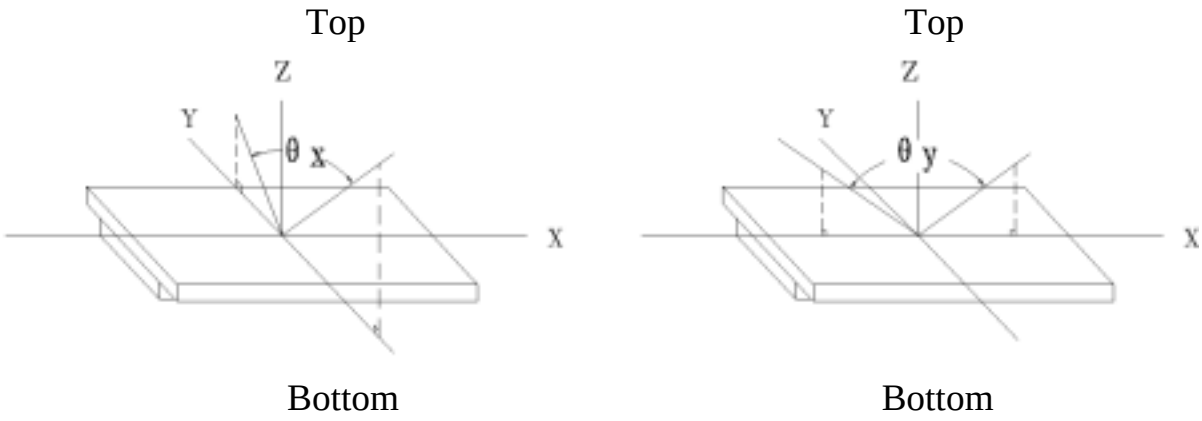
6. Optical Characteristics

6.1 Optical Characteristics V_{LCD}=16.8V Ta=25℃

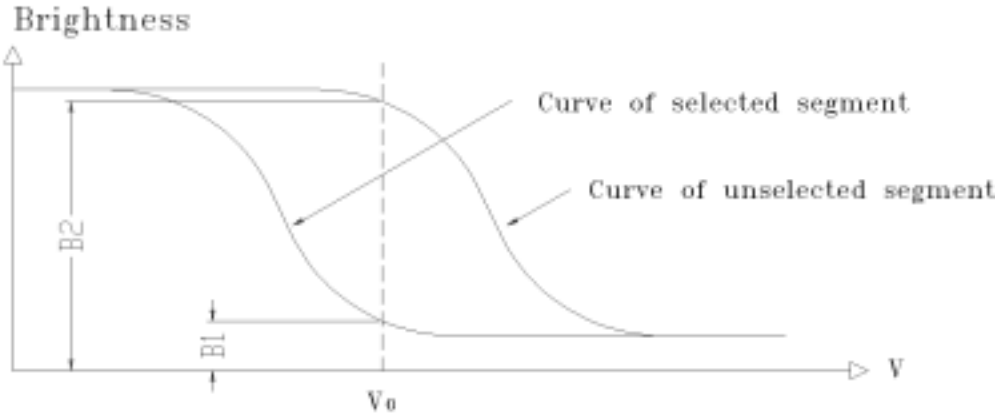
Item		Symbol	Condition			Min.	Typ.	Max.	Unit
Viewing Angle		θ_x	Cr≥2	θ_y=0 °	MAIN	-40--+35			Deg
					SUB	-60--36			
		θ_y		θ_x=0 °	MAIN	-30--+30			
					SUB	-42--40			
Contrast Ratio		Cr	θ_x=0 ° θ_y=0 °			30	50	60	--
Response Time	Turn on	T_{on}	θ_x=0 ° θ_y=0 °			-	-	150	ms
	Turn off	T_{off}				-	-	100	
Color Of CIE Coord-Inate	Red	x	θ_x=0 ° θ_y=0 °			-	0.43	-	-
		y				-	0.35	-	-
	Green	x	θ_x=0 ° θ_y=0 °			-	0.32	-	-
		y				-	0.46	-	-
	Blue	x	θ_x=0 ° θ_y=0 °			-	0.22	-	-
		y				-	0.26	-	-

6.2 Definition of Optical Characteristics

6.2.1 Definition of Viewing Angle



6.2.2 Definition of Contrast Ratio

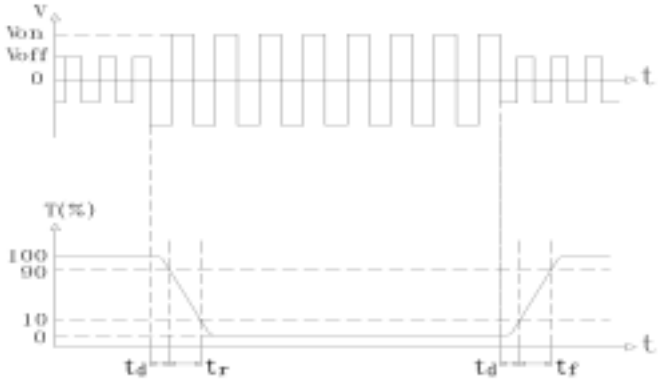


$$\text{Contrast Ratio} = B2/B1 = \frac{\text{unselected state brightness}}{\text{selected state brightness}}$$

Measuring Conditions:

1) Ambient Temperature: 25℃ ; 2) Frame frequency: 70.0Hz

6.2.3 Definition of Response time



Turn on time: $t_{on} = t_d + t_r$ Turn off time: $t_{off} = t_d + t_f$

Measuring Condition:

1) Operating Voltage:MAIN-LCD 16.8V SUB-LCD 9V

2) Frame frequency: 70.0Hz

6.3 Brightness Characteristic

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Brightness	Bp	Ta=25℃±3℃ 30-80%RH	100	-	-	cd/m^2
Uniformity	△Bp		-	-	60	%

Note:

1. The data is measured after LEDs are turned on for 5 minutes.
2. Testing conditions LED: V_{LED} = 270 V (AC)
   LCD: All dots are on (White color)
3. Brightness in the center of the LCD panel.
4. Definition of Uniformity (△Bp)
   △Bp = Bp (Min.) / Bp (Max.) X 100 (%)
   Bp (Max.) = Maximum brightness in 9 measurement spots
   Bp (Min.) = Minimum brightness in 9 measurement spots

7. Reliability

7.1 Content of Reliability Test Ta=25℃

No.	Test Item	Content of Test	Test condition
1	High Temperature Storage	Endurance test applying the high storage temperature for a long time	80℃±2℃ 240H Restore 4H at 25℃
2	Low Temperature Storage	Endurance test applying the low storage temperature for a long time	-30℃±2℃ 240H Restore 4H at 25℃
3	High Temperature /Humidity Storage	Endurance test applying the high temperature and high humidity storage for a long time	70℃±2℃ 90%RH 240H Restore 4H at 25℃
4	Temperature Cycle	Endurance test applying the low and high temperature cycle -30℃←→25℃←→80℃←→25℃ 30min 5min 30min 5min ←——————————→ 1 cycle	-30℃/80℃ 10 cycles Restore 4H at 25℃
5	Vibration Test (package state)	Endurance test applying the vibration during transportation	10Hz~150Hz, 100m/s^2, 120min
6	Shock Test (package state)	Endurance test applying the shock during transportation	Half- sine wave, 300m/s^2, 18ms
7	Atmospheric Pressure Test	Endurance test applying the atmospheric pressure during transportation by air	25kPa 16H Restore 2H

7.2 Failure Judgment Criterion

Criterion Item	Test Item No.									Failure Judgement Criterion
	1	2	3	4	5	6	7	8	9	
Basic Specification	√	√	√	√	√	√	√	√	√	Out of the basic Specification
Electrical specification	√	√	√	√	√					Out of the electrical specification
Mechanical Specification							√	√		Out of the mechanical specification
Optical Characteristic	√	√	√	√	√	√			√	Out of the optical specification
Note	For test item refer to 8.1									
Remark	Basic specification = Optical specification + Mechanical specification									

8. Quality Level

Examination or Test	At T_a=25℃ (unless otherwise stated)	Inspection				
		Min.	Max.	Unit	IL	AQL
External Visual Inspection	Under normal illumination and eyesight condition, the distance between eyes and LCD is 25cm.	See Appendix A			II	Major 1.0 Minor 2.5
Display Defects	Under normal illumination and eyesight condition, display on inspection.	See Appendix B			II	Major 1.0 Minor 2.5
Note: Major defects: Open segment or common, Short, Serious damages, Leakage Miner defects: Others Sampling standard conforms to GB2828						

9. Precautions for Use of LCD Modules

9.1 Handling Precautions

10.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

9.1.2 If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

9.1.3 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

9.1.4 The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

9.1.5 If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- ― Isopropyl alcohol
- ― Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- ― Water
- ― Ketone
- ― Aromatic solvents

9.1.6 Do not attempt to disassemble the LCD Module.

9.1.7 If the logic circuit power is off, do not apply the input signals.

9.1.8 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

a. Be sure to ground the body when handling the LCD Modules.

b. Tools required for assembly, such as soldering irons, must be properly ground.

c. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

d. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

9.2 Storage precautions

9.2.1 When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

9.2.2 The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0℃ ～ 40℃

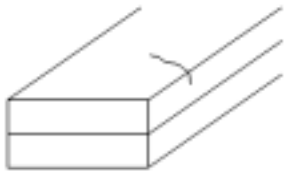
Relatively humidity: ≤80%

9.2.3 The LCD modules should be stored in the room without acid, alkali and harmful gas.

9.3 The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.

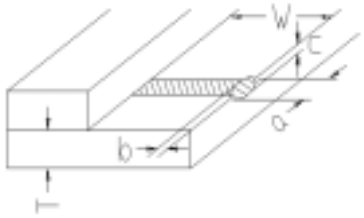
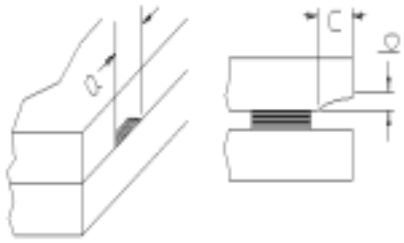
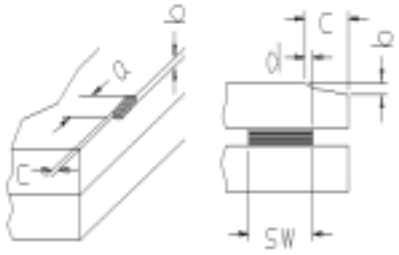
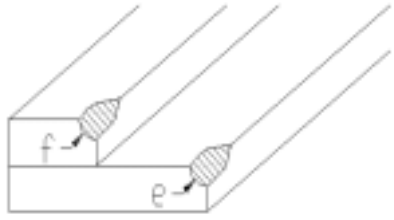
Appendix A

Inspection items and criteria for appearance defects

<table>
<tr><td>Items</td><td>Contents</td><td colspan="3">Criteria</td></tr>
<tr><td>Leakage</td><td></td><td colspan="3">Not permitted</td></tr>
<tr><td>Rainbow</td><td></td><td colspan="3">According to the limit specimen</td></tr>
<tr><td rowspan="3">Polarizer</td><td>Wrong polarizer attachment</td><td colspan="3">Not permitted</td></tr>
<tr><td rowspan="2">Bubble between polarizer and glass</td><td>Not counted</td><td colspan="2">Max. 3 defects allowed</td></tr>
<tr><td>ϕ<0.3mm</td><td colspan="2">0.3mm≤ϕ≤0.5mm</td></tr>
<tr><td>Scratches of polarizer</td><td colspan="3">According to the limit specimen</td></tr>
<tr><td rowspan="3">Black spot (in viewing area)</td><td rowspan="3">  </td><td>Not counted</td><td>Max. 3 spots allowed</td><td rowspan="4">Max. 3 spots (lines) allowed</td></tr>
<tr><td>X<0.2mm</td><td>0.2mm≤X≤0.5mm</td></tr>
<tr><td colspan="2">X=(a+b)/2</td></tr>
<tr><td rowspan="2">Black line (in viewing area)</td><td rowspan="2">  </td><td>Not counted</td><td>Max. 3 lines allowed</td></tr>
<tr><td>a<0.02mm</td><td>0.02mm≤a≤0.05mm
b≤2.0mm</td></tr>
<tr><td>Progressive cracks</td><td>  </td><td colspan="3">Not permitted</td></tr>
</table>

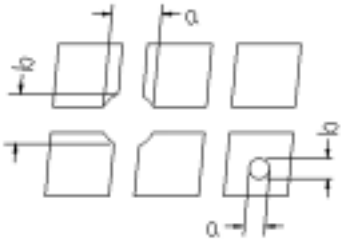
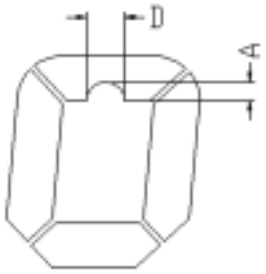
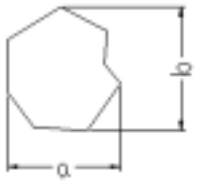
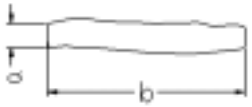
Appendix A

Inspection item and criteria for appearance defects (continued)

<table>
<tr><th>Items</th><th>Contents</th><th colspan="4">Criteria</th></tr>
<tr><td rowspan="4">Glass Cracks</td><td>Cracks on pads
  </td><td>a
≤3mm
≤2mm</td><td>b
≤W/5
≤W/5</td><td>c
≤T/2
T/2<C<T</td><td>Max. 2 cracks allowed</td><td rowspan="4">Max. 5 cracks allowed</td></tr>
<tr><td>Cracks on contact side
  </td><td colspan="2">a
≤3mm
≤2mm
C shall be not reach the seal area</td><td>b
≤T/2
T/2<b<T</td><td rowspan="2">Max. 2 cracks allowed</td></tr>
<tr><td>Cracks on non-contact side
  </td><td colspan="2">a
≤3mm
≤2mm
C≤0.5mm
d≤SW/3</td><td>b
≤T/2
T/2<b<T</td></tr>
<tr><td>Corner cracks
  </td><td colspan="3">e<2.0mm^2
f<2.0mm^2</td><td>Max. 3 cracks allowed</td></tr>
</table>

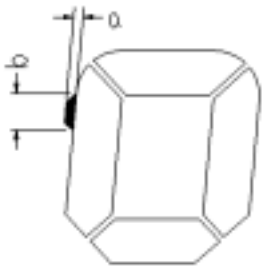
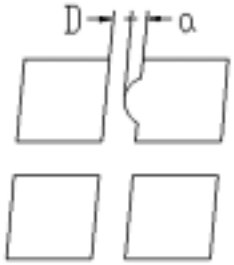
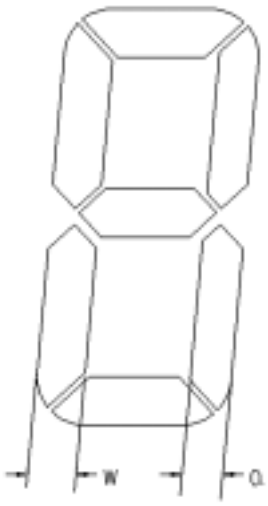
Appendix B

Inspection items and criteria for display defects

<table>
<tr><td colspan="2">Items</td><td>Contents</td><td colspan="3">Criteria</td></tr>
<tr><td colspan="3">Open segment or open common</td><td colspan="3">Not permitted</td></tr>
<tr><td colspan="3">Short</td><td colspan="3">Not permitted</td></tr>
<tr><td colspan="3">Wrong viewing angle</td><td colspan="3">Not permitted</td></tr>
<tr><td colspan="3">Contrast radio uneven</td><td colspan="3">According to the limit specimen</td></tr>
<tr><td colspan="3">Crosstalk</td><td colspan="3">According to the limit specimen</td></tr>
<tr><td rowspan="4">Pin holes and cracks in segment (DOT)</td><td rowspan="2">  </td><td>Not counted</td><td>Max.3 dots allowed</td><td rowspan="4">Max.3 dots allowed</td></tr>
<tr><td>X<0.1mm</td><td>0.1mm≤X≤0.2mm</td></tr>
<tr><td colspan="2">X=(a+b)/2</td></tr>
<tr><td rowspan="2">  </td><td>Not counted</td><td>Max.2 dots allowed</td></tr>
<tr><td>A<0.1mm</td><td>0.1mm≤A≤0.2mm
D<0.25mm</td></tr>
<tr><td rowspan="3">Black spot (in viewing area)</td><td rowspan="3">  </td><td>Not counted</td><td>Max.3 spots allowed</td><td rowspan="4">Max.3 spots (lines) allowed</td></tr>
<tr><td>X<0.1mm</td><td>0.1mm≤X≤0.2mm</td></tr>
<tr><td colspan="2">X=(a+b)/2</td></tr>
<tr><td rowspan="2">Black line (in viewing area)</td><td rowspan="2">  </td><td>Not counted</td><td>Max.3 lines allowed</td></tr>
<tr><td>a<0.02mm</td><td>0.02mm≤a≤0.05mm
b≤0.5mm</td></tr>
</table>

Appendix B

Inspection items and criteria for display defects (continued)

<table>
<tr><th>Items</th><th>Content</th><th colspan="3">Criteria</th></tr>
<tr><td rowspan="3">Transfor-
mation
of segment</td><td rowspan="2">  </td><td>Not counted</td><td>Max. 2 defects allowed</td><td rowspan="3">Max.3
defects
allowed</td></tr>
<tr><td>x＜0.1mm</td><td>0.1mm≤x≤0.2mm</td></tr>
<tr><td colspan="2">x=(a+b)/2</td></tr>
<tr><td>  </td><td>Not counted</td><td>Max. 1 defects allowed</td><td rowspan="2">Max.3
defects
allowed</td></tr>
<tr><td>a＜0.1mm</td><td>0.1mm≤a≤0.2mm
D>0</td></tr>
<tr><td>  </td><td colspan="3">Max.2 defects allowed
0.8W≤a≤1.2W

a=measured value of width
W=nominal value of width</td></tr>
</table>