

Description

The ADAM-824B and -825B analog-to-digital converters (ADCs), with their integral sample-and-hold amplifiers, are complete data acquisition subsystems that provide overall accuracies better than many ADCs alone. This high level of accuracy is accompanied by improved stability and reduced power dissipation over previous converters of similar architecture. For example, with a differential linearity tempco of ± 3 ppm, the 14-bit accuracy of the ADAM-824B is maintained over a full 20°C temperature rise! Due to the integral sample-and-hold (S/H) circuits, the ADAM-824B and -825B give the system designer optimized system performance and eliminate the potential difficulties in integrating the S/H and A/D of precision data acquisition systems.

Both the ADAM-824B and ADAM-825B provide guaranteed end-to-end performance in a small 2" x 4" modular package. Their accuracy, along with features such as tri-state output, low power dissipation, and low cost, make them an excellent choice for a variety of data acquisition systems, automatic test equipment, and analytical instrumentation.

Features

- **High Throughput Rate**
20 kHz (Includes both sampling and conversion time)
- **Low Power**
0.9W
- **S/H Feedthrough Rejection**
90 dB
- **Low Differential Nonlinearity**
 $\pm 1/2$ LSB maximum
- **Low Tempco**
Differential nonlinearity
 ± 2 ppm/°C FSR maximum (825B)
- **Low Noise**
50 μ V rms (ADC)
- **Byte-Selectable HCT Tri-State Buffered Outputs**
- **Pin-Programmable Input Voltage Range**
0V to +5V, 0V to +10V, ± 5 V, ± 10 V

Applications

- Automatic Test Equipment
- Analytical Instrumentation
- Precision Data Acquisition Systems
- Materials Testing



ANALOGIC

**ADAM-824B/
825B**

14- and 15-Bit
Highly Stable, Low Power
Sampling A/D Converters

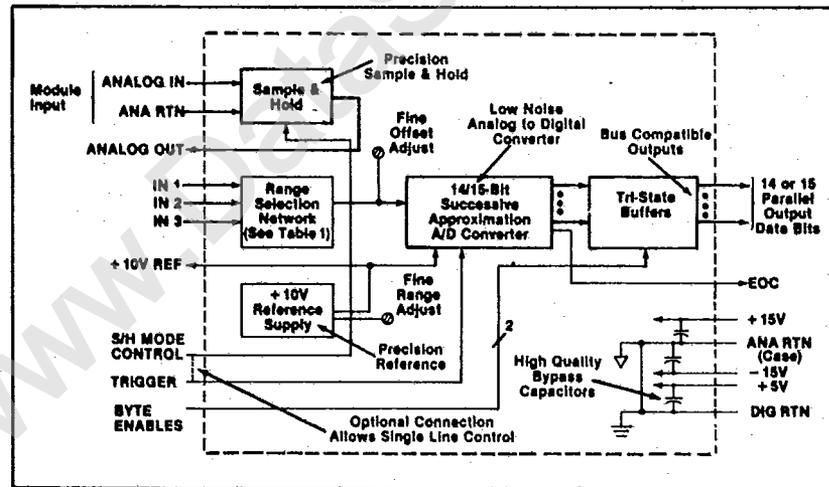


Figure 1. ADAM-824B/5B Function Block Diagram.

SAMPLING ANALOG-TO-DIGITAL CONVERTERS

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SPECIFICATIONS

T-51-07-01

(Includes combined S/H and A/D performance, and applies to both ADAM-824B and ADAM-825B except where noted)

(All specifications guaranteed at 25°C unless otherwise noted)

ANALOG INPUT

Full Scale Range (FSR)
0V to +5V, 0V to +10V, ±5V, ±10V
Maximum Input Without Damage
15V
Impedance
100 Megohm // 5 pF
Bias Current¹
1 nA maximum

ACCURACY

Absolute Accuracy²
Calibrated to ±0.006% FSR
Relative Accuracy³
±0.005% FSR maximum (ADAM-824B),
±0.003% FSR maximum (ADAM-825B)
Differential Nonlinearity
±0.003% FSR maximum (ADAM-824B),
±0.0015% FSR maximum (ADAM-825B)
Quantizing Error
± 1/2 LSB
Noise (S/H plus A/D)
75 μV rms
Noise (A/D only)
50 μV rms
Monotonicity
Guaranteed

STABILITY

Tempco of Differential Nonlinearity
± 3 ppm/°C FSR maximum (ADAM-824B),
± 2 ppm/°C FSR maximum (ADAM-825B)
Gain Tempco
± 8 ppm/°C FSR maximum
Offset Tempco
± 30 μV/°C typical, ± 80 μV/°C maximum
Clock Stability
± 0.03%/°C
Power Supply Sensitivity
± 0.001% FSR per 1% change in supply voltage
Warm-up Time to Specified Accuracy
5 minutes
Recommended Recalibration Interval
6 months

DYNAMIC PERFORMANCE

Maximum Throughput Rate⁴
20,000 measurements/second
S/H Aperture Delay
50 ns
S/H Aperture Uncertainty
1 ns
S/H Hold Mode Feedthrough Rejection
90 dB, measured with 20V p-p
10 kHz sinewave input
S/H Droop Rate¹
0.2 μV/μs
S/H Dielectric Absorption Error⁵
± 0.005% of input voltage change

DIGITAL OUTPUTS

General
Tri-state CMOS HCT
Parallel Data
Positive true; unipolar binary, offset binary, or two's complement (see Table 1)
End of Conversion (EOC)
Positive true

DIGITAL INPUTS

General
Standard TTL compatible, one unit load/line
S/H Mode Control
Logic 1 = SAMPLE (6 μs minimum)
Logic 0 = HOLD (conversion time minimum);
logic 1 to logic 0 transition time 10 ns maximum
A/D Trigger
Negative-going edge; logic 1 to
logic 0 transition 50 ns maximum
Low/High Byte Enable
Logic 0 = enable
Logic 1 = 3.5V min. @ 1 μA, HCT
Logic 0 = 1.5V max. @ 1 μA, HCT

POWER REQUIREMENTS

+ 15V, ± 3%
37 mA maximum
- 15V, ± 3%
35 mA maximum
+ 5V, ± 5%
9 mA maximum
Power Dissipation
0.9W

ENVIRONMENTAL AND MECHANICAL

Operating Temperature
0°C to +70°C
Storage Temperature
- 25°C to +85°C
Relative Humidity
5% to 95% noncondensing to 40°C
Shielding
Electrostatic (RFI) 6 sides;
Electrostatic (EMI) 5 sides
Package Size
2.0" x 4.0" x 0.375"
(50.8 x 101.6 x 9.53 mm)

Notes:

1. Doubles every 10°C.
2. Traceable to NBS, calibrated on ± 10V range.
3. Worst-case summation of S/H and A/D nonlinearity errors.
4. Includes 6 μs maximum for S/H acquisition and 44 μs maximum for A/D.
5. At maximum throughput rate. The error decreases as sampling time is decreased.

Operation

The ADAM-824B and -825B interface directly to most commonly available input devices (multiplexers, amplifiers, etc.). The high impedance of the fast, fully buffered, unity gain S/H input amplifier minimizes source loading errors. Excellent hold-mode feedthrough performance is provided even at 10 kHz—the maximum information frequency of data that can be digitized at the module's 20 kHz sampling rate (single-channel application). For multichannel inputs, excellent feedthrough rejection is maintained by switching the multiplexer channels coincident with either edge of the S/H mode control.

Parallel data bits are driven by tri-state buffers and may be enabled in one or two bytes. (If the tri-state feature is not needed, normal binary outputs can be obtained by connecting the enable pins to ground.) To obtain two's complement, use B1 instead of B1 (the MSB). Maximum system throughput rate is attained by reading the output of an A/D conversion while the S/H is acquiring the next sample.

To operate with a single control pulse, connect the S/H mode control input to the A/D trigger, and observe the timing requirements for the S/H mode control (Figure 2).

Operating range is established by connecting the S/H output to the appropriate A/D input pins (see Table 1). These pins provide access to the S/H output (a low-impedance buffer amp) for arbitrary signal processing prior to A/D conversion. The S/H can be bypassed for applications requiring direct input to a low noise A/D converter.

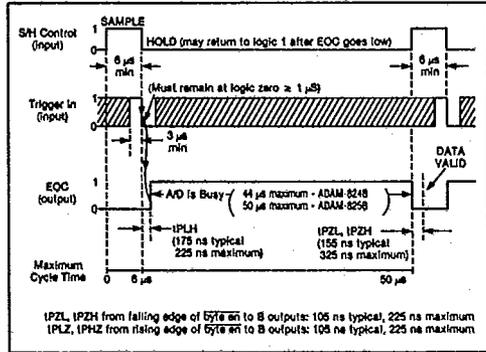


Figure 2. ADAM-824B/5B Timing.

Performance Features T-51-07-01

In most high accuracy applications the S/H, A/D, and related interfaces constitute the key subsystem of the data conversion process. By using an ADAM-series module that has been "worst-case" designed, the system engineer avoids the problems that commonly occur when transforming a 15-bit breadboard into a finished product.

End-to-end performance is not subject to the surprises that usually result from S/H output spikes, ground loops, timing problems, and so on. Offset is specified (and trimmed) as a single characteristic. The signal path from the S/H to the A/D is very short, minimizing noise pick-up, cross-talk, etc.; trim potentiometers and the bypass capacitors that filter power supply noise are in the module, not on the PC board. The module is EMI/RFI shielded.

The integral S/H is a precision circuit similar to Analogic's model MP260, so the total S/H error is very small. Due to the module's low power dissipation, errors induced by self-heating of the module are negligible. Internal temperature rise is only 12.5°C above external ambient, much less than in many other A/D converters.

The resulting performance is exceptional. Figure 3 shows a dynamic crossplot taken for the ADAM-824B with worst-case inputs (small signals). This crossplot allows visual detection of very small errors (approaching 1/8 LSB). The unit displays differential nonlinearity that is well within the specified ± 1/2 LSB.

RANGE PROGRAMMING AND OUTPUT CODING				
A/D Input Connections				
Full Scale Range	Connect IN 1 to	Connect IN 2 to	Connect IN 3 to	Input Impedance
0 to +5V	S/H ANA OUT	S/H ANA OUT	S/H ANA OUT	1.25k Ω
0 to +10V	ANA RTN	S/H ANA OUT	S/H ANA OUT	2.5k Ω
-5V to +5V	S/H ANA OUT	+10V REF	ANA RTN	2.5k Ω
-10V to +10V	ANA RTN	+10V REF	S/H ANA OUT	5.0k Ω

Output Codes	
ADAM-824B (14 bits)	ADAM-825B (14 bits)
Unipolar Binary	
11 111 111 111 111 = +9.99939V*	111 111 111 111 111 = +9.99969V*
00 000 000 000 000 = 0.00000V	000 000 000 000 000 = 0.00000V
Offset Binary	
11 111 111 111 111 = +9.99678V†	111 111 111 111 111 = +9.99939V†
10 000 000 000 000 = 0.00000V	100 000 000 000 000 = 0.00000V
00 000 000 000 000 = -10.00000V	000 000 000 000 000 = -10.00000V
Two's Complement	
01 111 111 111 111 = +9.99678V†	011 111 111 111 111 = +9.99939V†
00 000 000 000 000 = 0.00000V	000 000 000 000 000 = 0.00000V
10 000 000 000 000 = -10.00000V	100 000 000 000 000 = -10.00000V

*For +5V FSR, divide voltage by two
 †For ±5V FSR, divide voltage by two

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Calibration

Due to excellent long-term stability, these modules will rarely require re-calibration. They should, however, be re-adjusted when the selected FSR is changed. Offset should be zeroed prior to trimming the range.

Offset Zeroing Procedure

1. Provide the S/H analog input voltage shown in the accompanying table.
2. Adjust the Offset pot until the module output code corresponds to 0V, with the LSB alternating equally between 0 and 1.

Range Trimming Procedure (Gain Adjust)

1. Provide the S/H analog input voltage shown in the accompanying table.
2. Adjust the Gain pot until the module output code is all 1's with the LSB alternating equally between 0 and 1.

Input Voltages for Calibration

Nominal FSR	ADAM-824B (14 Bits)		ADAM-825B (14 Bits)	
	Offset	Range	Offset	Range
0 to + 5V	153 μ V	+ 4.99954V	76 μ V	+ 4.99977V
0 to + 10V	305 μ V	+ 9.99909V	153 μ V	+ 9.99954V
-5 to + 5V	305 μ V	+ 4.99909V	153 μ V	+ 4.99954V
-10 to 10V	610 μ V	+ 9.99817V	305 μ V	+ 9.99909V

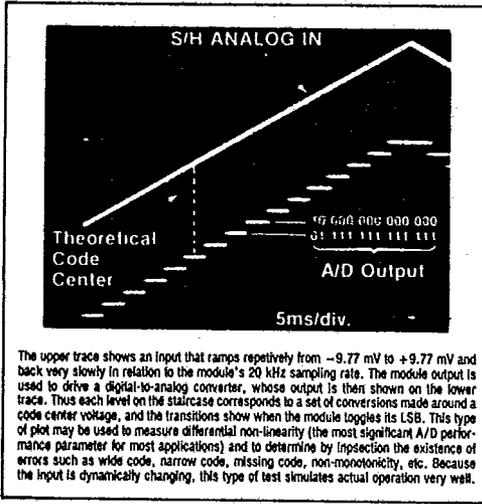
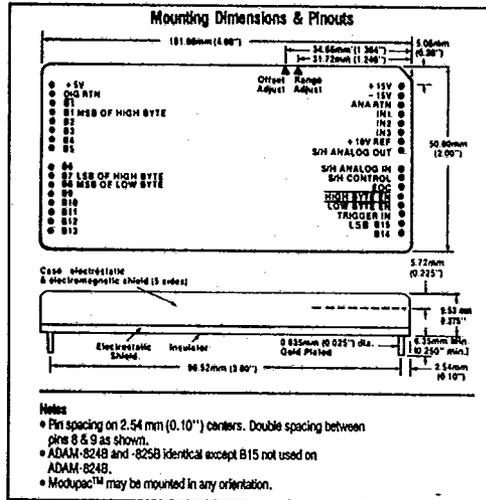


Figure 3. ADAM-824B Crossplot Shows Highly Linear Performance.



Ordering Guide

Simply Specify

- ADAM-824B
- ADAM-825B

- 14-Bit Resolution
- 15-Bit Resolution