Frequency Generator for Fibre Channel Systems

General Description

The **ICS9112-35/36** are high-speed clock generators designed to support fibre channel system requirements. The **ICS9112-35/36** generates 106.25 MHz from a 17 MHz crystal.

An exact frequency multiplying ratio ensures better than ±100 ppm frequency accuracy using a standard AT crystal with external load capacitors (typically 33pF±5% for an 18pF load crystal). Achieving ±100 ppm over four years requires the crystal to have a ±20 ppm initial accuracy, ±30 ppm temperature and ±5 ppm/year aging coefficients.

The **ICS9112-35/36** with less than 40ps accumulative jitter is well suited for Fibre Channel applications.

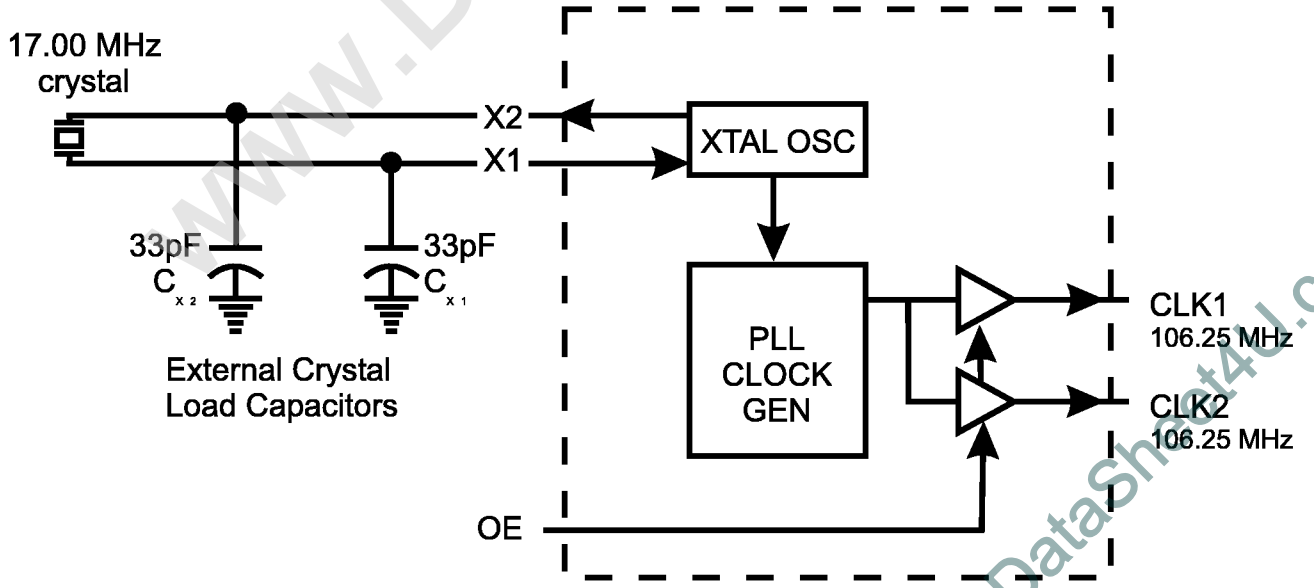
Features

- Generates 106.25 MHz clocks from a 17 MHz crystal
- Less than 45ps one sigma jitter (15ps typ.)
- Less than ±130ps absolute jitter
- Less than 40ps accumulative jitter @ 256 cycles
- Rise/fall times less than 1.2ns driving 15pF
- On-chip loop filter components
- 3.0V-5.5V supply range
- 8-pin, 150-mil SOIC package

Applications

- Specifically designed to support the high-speed clocking requirements of fibre channel systems.

Block Diagram



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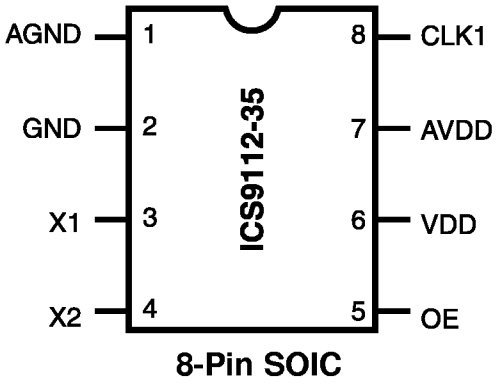
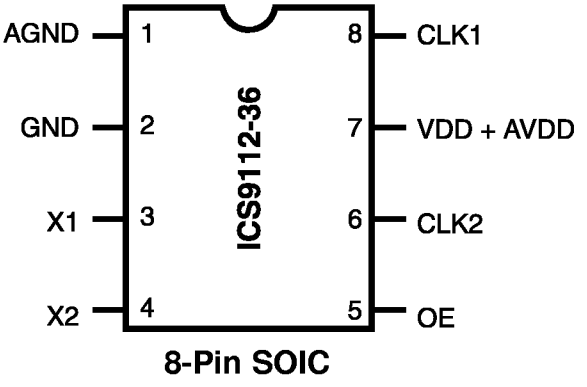
Pin Configurations



8-Pin SOIC



8-Pin SOIC

Functionality

OE	X1, X2 (MHz)	FOUT (MHz)
1	17.00	106.25
0	17.00	Tristate

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	AGND	PWR	Analog ground.
2	GND	PWR	Digital Ground.
3	X1	IN	Crystal or clock input to device; nominally 17.00 MHz. Requires external load capacitors.
4	X2	IN	Crystal drive output from device. Requires external load capacitors.
5	OE	IN	Output Enable (has internal pull_up.): when OE is low, it tristates the clock output (FOUT)
6	VDD	PWR	+3.3 or +5.0 volt supply (-35)
	CLK2	OUT	Clock output (106.25MHz) (-36)
7	AVDD	PWR	Analog power. (Must equal digital power voltage).(-35)
	VDD+AVDD	PWR	Digital and analog power, +3.3 or +5.0Volt supply (-36)
8	CLK1	OUT	Clock output (106.25MHz)

Absolute Maximum Ratings

AVDD, VDD referenced to GND 7V
Operating temperature under bias. . . . . 0°C to +70°C
Storage temperature . . . . . -65°C to +150°C
Voltage on I/O pins referenced to GND. . . . . GND -0.5V to VDD +0.5V
Power dissipation . . . . . 0.5 Watts

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 5.0V

Operating V_{DD} = +4.5V to +5.5V; T_A =0°C to 70°C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		-	-	0.8	V
Input High Voltage	V_{IH}		2.0	-	-	V
Input Low Current	I_{IL}	V_{IN}=0V (Pull-up input)	-16.0	-6.0	-	µA
Input High Current	I_{IH}	V_{IN}=V_{DD}	-2.0	-	2.0	µA
Output Low Voltage[1]	V_{OL}	I_{OL}=10mA	-	0.15	0.40	V
Output High Voltage[1]	V_{OH}	I_{OH}=-30mA	2.4	3.25	-	V
Output Low Current[1]	I_{OL}	V_{OL}=0.8V	22.0	35.0	-	mA
Output High Current[1]	I_{OH}	V_{OH}=2.0V	-	-50.0	-35.0	mA
Supply Current	I_{DD}	Unloaded	-	22.0	45.0	mA
Pull-up Resistor[1]	R_{pu}		-	100	-	k ohms
AC Characteristics						
Rise Time[1]	T_{r1}	15pF load, 0.8 to 2.0V	-	0.8	1.2	ns
Fall Time[1]	T_{f1}	15pF load, 2.0 to 0.8V		0.7	1.2	ns
Duty Cycle[1]	D_t	15pF load @ 1.4V	42.0	49.0	55.0	%
Jitter, One Sigma[1]	T_{j1s}	15pF load	-	15.0	45.0	ps
Jitter, Absolute[1]	T_{jab}	15pF load	-130.0		130.0	ps
Accumulative Jitter[1]	T_{jacc}	15pF load @ 256 Cycle	-	17.0	-	ps
Input Frequency[1]	F_i		-	17.0	-	MHz
Output Frequency[1]	F_o		-	106.25	-	MHz
Power-up Time[1]	T_{pu}		-	7.58	18.0	ms
Crystal Input Capacitance[1]	C_{inx}	X1 (Pin 1) X2 (Pin 8)	-	3.0	-	pF

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

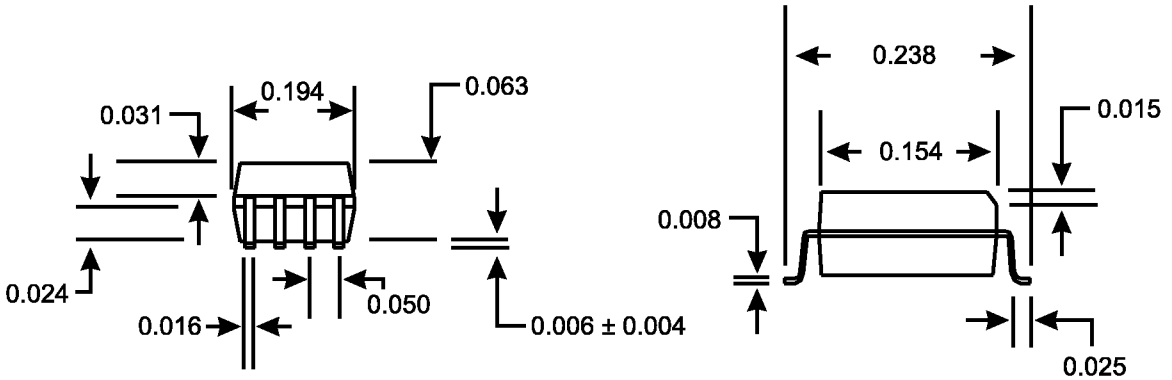
SUBJECT TO CHANGE PRELIMINARY INFORMATION

Electrical Characteristics at 3.3V

Operating V_{DD} = +3.0V to +3.7V; T_A =0°C to 70°C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		-	-	$0.20V_{DD}$	V
Input High Voltage	V_{IH}		$0.7V_{DD}$	-	-	V
Input Low Current	I_{IL}	V_{IN}=0V (Pull-up input)	-7.0	-2.5	-	µA
Input High Current	I_{IH}	$V_{IN}=V_{DD}$	-2.0	-	2.0	µA
Output Low Voltage[1]	V_{OL}	I_{OL}=6mA	-	$0.05V_{DD}$	$0.1V_{DD}$	V
Output High Voltage[1]	V_{OH}	I_{OH}=-5mA	$0.85V_{DD}$	$0.92V_{DD}$	-	V
Output Low Current[1]	I_{OL}	$V_{OL}=0.2V_{DD}$	15.0	22.0	-	mA
Output High Current[1]	I_{OH}	$V_{OH}=0.7V_{DD}$	-	-17.0	-10.0	mA
Supply Current	I_{DD}	Unloaded	-	14.0	30.0	mA
Pull-up Resistor[1]	R_{pu}		-	175.0	-	k ohms
AC Characteristics						
Rise Time[1]	T_{r1}	15pF load, 0.8 to 2.0V	-	0.65	1.2	ns
Fall Time[1]	T_{f1}	15pF load, 2.0 to 0.8V	-	0.6	1.2	ns
Duty Cycle[1]	D_t	15pF load @ 1.4V	40.0	50.0	60.0	%
Jitter, One Sigma[1]	T_{j1s}	15pF load	-	15.0	45.0	ps
Jitter, Absolute[1]	T_{jab}	15pF load	-130.0	-	130.0	ps
Accumulative Jitter[1]	T_{jacc}	15pF load @ 256 cycle	-	17.0	-	ps
Input Frequency[1]	F_i		-	17.0	-	MHz
Output Frequency[1]	F_o		-	106.25	-	MHz
Power-up Time[1]	T_{pu}		-	7.58	18.0	ms
Crystal Input Capacitance[1]	C_{inx}	X1 (Pin 1) X2 (Pin 8)	-	3.0	-	pF

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.



8-Pin Plastic SOIC Package

Ordering Information

ICS9112M-35/36

Example:

ICS XXXX M-PPP

- **Pattern Number(2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  M=SOIC, SOP
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS=Standard Device

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