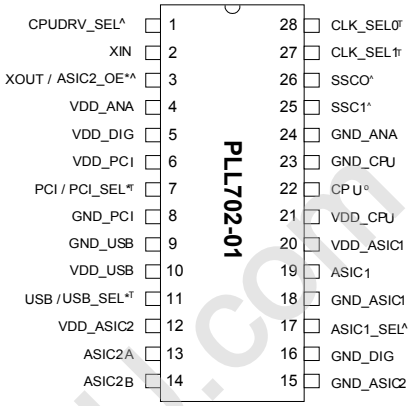
PLL702-01

Clock Generator for PowerPC Based Applications

FEATURES

- 1 CPU Clock output with selectable frequencies (50, 66, 75, 80, 83, 90, 100,125 or 133 MHz).
- 1 ASIC output clock (at CPU clock or CPU clock ÷ 2).
- 2 ASIC output clocks (at CPU clock) w/ output enable.
- 1 PCI output clock w/ output enable
- 1 Selectable 48, 30 or 12MHz (USB) output.
- Selectable Spread Spectrum (SST) for EMI reduction on ASIC and CPU.
- PowerPC compatible output and drive CPU Clock.
- Selectable reduced 67% drive strength on CPU Clock
- Advanced, low power, sub-micron CMOS processes.
- 14.31818MHz fundamental crystal input.
- 3.3V and/or 2.5V operation.
- Available in 28-Pin 209mil SSOP (QSOP).

PIN ASSIGNMENT (28 pin SSOP)



Note: ^: Internal pull-up resistor
°: Selectable reduced drive strength
*: Bi-directional pin
T: Tri-level input

DESCRIPTIONS

The PLL702-01 is a low cost, low jitter, and high performance clock synthesizer for generic PowerPC based applications. It provides one CPU clock, three ASIC outputs, one PCI output, and a selectable 48, 30 or 12MHz (USB) output. The user can choose between 9 different CPU clock frequencies, while the ASIC output can be identical or half of the CPU frequency. Low EMI Spread Spectrum Technology is available for the CPU, ASIC and PCI clocks. The CPU drive strength is user selectable from 100% to 67%. All frequencies are generated from a single low cost 14.31818MHz crystal. The CPU and ASIC clock can be driven from an independent 2.5V power supply.

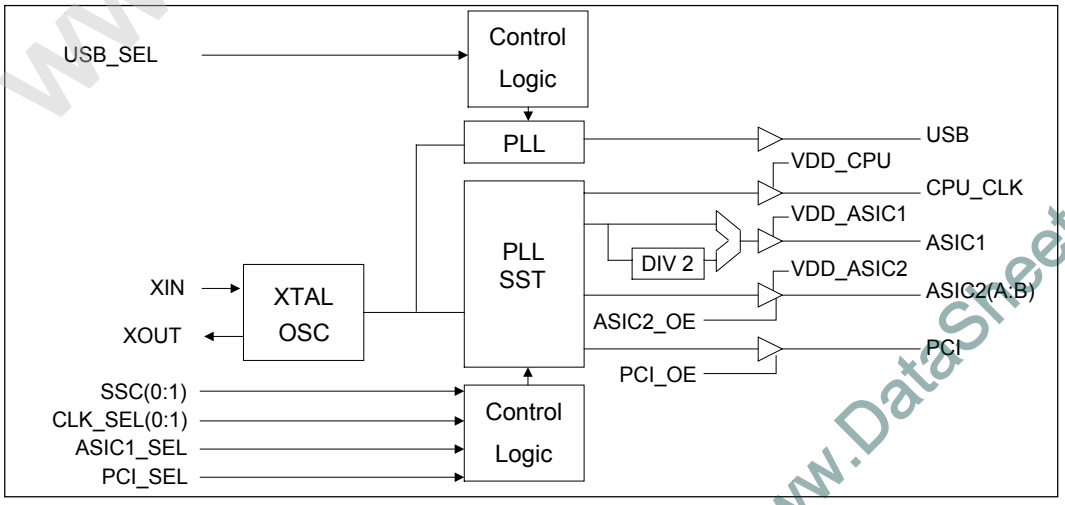
FREQUENCY TABLES

CLK_SEL1	CLK_SEL0	CPU	ASIC1		ASIC2
			ASIC1_SEL=1	ASIC1_SEL=0	
0	0	50 MHz	50 MHz	25 MHz	50 MHz
0	M	66 MHz	66 MHz	33 MHz	66 MHz
0	1	75 MHz	75 MHz	37.5 MHz	75 MHz
M	0	80 MHz	80 MHz	40 MHz	80 MHz
M	M	83 MHz	83 MHz	41.5 MHz	83 MHz
M	1	90 MHz	90 MHz	45 MHz	90 MHz
1	0	100 MHz	100 MHz	50 MHz	100 MHz
1	M	125 MHz	125 MHz	62.5 MHz	125 MHz
1	1	133 MHz	133 MHz	66.5 MHz	133 MHz

Notes: When CPU=90MHz, it implements 88.88MHz to meet PCI=33.3MHz/66.6MHz; When CPU=133MHz, it implements 130.9MHz to meet Power PC clock AC Timing Specification.

PCI output		
PCI_SEL = 0	PCI_SEL = M	PCI_SEL = 1
66 MHz (min. 62.0 MHz)	33 MHz (min. 31.0 MHz)	Tri-state (output disabled)

BLOCK DIAGRAM



PIN DESCRIPTIONS

Name	Number	Type	Description
CPUDRV_SEL	1	I	CPU drive strength selector pin. The CPU drive strength can be set to 67% of nominal strength with CPUDRV_SEL = 0. When CPUDRV_SEL = 1, the CPU drive strength will be 100% of the nominal strength. Internal pull-up of 60kΩ. 0=connect to GND, 1=leave open.
XIN	2	I	Crystal input to be connected to a 14.31818MHz fundamental crystal (CL = 20pF, parallel resonant mode). Load capacitors have been integrated on the chip. No external Load capacitor is required.
XOUT/ ASIC2_OE	3	B	Bi-directional pin. Upon power-on, the value of ASIC2_OE is latched in and used to enable / disable the ASIC2A and ASIC2B outputs (outputs are enabled if ASIC2_OE=1, otherwise, outputs are in tri-state). Internal pull-up of 120 kΩ. After the input has been latched-in, the pin serves as Crystal connection.
VDD_ANA / GND_ANA VDD_DIG / GND_DIG	4, 5, 16, 24	P	3.3V power supply and GND.
VDD_xxx / GND_xxx for USB, CPU, PCI, ASIC1 and ASIC2	6, 8, 9, 10, 12, 15, 18, 20, 21, 23	P	CPU, PCI, ASIC1 and ASIC2 outputs have separate power supply pins (VDD and GND). VDD_CPU, VDD_ASIC1 and VDD_ASIC2 can accept 3.3V and/or 2.5V power supply. Other VDD pins are to be supplied 3.3V
PCI / PCI_SEL	7	B	Bi-directional pin. Upon power-on, the value of PCI_SEL is latched in and used to select the PCI clock output (see frequency table on p.1). PCI output is disabled (tri-state) when PCI_SEL=1. PCI clock will be 33MHz (min. 31.25MHz) if PCI_SEL=M (not connected), and 66MHz (min. 62.5MHz) if PCI_SEL=0. 0=15kΩ to GND, M=leave open, 1=15kΩ to VDD_PCI
USB / USB_SEL	11	B	Bi-directional pin. Upon power-on, the value of USB_SEL is latched in and used to select the USB output (see USB selection table on page 3). After the input has been latched-in, the pin serves as USB (48, 30 or 12 MHz) output. 0=15kΩ to GND, M=leave open, 1=15kΩ to VDD_USB
ASIC2A and ASIC2B	13, 14	O	ASIC clock signal output pins. ASIC2A and ASIC2B will have the same frequency as CPU. These outputs can be disabled through ASIC2_OE.
ASIC1_SEL	17	I	ASIC1 frequency select input pin (see also frequency table on p.1). ASIC1 will have the same frequency as CPU if ASIC1_SEL = 1, and have half of CPU if ASIC_SEL = 0. Internal pull-up of 60 kΩ. 0=connect to GND, 1=leave open
ASIC1	19	O	ASIC1 output pin (see frequency table on p.1 and ASIC1_SEL pin description).
CPU	22	O	CPU clock signal output pin. The CPU clock frequency is selected as per the frequency table on page 1, depending on the value of CLK_SEL(0:1). Selectable drive strength through CPUDRV_SEL.
SSC(0:1)	25, 26	I	Bi-level input with Pull-up for SST control (see Spread Spectrum selection table on p.3). 0=connect to GND, 1=leave open.
CLK_SEL(0:1)	27, 28	I	Tri-level inputs for CPU clock frequency selection (see table on p.1). 0=connect to GND, M=not connected, 1=connect to VDD_ANA

USB OUTPUT FREQUENCY AND CPU DRIVE STRENGTH SELECTION TABLES

USB_SEL	USB
0	48 MHz
M	30 MHz
1	12 MHz

CPUDRV_SEL	CPU drive strength
0	67% (reduced)
1	100% (nominal)

SPREAD SPECTRUM SELECTION TABLE

SSC1	SSC0	Spread Spectrum Modulation
0	0	OFF
0	1	- 0.50% – Downspread
1	0	- 1.00% – Downspread
1	1	- 1.25% – Downspread

FUNCTIONAL DESCRIPTION

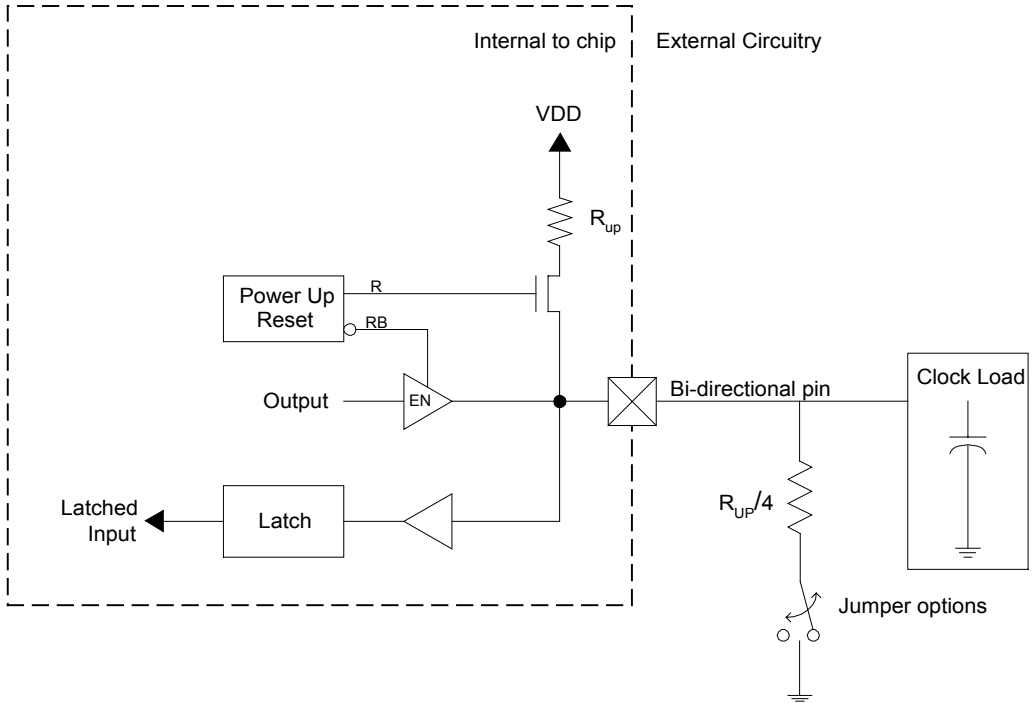
Tri-level and two-level inputs

In order to reduce pin usage, the PLL702-01 uses tri-level input pins. These pins allow 3 levels for input selection: namely, 0 = Connect to GND, 1 = Connect to VDD, M = Do not connect. Thus, unlike the two-level selection pins, the tri-level input pins are in the “M” (mid) state when not connected. In order to connect a tri-level pin to a logical “zero”, the pin must be connected to GND. Likewise, in order to connect to a logical “one”, the pin must be connected to VDD.

Connecting a bi-directional pin

The PLL702-01 also uses bi-directional pins. The same pin serves as input upon power-up, and as output as soon as the inputs have been latched. The value of the input is latched-in upon power-up. Depending on the pin (see pin description), the input can be tri-level or a standard two-level. Unlike unidirectional pins, bi-directional pins cannot be connected directly to GND or VDD in order to set the input to "0" or "1", since the pin also needs to serve as output. In the case of two level input pins, an internal pull-up resistor is present. This allows a default value to be set when no external pull down resistor is connected between the pin and GND (by definition, a tri-level input has a the default value of "M" (mid) if it is not connected). In order to connect a bi-directional pin to a non-default value, the input must be connected to GND or VDD through an external pull-down/pull-up resistor. ***Note:*** *when the output load presents a low impedance in comparison to the internal pull-up resistor, the internal pull-up resistor may not be sufficient to pull the input up to a logical “one”, and an external pull-up resistor may be required.*
For bi-directional inputs, the external loading resistor between the pin and GND has to be sufficiently small (compared to the internal pull-up resistor) so that the pin voltage be pulled below 0.8V (logical “zero”). In order to avoid loading effects when the pin serves as output, the value of the external pull-down resistor should however be kept as large as possible. In general, it is recommended to use an external resistor of around one sixth to one quarter of the internal pull-up resistor (see Application Diagram). ***Note:*** *when the output is used to drive a load presenting an small resistance between the output pin and VDD, this resistance is in essence connected in parallel to the internal pull-up resistor. In such a case, the external pull-down resistor may have to be dimensioned smaller to guarantee that the pin voltage will be low enough achieve the desired logical “zero”. This is particularly true when driving 74FXX TTL components.*

APPLICATION DIAGRAM: BI-DIRECTIONAL PINS WITH INTERNAL PULL-UP

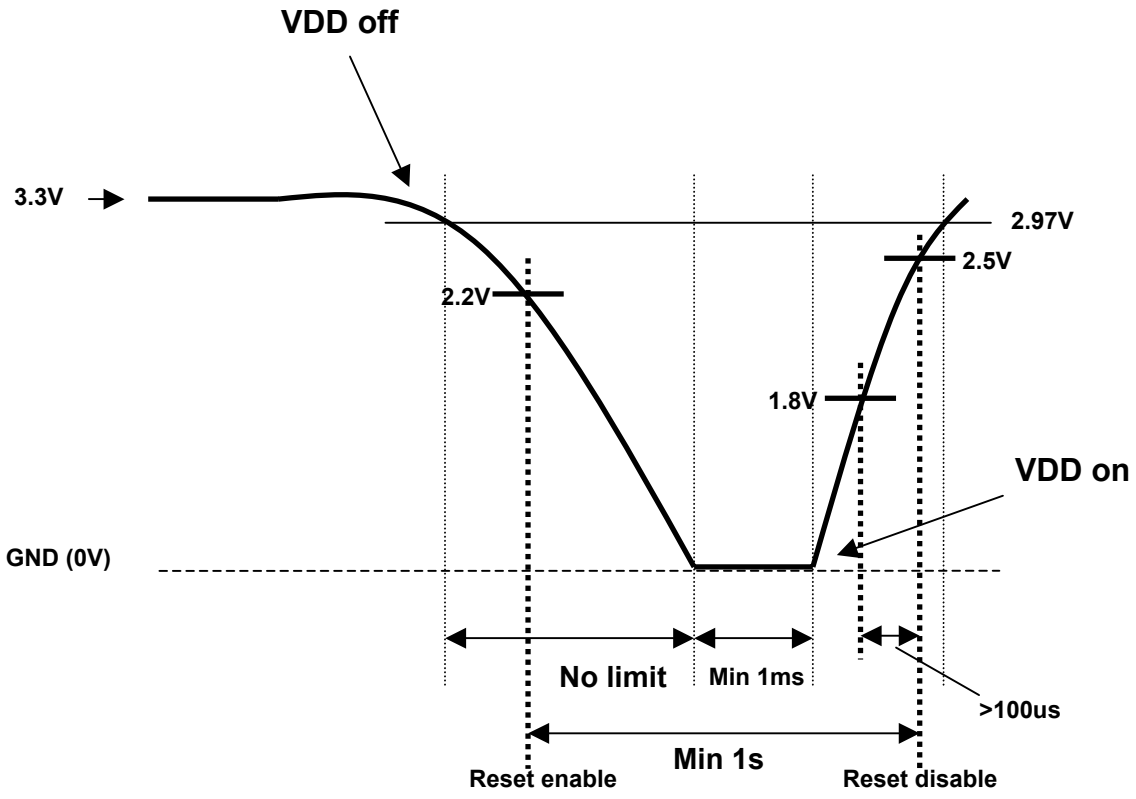


NOTE: Rup=Internal pull-up resistor (see pin description). Power-up Reset : R starts from 1 to 0 while RB starts from 0 to 1.

VDD Power Up Ramp requirements:

At startup, the chip reads a lot of settings for operation according to the application's requirements. Since reading the settings is done only at startup and then frozen for the time of operation, it is important that the power-up environment is somewhat controlled to facilitate proper reading of the settings. The important VDD pins are VDD_ANA and VDD_DIG and they should apply to the following two-startup requirements:

1. VDD_DIG should be equally fast or slower than VDD_ANA. VDD_DIG performs a chip reset when VDD has reached a certain level and VDD_ANA should have reached at least up to the same level as well to properly process the reset.
2. The VDD Power Up Ramp of VDD_DIG and VDD_ANA should pass through the section 1.8V to 2.5V no faster than 100µs and with a continuously increasing slope. In this section the tri-level select inputs are read.
3. After VDD Power off, VDD should be allowed to go to 0V and stay there for at least 1ms before a new VDD Power on. It is important that proper preconditions exist at every startup. Remaining charges in the chip or in circuit filter capacitors may interfere with the preconditions so it is important that VDD has been at 0V for some time before each startup.



Electrical Specifications

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage Range	V_{CC}	-0.5	7	V
Input Voltage Range	V_I	-0.5	V_{CC}+0.5	V
Output Voltage Range	V_O	-0.5	V_{CC}+0.5	V
Soldering Temperature			260	°C
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature		0	70	°C

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

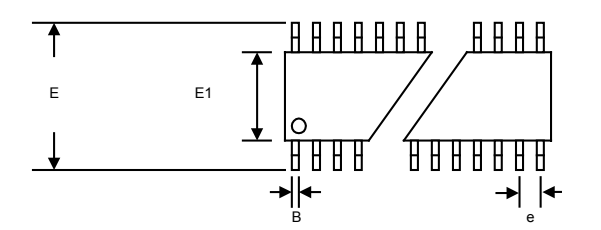
2. AC Specification

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Frequency			14.31818		MHz
SST modulation sweep rate			28		kHz
Output Rise Time	0.8V to 2.0V with no load			1.5	ns
Output Fall Time	2.0V to 0.8V with no load			1.5	ns
Duty Cycle	At VDD/2	45	50	55	%
Max. output skew CPU and ASIC1	Equal loading (20 pF) Equal frequency & drive strength Equal Power Supply for both ASIC and CPU		500	750	ps
Max. output skew CPU and ASIC2	Equal loading (20 pF) Equal frequency & drive strength Equal Power Supply for both ASIC and CPU		200	250	ps
Max. Absolute Period Jitter	Long term, No SST			150	ps
Max. Jitter, cycle to cycle	Long term + Short term			120	ps

3. DC Specification

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operating Voltage	VDD_ANA VDD_DIG	Nominal voltage is 3.3V	2.97		3.63	V
	VDD_USB VDD_PCI VDD_ASIC1 VDD_ASIC2 VDD_CPU	Nominal voltage is 2.5V	2.25		2.75	V
		Nominal voltage is 3.3V	2.97		3.63	V
Input High Voltage	V_{IH}			VDD/2		V
Input Low Voltage	V_{IL}			VDD/2	VDD/2 - 1	V
Input High Voltage	V_{IH}	For all Tri-level input	VDD-0.5			V
Input Low Voltage	V_{IL}	For all Tri-level input			0.5	V
Input High Voltage	V_{IH}	For all normal input	2			V
Input Low Voltage	V_{IL}	For all normal input			0.8	V
Output High Voltage	V_{OH}	I_{OH} = -25mA VDD = 3.3V	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 25mA			0.4	V
Output High Voltage At CMOS Level	V_{OH}	I_{OH} = -8mA	VDD-0.4			V
Nominal Output Current	I_{out}		25			mA
Operating Supply Current	I_{DD}	No Load		35		mA
Short-circuit Current	I_S			±100		mA

PACKAGE INFORMATION



28PIN SSOP

Package	SSOP (QSOP) 209mil			
Pins#	**28**			
Unit	mm		inches	
	min	max	min	max
A		2.0		0.079
A1	0.05		0.002	
B	0.25	0.38	0.01	0.015
C	0.09	0.25	0.004	0.010
D	9.9	10.5	0.390	0.413
E	7.40	8.20	0.291	0.323
E1	5.00	5.60	0.197	0.220
e	0.65BSC		0.0256BSC	
L	0.55	0.95	0.022	0.038

ORDERING INFORMATION

For part ordering, please contact our Sales Department:
47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER
The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range