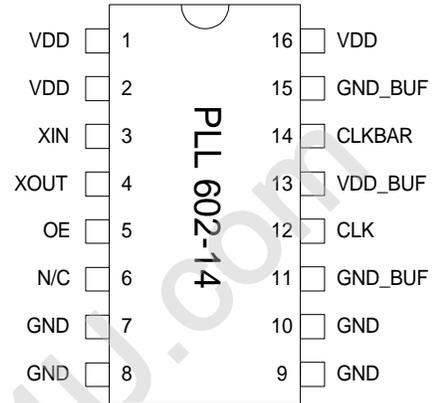


192MHz – 384MHz Low Phase Noise LVDS XO (12 – 24MHz Crystals)

FEATURES

- Low phase noise output for the 192MHz to 384MHz range (-134 dBc at 10kHz offset).
- LVDS output.
- 12 to 24MHz crystal input.
- Integrated crystal load capacitor: no external load capacitor required.
- Output Enable selector.
- 3.3V operation.
- Available in 16 Pin TSSOP or SOIC.

PIN CONFIGURATION



$F_{OUT} = F_{XIN} \times 16$

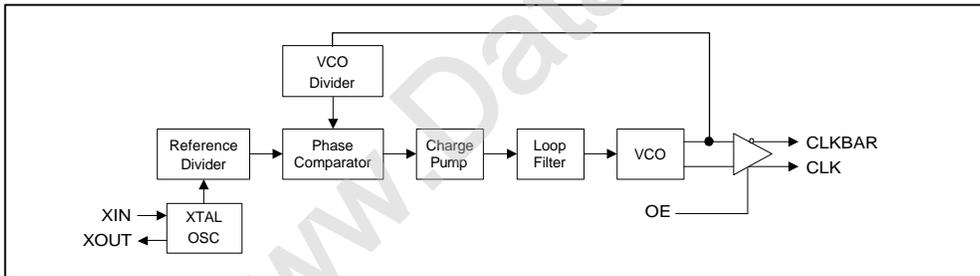
DESCRIPTION

The PLL602-14 is a monolithic low jitter and low phase noise (-134dBc/Hz @ 10kHz offset) XO IC with LVDS output, for 192MHz to 384MHz output range. It provides a low phase noise reference frequency using a low cost crystal.

The chip delivers an output frequency of $F_{XIN} \times 16$. This makes the PLL602-14 ideal for a wide range of applications.

OE (Pin 5)	Output State
0	Tri-state
1 (Default)	Output enabled

BLOCK DIAGRAM



192MHz – 384MHz Low Phase Noise LVDS XO (12 – 24MHz Crystals)
PIN DESCRIPTIONS

Name	Number	Type	Description
VDD	1,2,16	P	+3.3V Power supply connectors.
XIN	3	I	Crystal input pin.
XOUT	4	I	Crystal output pin.
OE	5	I	Output enable input pin. Disables (tri-state) output when low. Internal pull-up enables output by default if pin is not connected to low.
N/C	6	-	Not connected.
GND	7,8,9,10	P	GND Power connectors.
GND_BUF	11,15	P	GND connector for output buffers.
CLK	12	O	True clock output pin.
VDD_BUF	13	P	+3.3V Power supply connector for output buffers.
CLKB	14	O	Complementary clock output pin.

ELECTRICAL SPECIFICATIONS
1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		7	V
Input Voltage, dc	V_I	$V_{SS}-0.5$	$V_{DD}+0.5$	V
Output Voltage, dc	V_O	$V_{SS}-0.5$	$V_{DD}+0.5$	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature	T_A	0	70	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
Input Static Discharge Voltage Protection			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

192MHz – 384MHz Low Phase Noise LVDS XO (12 – 24MHz Crystals)
2. Crystal Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Resonator Frequency	F_{XIN}	Parallel Fundamental Mode	12		24	MHz
Crystal Loading Rating	C_L (xtal)			TBD		pF
Recommended ESR	R_E	AT cut			30	Ω

3. General Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic (with Loaded Outputs)	I_{DD}	LVDS			60	mA
Operating Voltage	V_{DD}		3.13		3.47	V
Output Clock Duty Cycle		@ 1.25V (LVDS)	45	50	55	%
Short Circuit Current				± 50		mA

4. Jitter and Phase Noise specification

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Period jitter RMS	With capacitive decoupling between VDD and GND.		7		ps
Accumulated jitter RMS	With capacitive decoupling between VDD and GND. Over 10,000 cycles.		11		ps
Phase Noise relative to carrier	311MHz @100Hz offset		-90		dBc/Hz
Phase Noise relative to carrier	311MHz @1kHz offset		-114		dBc/Hz
Phase Noise relative to carrier	311MHz @10kHz offset		-134		dBc/Hz
Phase Noise relative to carrier	311MHz @100kHz offset		-134		dBc/Hz

192MHz – 384MHz Low Phase Noise LVDS XO (12 – 24MHz Crystals)
5. LVDS Electrical Characteristics

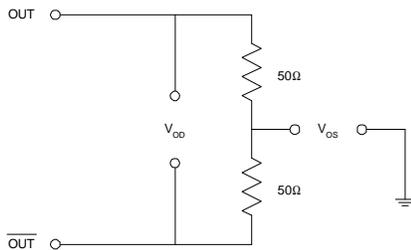
PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Differential Voltage	V_{OD}	$R_L = 100 \Omega$ (see figure)	247	355	454	mV
V_{DD} Magnitude Change	ΔV_{OD}		-50		50	mV
Output High Voltage	V_{OH}			1.4	1.6	V
Output Low Voltage	V_{OL}		0.9	1.1		V
Offset Voltage	V_{OS}		1.125	1.2	1.375	V
Offset Magnitude Change	ΔV_{OS}		0	3	25	mV
Power-off Leakage	I_{OXD}	$V_{out} = V_{DD}$ or GND $V_{DD} = 0V$		± 1	± 10	μA
Output Short Circuit Current	I_{OSD}			-5.7	-8	mA

192MHz – 384MHz Low Phase Noise LVDS XO (12 – 24MHz Crystals)

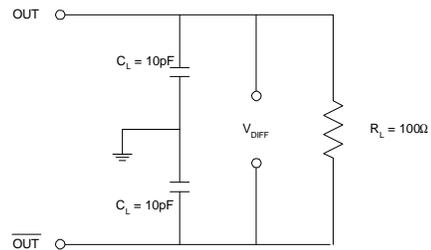
6. LVDS Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Clock Rise Time	t_r	$R_L = 100 \Omega$ $C_L = 10 \text{ pF}$ (see figure)	0.2	0.7	1.0	ns
Differential Clock Fall Time	t_f		0.2	0.7	1.0	ns

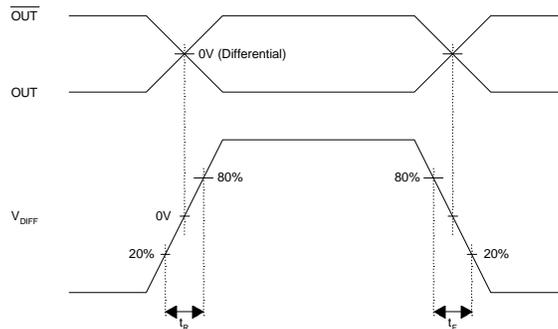
LVDS Levels Test Circuit



LVDS Switching Test Circuit



LVDS Transistion Time Waveform



192MHz – 384MHz Low Phase Noise LVDS XO (12 – 24MHz Crystals)

PACKAGE INFORMATION

Symbol	SOIC		TSSOP	
	Min.	Max.	Min.	Max.
A	1.35	1.75	-	1.20
A1	0.10	0.25	0.05	0.15
B	0.33	0.51	0.19	0.30
C	0.19	0.25	0.09	0.20
D	9.80	10.00	4.90	5.10
E	3.80	4.00	4.30	4.50
H	5.80	6.20	6.40 BSC	
L	0.40	1.27	0.45	0.75
e	1.27 BSC		0.65 BSC	

ORDERING INFORMATION

For part ordering, please contact our Sales Department:
 47745 Fremont Blvd., Fremont, CA 94538, USA
 Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:
 Device number, Package type and Operating temperature range

PLL602-14 S C XX

PART NUMBER _____

- _____ REVISION CODE (when applicable)
- _____ TEMPERATURE
 C=COMMERCIAL
 M=MILITARY
 I=INDUSTRIAL
- _____ PACKAGE TYPE
 S=SOIC. O=TSSOP

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