

Low Phase Noise XO with multipliers (for HF Fund. and 3rd O.T.)

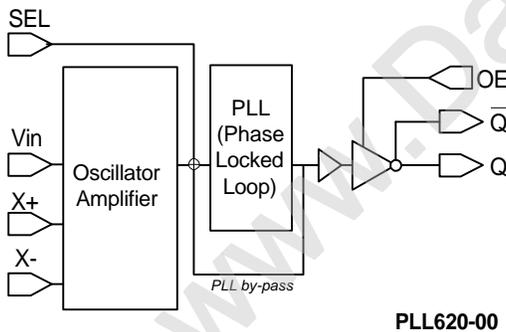
FEATURES

- 100MHz to 200MHz Fundamental Mode Crystal.
- Output range: 100 – 200MHz (no multiplication), 200 – 400MHz (2x multiplier) or 400 – 700MHz (4x multiplier).
- High yield design support up to 2pF string capacitance at 200MHz.
- Available outputs: PECL, LVDS, or CMOS.
- Supports 3.3V-Power Supply.
- Available in die form.
- Thickness 10 mil.

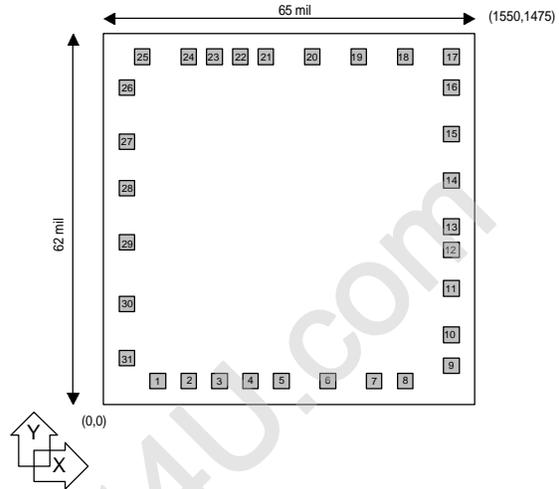
DESCRIPTIONS

PLL620-00 is an XO IC specifically designed to work with high frequency fundamental and third overtone crystals. Its design was optimized to tolerate higher limits of interelectrodes capacitance and bonding capacitance to improve yield. It achieves very low current into the crystal resulting in better overall stability. It is ideal for XO applications requiring LVDS or PECL output levels at high frequencies.

BLOCK DIAGRAM



DIE CONFIGURATION



DIE SPECIFICATIONS

Name	Value
Size	62 x 65 mil
Reverse side	GND
Pad dimensions	80 micron x 80 micron
Thickness	10 mil

OUTPUT SELECTION AND ENABLE

Pad #18 OUTSEL1	Pad #25 OUTSEL0	Selected Output
0	0	High Drive CMOS
0	1	Standard CMOS
1	0	LVDS
1	1	PECL (default)

OE_SELECT (Pad #9)	OE_CTRL (Pad #30)	State
0	0	Tri-state
	1 (Default)	Output enabled
1 (Default)	0 (Default)	Output enabled
	1	Tri-state

Pad #9: Bond to GND to set to '0'; bond to VDD to set to '1'
 Pad #30: Logical states defined by PECL levels if OE_SELECT (pad #9) is '1'
 Logical states defined by CMOS levels if OE_SELECT is '0'

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FREQUENCY SELECTION TABLE

Pad #28 SEL3	Pad #29 SEL2	Pad #19 SEL1	Pad #20 SEL0	Selected Multiplier
1	0	1	1	Fin x 4
1	1	1	0	Fin x 2
1	1	1	1	No multiplication (no PLL)

All pads have internal pull-ups (default value is 1). Bond to GND to set to 0.

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		7	V
Input Voltage, dc	V_I	$V_{SS}-0.5$	$V_{DD}+0.5$	V
Output Voltage, dc	V_O	$V_{SS}-0.5$	$V_{DD}+0.5$	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*	T_A	-40	85	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
Input Static Discharge Voltage Protection			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

* **Note:** Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for INDUSTRIAL grade only.

2. Crystal Specifications

Name	Symb.	Conditions	Min.	Max.	Units
Parallel Resonant mode		Fund. Or 3 rd Overtone			N/A
Load capacitance (capacitance on built-in on die seen by crystal)	C_L	Die only, no bond wire, no package		3.2	pF
Inter-electrode capacitance	C_0			2	pF
Oscillation Frequency		Fund. Or 3 rd Overtone	120	200	MHz

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3. General Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current (Loaded Outputs)	I _{DD}	PECL/LVDS/CMOS			100/80/40	mA
Operating Voltage	V _{DD}		3.13		3.47	V
Output Clock Duty Cycle		@ 1.4V (CMOS) @ 1.25V (LVDS) @ V _{dd} - 1.3V (PECL)	45 45 45	50 50 50	55 55 55	%
Short Circuit Current				±50		mA

4. Jitter specifications

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Period jitter RMS	At 155.52MHz, with capacitive decoupling between VDD and GND.		4		ps
Period jitter peak-to-peak			25		
Accumulated jitter RMS	At 155.52MHz, with capacitive decoupling between VDD and GND. Over 10,000 cycles.		7*		ps
Accumulated jitter peak-to-peak			45*		
Integrated jitter RMS at 155MHz	Integrated 12 kHz to 20 MHz		0.3		ps

*: To be measured

Note: Higher Q factor of 3rd overtone crystals will result in even better jitter performance.

5. Phase noise specifications

PARAMETERS	FREQUENCY	@ 10Hz	@ 100Hz	@ 1kHz	@ 10kHz	@ 100kHz	UNITS
Phase Noise vs. carrier with fund. crystal.	155.52MHz	-75	-95	-125	-140	-145	dBc/Hz
	622.08MHz	-75	-95	-110	-125	-120	

*: To be measured

Note: Higher Q factor of 3rd overtone crystals will result in even better phase noise performance.

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6. CMOS Output Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output High Voltage	V_{OH}	$I_{OH} = -12\text{mA}$ (Standard drive)	2.4			V
Output Low Voltage	V_{OL}	$I_{LO} = 12\text{mA}$ (Standard drive)			0.4	V
Output High Voltage at CMOS level	V_{OHC}	$I_{OH} = -4\text{mA}$ (Standard drive)	$V_{DD} - 0.4$			V
Output drive current		At TTL level (High drive)	36	51		mA
		At TTL level (Standard drive)	12	17		mA

7. CMOS Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Clock Rise/Fall Time (Standard Drive)		0.8V ~ 2.0V with 10 pF load		1.15		ns
		0.3V ~ 3.0V with 15 pF load		3.7		
Output Clock Rise/Fall Time (High Drive)		0.8V ~ 2.0V with 10 pF load		0.5		
		0.3V ~ 3.0V with 15 pF load		1.5		

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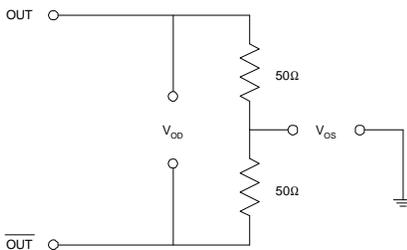
8. LVDS Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Differential Voltage	V_{OD}	$R_L = 100 \Omega$ (see figure)	247	355	454	mV
V_{DD} Magnitude Change	ΔV_{OD}		-50		50	mV
Output High Voltage	V_{OH}			1.4	1.6	V
Output Low Voltage	V_{OL}		0.9	1.1		V
Offset Voltage	V_{OS}		1.125	1.2	1.375	V
Offset Magnitude Change	ΔV_{OS}		0	3	25	mV
Power-off Leakage	I_{OXD}	$V_{out} = V_{DD}$ or GND $V_{DD} = 0V$		± 1	± 10	μA
Output Short Circuit Current	I_{OSD}			-5.7	-8	mA

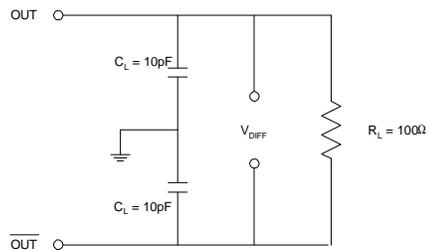
9. LVDS Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Clock Rise Time	t_r	$R_L = 100 \Omega$ $C_L = 10 \text{ pF}$ (see figure)	0.2	0.7	1.0	ns
Differential Clock Fall Time	t_f		0.2	0.7	1.0	ns

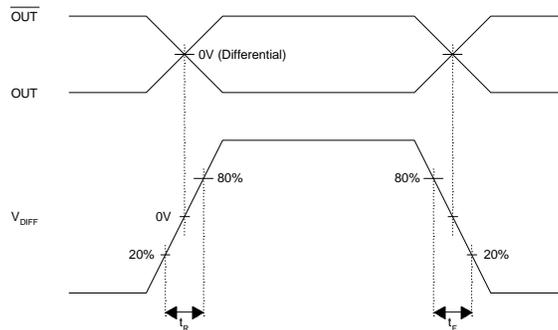
LVDS Levels Test Circuit



LVDS Switching Test Circuit



LVDS Transition Time Waveform



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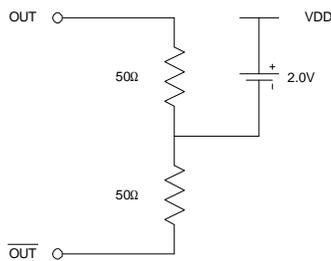
10. PECL Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	MAX.	UNITS
Output High Voltage	V_{OH}	$R_L = 50 \Omega$ to $(V_{DD} - 2V)$ (see figure)	$V_{DD} - 1.025$		V
Output Low Voltage	V_{OL}			$V_{DD} - 1.620$	V

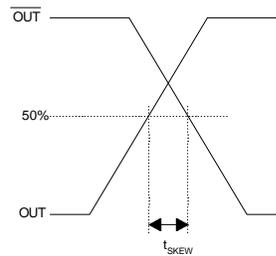
11. PECL Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Clock Rise Time	t_r	@20/80% - PECL		0.6	1.5	ns
Clock Fall Time	t_f	@80/20% - PECL		0.5	1.5	ns

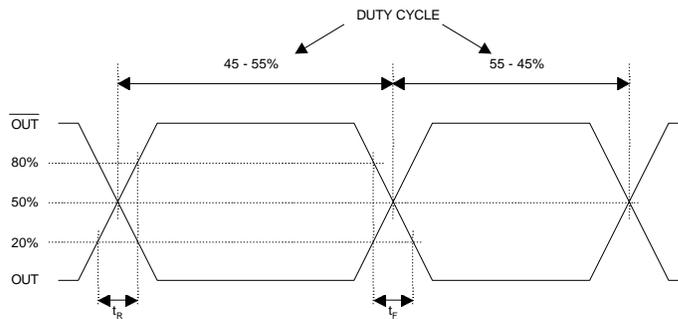
PECL Levels Test Circuit



PECL Output Skew



PECL Transition Time Waveform



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PAD ASSIGNMENT

Pad #	Name	X (μm)	Y (μm)
1	GND	248	109
2	GND	361	109
3	GND	473	109
4	GND	587	109
5	GND	702	109
6	N/C	874	109
7	GND	1042	109
8	GNDBUF	1171	109
9	OE_SELECT	1400	125
10	LVDS	1400	259
11	PECL	1400	476
12	VDDBUF	1400	616
13	VDDBUF	1400	716
14	PECLB	1400	871
15	LVDSB	1400	1089
16	CMOS	1400	1227
17	GNDBUF	1389	1365
18	OUTSEL1	1232	1365
19	SEL1	1042	1365
20	SEL0	854	1365
21	VDD	659	1365
22	VDD	559	1365
23	VDD	459	1365
24	VDD	358	1365
25	OUTSEL0	194	1365
26	XIN	109	1223
27	XOUT	109	1017
28	SEL3	109	858
29	SEL2	109	646
30	OE_CTRL	109	397
31	N/C	109	181

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ORDERING INFORMATION

For part ordering, please contact our Sales Department:

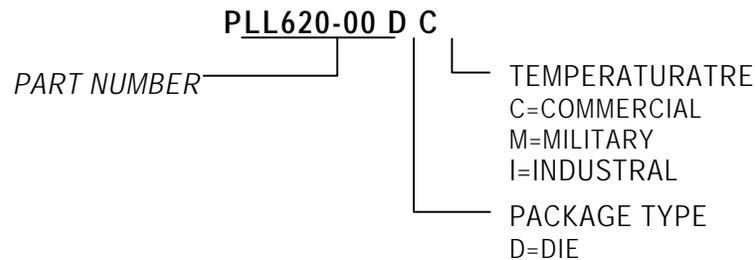
47745 Fremont Blvd., Fremont, CA 94538, USA

Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:

Device number, Package type and Operating temperature range



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