Low Phase Noise XO (for 27-65MHz Fund. Or 3rd O.T. Crystals)

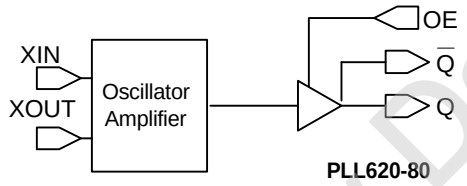
FEATURES

- 27MHz to 65MHz Fundamental or 3rd overtone Crystal.
- Output range: 27MHz – 65MHz (no PLL).
- Complementary outputs: CMOS, PECL or LVDS.
- Selectable OE Logic (enable high or enable low).
- Integrated variable capacitors.
- Supports 3.3V-Power Supply.
- Available in die form.
- Thickness 10 mil.

DESCRIPTIONS

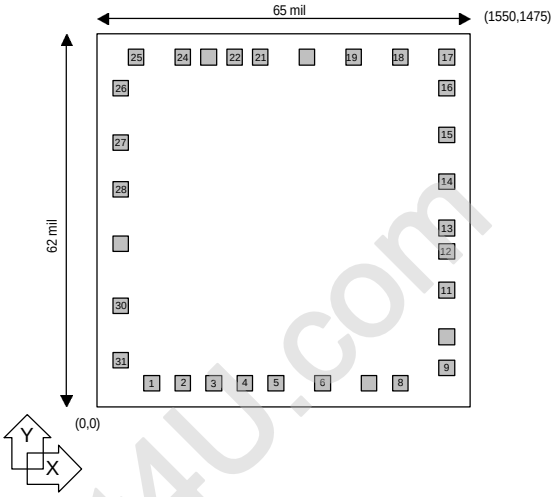
PLL620-80 is an XO IC specifically designed to work with crystals between 27MHz and 65MHz. It accepts fundamental crystals, and also 3rd overtone crystals (requires external resistor). It achieves very low current into the crystal resulting in better overall stability. It features a selectable OE logic, as well as selectable output buffers (CMOS, LVDS or PECL).

BLOCK DIAGRAM



PLL620-80

DIE CONFIGURATION



SPECIFICATIONS

	Value
Size	
Reverse side	GND
	80 micron x 80 micron
Thickness	

OUTPUT SELECTION AND ENABLE

Pad #18	Pad #25 OUTSEL0	
0	0	
0	1	
1	0	
1	1	(default)

OE_SELECT (Pad #9)	OE_CTRL (Pad #30)	State
0	0	Tri-state
	1 (Default)	Output enabled
1 (Default)	0 (Default)	Output enabled
	1	Tri-state

Pad #9, 18, 25: Bond to GND to set to "0", bond to VDD to set to "1".
No connection results to "default"setting through internal pull-up/-down.
Pad #30: Logical states defined by PECL levels if OE_SELECT (pad #9) is "1"
Logical states defined by CMOS levels if OE_SELECT is "0"

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		7	V
Input Voltage, dc	V_I	V_{SS}-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	V_{SS}-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*	T_A	-40	85	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
Input Static Discharge Voltage Protection			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

* **Note**: Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for INDUSTRIAL grade only.

2. Crystal Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Resonator Frequency	F_{XIN}	Fundamental or 3rd overtone*	27		65	MHz
Crystal Loading Rating	$C_{L\ (xtal)}$	Die		4		pF
Interelectrode Capacitance	C_0				5	pF
Recommended ESR	R_E	AT cut			30	Ω

*** Note**: 3rd overtone crystals require an external resistor between XIN and XOUT to prevent the fundamental from oscillating.

3. General Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current (Loaded Outputs)	I_{DD}	PECL/LVDS			100/80/40	mA
Operating Voltage	V_{DD}		3.13		3.47	V
Output Clock Duty Cycle		@ 1.25V (LVDS) @ Vdd – 1.3V (PECL)	45 45	50 50	55 55	%
Short Circuit Current				±50		mA

4. Jitter specifications

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Period jitter RMS at 27MHz	With capacitive decoupling between VDD and GND. Over 10,000 cycles		2.3		ps
Period jitter peak-to-peak at 27MHz			18.5	20	
Accumulated jitter RMS at 27MHz	With capacitive decoupling between VDD and GND. Over 1,000,000 cycles.		2.3		ps
Accumulated jitter peak-to-peak at 27MHz			24	25	
Random Jitter	"RJ" measured on Wavecrest SIA 3000		2.3		ps

Measured on Wavecrest SIA 3000

5. Phase noise specifications

PARAMETERS	FREQUENCY	@10Hz	@100Hz	@1kHz	@10kHz	@100kHz	UNITS
Phase Noise relative to carrier	27MHz	-75	-100	-125	-140	-145	dBc/Hz

Note: Phase Noise measured on Agilent E5500

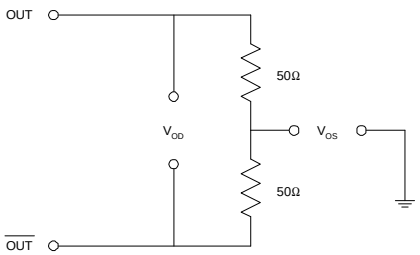
6. LVDS Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Differential Voltage	V_{OD}	R_L = 100 Ω (see figure)	247	355	454	mV
V_{DD} Magnitude Change	ΔV_{OD}		-50		50	mV
Output High Voltage	V_{OH}			1.4	1.6	V
Output Low Voltage	V_{OL}		0.9	1.1		V
Offset Voltage	V_{OS}		1.125	1.2	1.375	V
Offset Magnitude Change	ΔV_{OS}		0	3	25	mV
Power-off Leakage	I_{OXD}	V_{out} = V_{DD} or GND, V_{DD} = 0V		±1	±10	uA
Output Short Circuit Current	I_{OSD}			-5.7	-8	mA

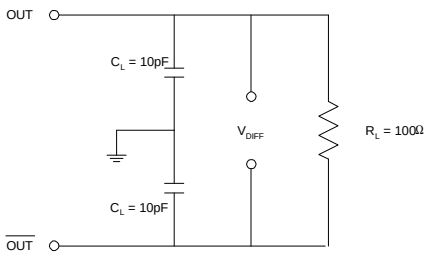
7. LVDS Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Clock Rise Time	t_r	R_L = 100 Ω, C_L = 10 pF (see figure)	0.2	0.7	1.0	ns
Differential Clock Fall Time	t_f		0.2	0.7	1.0	ns

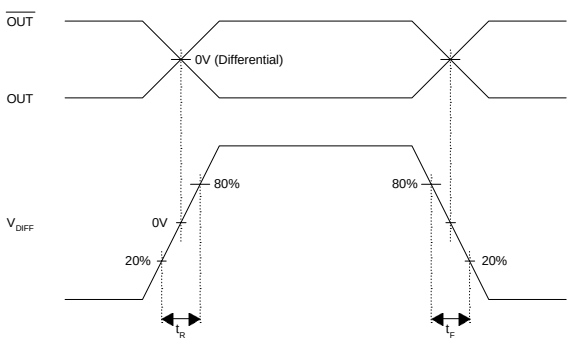
LVDS Levels Test Circuit



LVDS Switching Test Circuit



LVDS Transistion Time Waveform



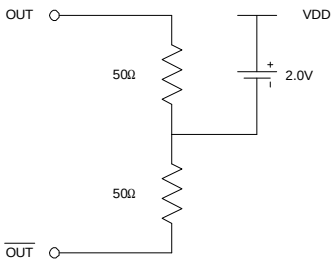
8. PECL Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	MAX.	UNITS
Output High Voltage	V_{OH}	R_L = 50 Ω to (V_{DD} – 2V) (see figure)	V_{DD} – 1.025		V
Output Low Voltage	V_{OL}			V_{DD} – 1.620	V

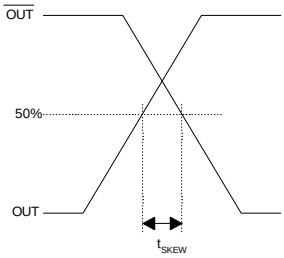
9. PECL Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Clock Rise Time	t_r	@20/80% - PECL		0.6	1.5	ns
Clock Fall Time	t_f	@80/20% - PECL		0.5	1.5	ns

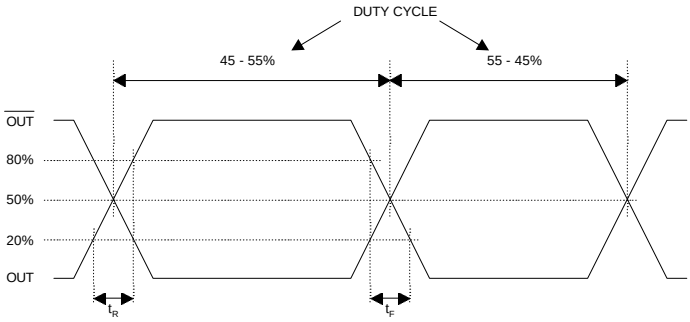
PECL Levels Test Circuit



PECL Output Skew



PECL Transistion Time Waveform



PAD ASSIGNMENT

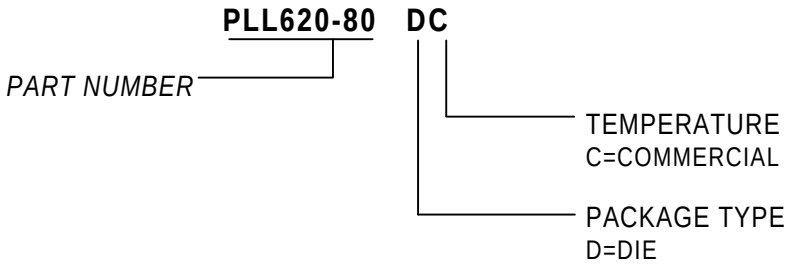
Pad #	Name	X (µm)	Y (µm)
1	GND	248	109
2	GND	361	109
3	GND	473	109
4	GND	587	109
5	GND	702	109
6	N/C	874	109
7	GND	1042	109
8	GNDBUF	1171	109
9	OE_SELECT	1400	125
10	LVDS	1400	259
11	PECL	1400	476
12	VDDBUF	1400	616
13	VDDBUF	1400	716
14	PECLB	1400	871
15	LVDSB	1400	1089
16	CMOS	1400	1227
17	GNDBUF	1389	1365
18	OUTSEL1	1232	1365
19	*Reserved*	1042	1365
20	*Not connected*	854	1365
21	VDD	659	1365
22	VDD	559	1365
23	VDD	459	1365
24	VDD	358	1365
25	OUTSEL0	194	1365
26	XIN	109	1223
27	XOUT	109	1017
28	*Not connected*	109	858
29	*Not connected*	109	646
30	OE_CTRL	109	397
31	*Not connected*	109	181

Note: for optimal Phase Noise performance, it is recommended to bond all optional VDD and GND pads.

ORDERING INFORMATION

PART NUMBER

The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range



Order Number	Marking	Package Option
PLL620-80DC	PLL620-80DC	Die – Waffle Pack