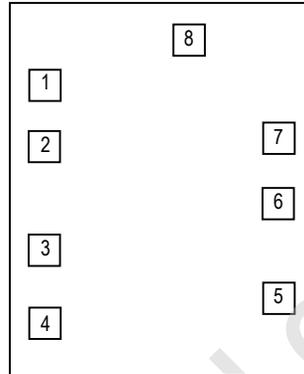


Ultra Low Current XO (Crystals from 10 MHz to 52 MHz)

FEATURES

- Low phase noise (-130 dBc @ 10kHz offset at 30MHz).
- CMOS output with OE tri-state control.
- Selectable oscillator “on” or “off” feature in output disable mode
- Ultra Low current consumption (<2.5mA, <2mA, <1.3mA at 27MHz respectively for PLL600-10, PLL600-20, and PLL600-30)
- Ultra Low disable mode current (<2uA when disabled with osc. off)
- 10 to 52MHz fundamental crystal input.
- Selectable divider by 2 (PLL600-10 only).
- 12mA drive capability at TTL output.
- Low jitter (RMS): 2.5ps period jitter.
- 2.25V to 3.63V DC operation.
- Available in die (fits 5x3.2 low profile substrate).

PAD LAYOUT



SELECTION TABLE

SEL (PLL600-10)	DIVIDER
0	/ 2
1	No division

Internal Pull-up, default value is '1' when not connected.
Selectable divider available on P600-10 only.

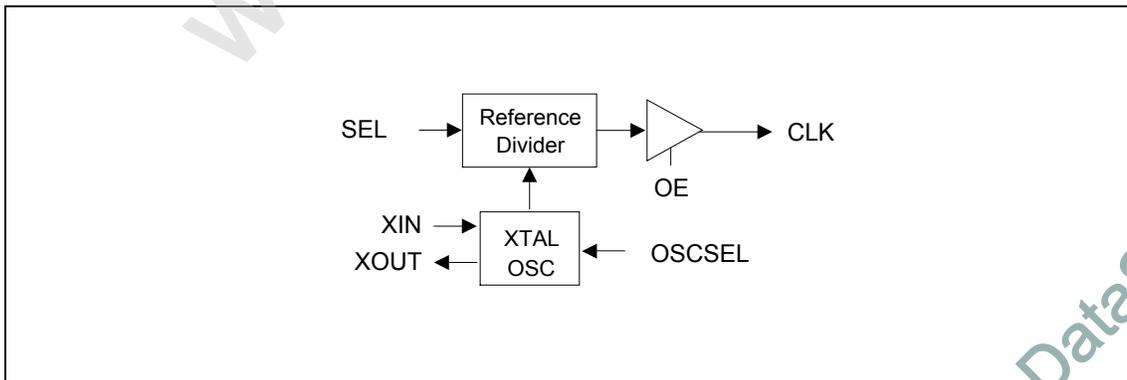
OE	OSCSEL	OUTPUT
0	0	Disabled Osc. Off
0	1	Disabled Osc. On
1	0	Enabled
1	1	Enabled

Internal Pull-up, default value is '1' when not connected.

DESCRIPTION

The PLL600-10/-20/-30 form a low cost family of XO dies, designed to consume the lowest current on the market for the 5MHz to 52MHz range. It accepts input crystal from 10 to 52MHz (fundamental resonant mode) and offers (PLL600-10 only) a selectable divider by 2 or no division. Providing less than -130dBc at 10kHz offset at 30MHz, and with a very low jitter (2.5 ps RMS period jitter) makes this chip ideal for applications requiring low current frequency sources, such as handheld devices.

BLOCK DIAGRAM



Ultra Low Current XO (Crystals from 10 MHz to 52 MHz)
PAD DESCRIPTION

Name	Number	Type	Description
XOUT	1	I	Crystal output pin.
SEL	2	I	PLL600-10 only: select pin. See Selection Table on page 1. PLL600-20/-30: no connect
GND	3	P	Output Enable input pin. Tri-states output if low. Enables output if high.
OSCSEL	4	I	Disable mode (on or off) select pin. See Selection Table on page 1.
CLK	5	O	Output clock pin.
VDD	6	P	+3.3V VDD power supply pin.
OE	7	I	Output Enable input pin. Tri-states output if low. Enables output if high.
XIN	8	I	Crystal input pin.

See also pad coordinates table at the end of this document.

SEL and OSCSEL have internal pull-ups, so the default value is '1' when not connected.

ELECTRICAL SPECIFICATIONS
1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage Range	V_{CC}	-0.5	7	V
Input Voltage Range	V_I	-0.5	$V_{CC}+0.5$	V
Output Voltage Range	V_O	-0.5	$V_{CC}+0.5$	V
Soldering Temperature			260	°C
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*		-40	85	°C

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

Note: Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for INDUSTRIAL grade only.

Ultra Low Current XO (Crystals from 10 MHz to 52 MHz)
2. AC Electrical Specifications

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Crystal Frequency		10		52	MHz
Settling time	At power-up (Vdd reaches 2.2V)		10*		ms
	Disable to enable, osc. Off		10*		ms
	Disable to enable, osc. On			500*	μs
Output Clock Rise/Fall Time	0.8V ~ 2.0V with 10 pF load		1.15		ns
	0.3V ~ 3.0V with 15 pF load		3.7		
VDD sensitivity	Frequency vs. VDD +/- 10%	0.8		0.8	ppm
Output Clock Duty Cycle	Measured @ 1.4V	45	50	55	%
Short Circuit Current			±50		mA

Note: (*) Preliminary Specifications still to be characterized.

3. Jitter and Phase Noise specification

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
RMS Period Jitter (1 sigma – 1000 samples)	with capacitive decoupling between VDD and GND.		2.1	2.5	ps
Phase Noise relative to carrier	30MHz @100Hz offset		-80		dBc/Hz
Phase Noise relative to carrier	30MHz @1kHz offset		-110		dBc/Hz
Phase Noise relative to carrier	30MHz @10kHz offset		-130		dBc/Hz
Phase Noise relative to carrier	30MHz @100kHz offset		-138		dBc/Hz
Phase Noise relative to carrier	30MHz @1MHz offset		-145		dBc/Hz

Ultra Low Current XO (Crystals from 10 MHz to 52 MHz)
4. DC Specification

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic, with Loaded Outputs (at VDD = 3.3V) Respectively for PLL600-10/-20/-30	I _{DD}	At 10MHz, Cload=15pF		1.3 / 1 / 0.75	1.4 / 1.1 / 0.9	mA
		At 13.5MHz, Cload=15pF		1.5 / 1.2 / 0.8	1.6 / 1.3 / 1	
		At 17.7MHz, Cload=15pF		1.8 / 1.5 / 1	1.9 / 1.6 / 1.1	
		At 27MHz, Cload=15pF		2.4 / 2 / 1.2	2.5 / 2.1 / 1.3	
		At 48MHz, Cload=15pF		4.1 / 3.5 / 2.1	4.2 / 3.6 / 2.2	
Supply Current in tri-state	I _{DD}	Output disabled, Osc. off		2	4	μA
		Output disabled, Osc. On (PLL600-10)			620	μA
		Output disabled, Osc. On (PLL600-20/-30)			520	
Operating Voltage	V _{DD}		2.25		3.63	V
Output High Voltage	V _{OH}	I _{OH} = -12mA*	2.4			V
		PLL600-30*, I _{OH} = -12mA*	2.4	2.9		V
Output Low Voltage	V _{OL}	I _{LO} = 12mA*			0.4	V
		PLL600-30*, I _{OH} = -12mA*		0.32	0.4	V
Output High Voltage at CMOS level	V _{OHc}	I _{OH} = -4mA	V _{DD} - 0.4			V
Output drive current		At TTL level	12	17		mA
Short Circuit Current				±50		mA
ESD Protection		Human Body Model	3000			

* Note: PLL600-30 has non-standard CMOS VOH and VOL levels for lower current consumption, but meet CMOS input stages needs. PLL600-30 should be used to drive pure capacitive loads only.

5. Crystal Specifications

PARAMETERS	SYMBOL	MIN.	TYP.	MAX.	UNITS
Crystal Resonator Frequency	F _{XIN}	10		52	MHz
Crystal Loading Rating	C _{L (xtal)}		8.5		pF
Maximum Sustainable Drive Level				200	μW
Operating Drive Level			50		μW
C0 (for frequencies below 30MHz)				5	pF
C0 (for frequencies above 30MHz)				4	pF
ESR	R _s			30	Ω

Note: A detailed crystal specification document is also available for this part

Ultra Low Current XO (Crystals from 10 MHz to 52 MHz)

PAD ASSIGNMENT

Pad #	Name	X (μm)	Y (μm)
1	XOUT	94.183	768.599
2	SEL	94.157	605.029
3	GND	94.183	331.756
4	OSCSEL	94.193	140.379
5	CLK	715.472	203.866
6	VDD	715.307	455.726
7	SEL	715.472	626.716
8	XIN	476.906	888.881

Die dimensions and reference coordinates in μm excluding scribe lines:

Lower left: X=0, Y=0
Upper right: X=812, Y=986

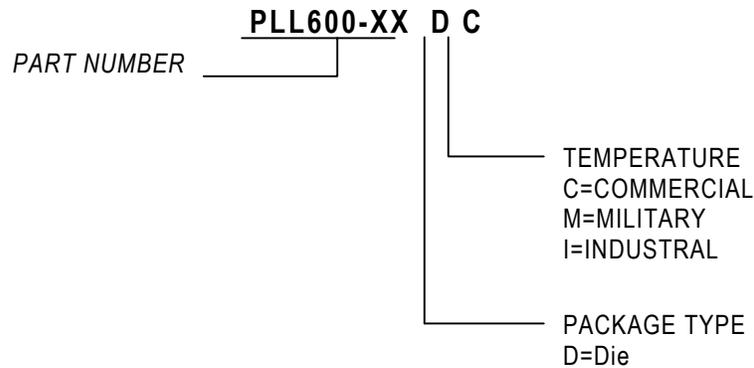
ORDERING INFORMATION

For part ordering, please contact our Sales Department:

47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range



PhaseLink Corporation, reserves the right to make changes in its products or specifications, or both at any time without notice. The information furnished by Phaselink is believed to be accurate and reliable. However, Phaselink makes no guarantee or warranty concerning the accuracy of said information and shall not be responsible for any loss or damage of whatever nature resulting from the use of, or reliance upon this product.

LIFE SUPPORT POLICY: PhaseLink's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of PhaseLink Corporation.