

# OKI Semiconductor

**FEDL6948\_6948V-02**

Issue Data: Jun 8, 2005

## MSM6948/6948V

**1200 bps Single Chip MSK Modem**

### GENERAL DESCRIPTION

The MSM6948/6948V is a single chip MSK (Minimum Shift Keying) modem which is fabricated by Oki's low power consumption CMOS silicon gate technology.

The demodulator receives the data to be transmitted (SD) synchronized with the transmit timing clock (ST) generated by the on-chip clock generator. The signal, which is modulated by MSK method, is output.

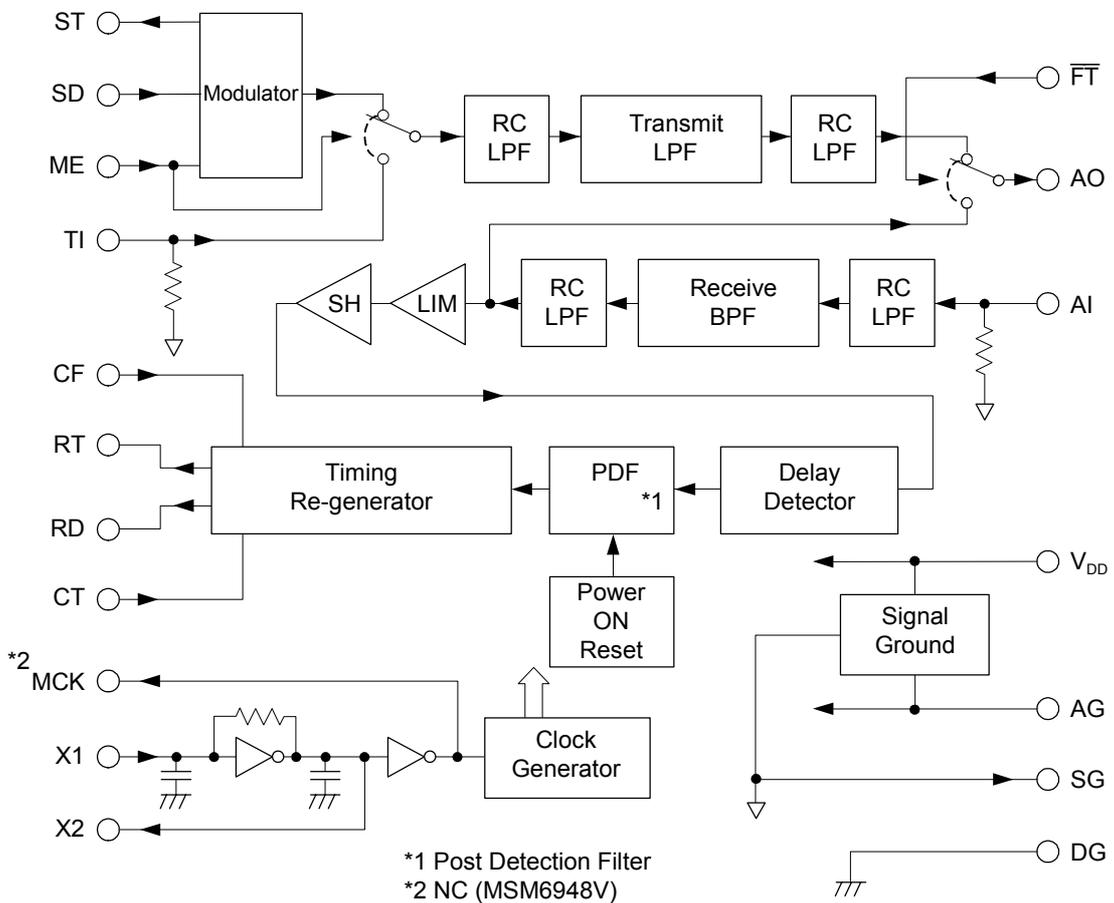
The demodulator converts the received MSK signal to the received data (RD) by means of a delay detection technique after limiting the band of the received MSK signal. This signal is input to the digital PLL and the re-generated timing clock (RT) is output from the demodulator, synchronized with the RD.

### FEATURES

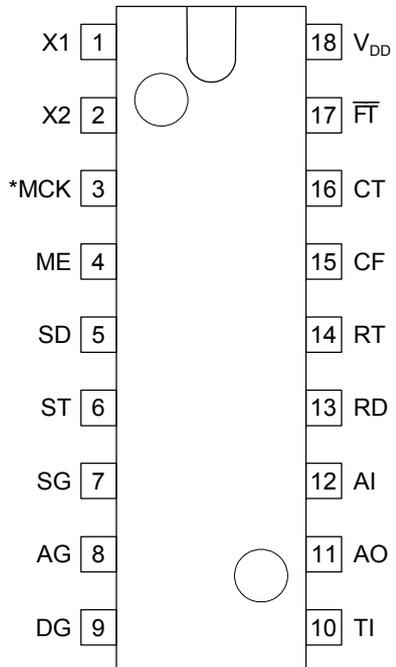
- Signal power supply: +5 V
- On-chip SCF (Switched Capacitor Filter)
- The transmit filter can be also used as voice splatter filter.
- The receive timing re-generator has two different lock-in time performance options to be chosen from.
- Built-in crystal oscillation circuit
- Small number of external components for easy application
- Wide application-wireless data equipment, MCA system
- Low power consumption CMOS
- Package options:

18-pin plastic DIP	(DIP18-P-300-2.54)	(Product name: MSM6948RS)
24-pin plastic SOP	(SOP24-P-430-1.27-K)	(Product name: MSM6948GS-K)

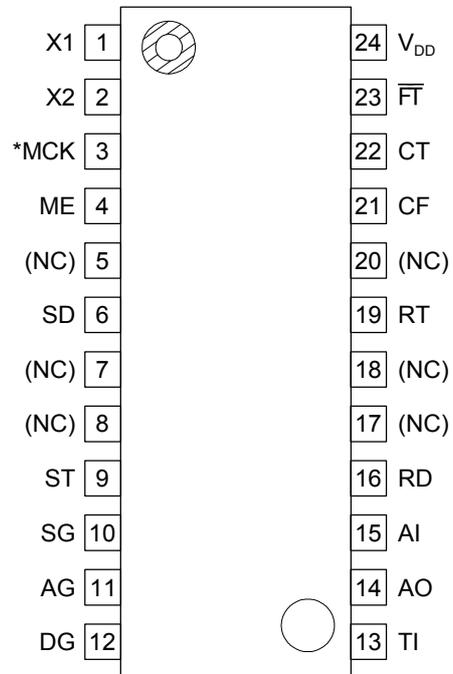
**BLOCK DIAGRAM**



**PIN CONFIGURATION (TOP VIEW)**



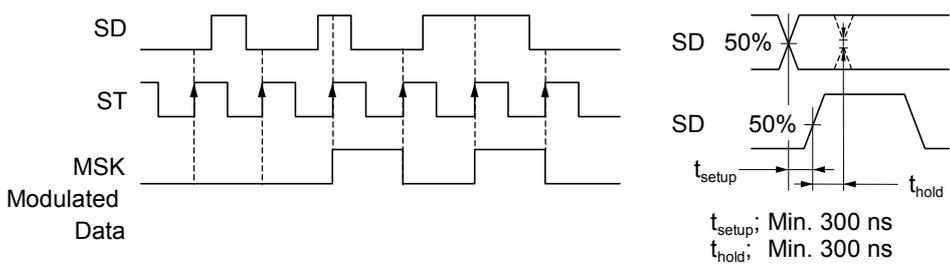
18-Pin Plastic DIP



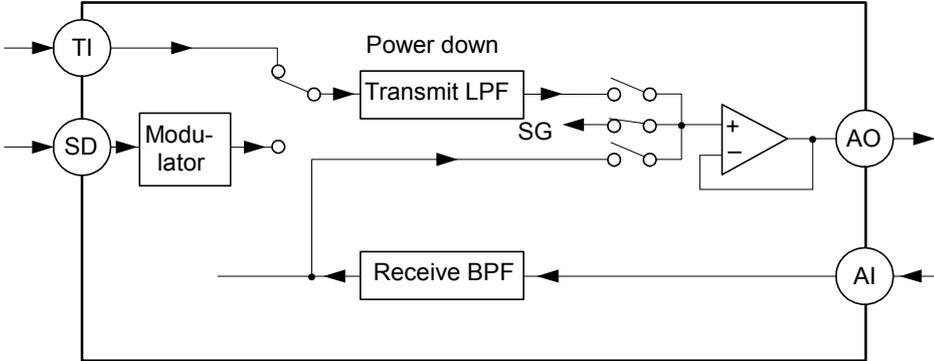
24-Pin Plastic SOP

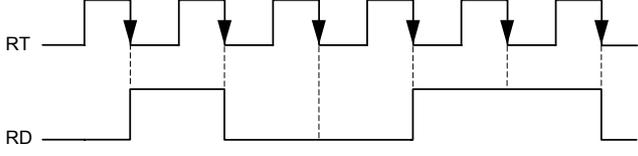
\* NC (MSM6948V)  
 NC: No connect pin

## PIN DESCRIPTION

Name	Description
X1	Crystal connection pins. A 3.6864 MHz crystal shall be connected.
X2	When an external clock is applied for MSM6948's oscillation source, it has to be input to X2. In this case, X2 has to be AC-coupled by the capacitor of 200 pF. X1 shall be left open.
*MCK	3.6864 MHz $\pm$ 0.02% clock output. This can be used for other devices under limited load conditions.
ME	When digital "1" is put on this pin, MSK modulator output is connected to the input of transmit LPF. When digital "0" is put on, the input of transmit LPF is connected to TI that is voice signal input. The data put on ME terminal is synchronized with the rising edge of ST and input to internal logic as a control data. The rising edge of this synchronized data resets MSK modulator.
SD	<p>Transmit data input. The data on this pin is synchronized with the rising edge of ST and input to MSK modulator as an actual transmit data.</p>  <p> <math>t_{\text{setup}}</math>: Min. 300 ns  <math>t_{\text{hold}}</math>: Min. 300 ns </p>
ST	ST is synchronizing signal used for ME and SD. This is made from master clock and is usually 1200 Hz.
SG	Built-in analog signal ground. The DC voltage is approximately half of $V_{DD}$ , so the analog signals of AI, AO, and TI interfaces with peripheral circuits which must be implemented by AC-coupling. To make this voltage source impedance lower and ensure the device performance, it is necessary to put a bypass capacitor on SG in close physical proximity to the device.
AG	Analog ground. This pin should be common with DG at the system ground point as close as possible.

\*NC: MSM6948V

Name	Description																		
DG	Digital ground. This pin should be common with AG at the system ground point as close as possible.																		
TI	Voice signal input. The signal input to this pin can be sent out to AO through the transmit LPF, the characteristics of which, gives the splatter filter for voice band signal. When this function is used, digital "0" must be input to ME. TI is biased internally to SG with about 100 kΩ.																		
AO	<p>Transmit analog signal output. According to the control data on ME and <math>\overline{FT}</math>, AO is set to various state as an output terminal as follows.</p> <table border="1" data-bbox="427 779 1326 1088"> <thead> <tr> <th><math>\overline{FT}</math></th> <th>ME</th> <th>Transmit LPF</th> <th>State of AO</th> </tr> </thead> <tbody> <tr> <td>"1"</td> <td>"1"</td> <td rowspan="2">Power On</td> <td>The output of Transmit LPF</td> </tr> <tr> <td>"1"</td> <td>"0"</td> <td>MSK Signal Voice Signal</td> </tr> <tr> <td>"0"</td> <td>"1"</td> <td rowspan="2">Power Down</td> <td>The Output of Receive BPF (Used for Device Test Only)</td> </tr> <tr> <td>"0"</td> <td>"0"</td> <td>No-signal Output (DC-biased to SG)</td> </tr> </tbody> </table>  <p>The state when <math>\overline{FT}</math> and ME = "0" is shown above. When the input digital data on <math>\overline{FT}</math> changes to "1" from "0", AO remains to be connected to SG during about 12 ms and after that, and AO is switched to transmit LPF. This delay time prevents AO from outputting meaningless signal during transient time from power down to on of LPF.</p>	$\overline{FT}$	ME	Transmit LPF	State of AO	"1"	"1"	Power On	The output of Transmit LPF	"1"	"0"	MSK Signal Voice Signal	"0"	"1"	Power Down	The Output of Receive BPF (Used for Device Test Only)	"0"	"0"	No-signal Output (DC-biased to SG)
$\overline{FT}$	ME	Transmit LPF	State of AO																
"1"	"1"	Power On	The output of Transmit LPF																
"1"	"0"		MSK Signal Voice Signal																
"0"	"1"	Power Down	The Output of Receive BPF (Used for Device Test Only)																
"0"	"0"		No-signal Output (DC-biased to SG)																
AI	Receive analog signal input. AI is biased internally to SG with about 100 kΩ same as TI. Receive BPF and demodulator extract the information in this signal and convert it into a serial data stream at RD output.																		

Name	Description						
RD	Demodulated serial data output. This data is synchronized with the re-generated timing clock RT.						
RT	Receive data timing clock output. This signal is re-generated by internal digital PLL. Synchronizing to falling edge of RT, RD is output. <div style="text-align: center;">  <p>Delay time (RT → RD) &lt; 300 ns</p> </div>						
CF	Receive data timing clock is re-generated by digital PLL of which phase correcting speed can be selected with CF. When a digital "1" is put on CF and phase difference between receive data timing and RT is more than 22.5 degree, phase correcting speed is high. In this case, as the phase difference enters within 22.5 degrees, that speed changes to low immediately. When digital "0" is input to CF, phase correcting speed of PLL remains low regardless of the phase difference. Usually, CF is connected to digital "1".						
CT	PLL's lock-in characteristics can be selected with CT. When digital "1" is put on CT, PLL requires max. 50-bit alternative data pattern. On the other hand, when digital "0" is input to CT, PLL can be locked in below 18-bit data. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Equipment</th> <th>CT</th> </tr> </thead> <tbody> <tr> <td>Personal/MCA wireless terminals</td> <td>"1"</td> </tr> <tr> <td>MCA wireless bases</td> <td>"0"</td> </tr> </tbody> </table>	Equipment	CT	Personal/MCA wireless terminals	"1"	MCA wireless bases	"0"
Equipment	CT						
Personal/MCA wireless terminals	"1"						
MCA wireless bases	"0"						
$\overline{FT}$	Control signal for the internal connection of AO. Refer to column AO. When digital "0" is input to this pin, transmit LPF enters in power down mode, but the output buffer operational amplifier remains active.						
V <sub>DD</sub>	+5 V power supply. This device is sensitive to supply noises as switched capacitor techniques are utilized. Bypass capacitors of more than 2.2 $\mu$ F between V <sub>DD</sub> and AG, and between V <sub>DD</sub> and DG are indispensable to ensure the performance.						

Note : The output from the RD-pin may be locked to logic '0' if the AIN-pin is input space or mark when this LSI is powered up. To avoid this, there shouldn't be either space or mark to the AIN-pin for 10ms or longer after the power up. The lock with the RD-pin, once it happens, can be released by inputting two bits of spaces in series to the AIN-pin.

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	$V_{DD}$	Ta = 25°C With respect to AG and DG	-0.3 to 7.0	V
Analog Input Voltage *1	$V_{IA}$		-0.3 to $V_{DD} + 0.3$	
Digital Input Voltage *2	$V_{ID}$		-0.3 to $V_{DD} + 0.3$	
Operating Temperature	$T_{op}$	—	-25 to 70	°C
Storage Temperature	$T_{STG}$	—	-55 to 150	

\*1 TI, AI

\*2 ME, SD, CF, CT,  $\overline{FT}$ **RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	$V_{DD}$	With respect to AG and DG	4.75	5	5.25	V
	AG, DG	—	—	0	—	
Operating Temperature	$T_{op}$	—	-25	25	70	°C
Crystal Resonant Frequency	$f_{XTAL}$	—	3.6860	3.6864	3.6868	MHz
Data Speed	$T_S$	—	—	1200	—	bit/sec
C1	—	—	—	2.2	—	μF
C2, C6	—	—	—	0.1	—	
C3	—	—	—	0.047	—	
C4	—	$R_{LX} \geq 100 \text{ k}\Omega$	—	0.01	—	
C5	—	—	—	0.047	—	
Crystal	Frequency Deviation	25 ±5°C	-100	—	+100	ppm
	Temperature Characteristics	At -40 to +85°C	-100	—	+100	
	Equivalent Series Resistance	—	—	—	100	Ω
	Load Capacitance	—	—	—	16	—

**ELECTRICAL CHARACTERISTICS****DC and Digital Interface Characteristics**(V<sub>DD</sub> = 5 V ±5%, Ta = -25 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Current	I <sub>DD</sub>	Normal Operating Mode	—	3	6	mA
Oscillating Frequency	f <sub>MCK</sub>	f <sub>X'TAL</sub> = 3.6864 MHz ±0.01%	3.6857	3.6864	3.6871	MHz
Input Leakage Current *1	I <sub>IL</sub>	V <sub>IN</sub> = 0 V	-10	—	10	μA
	I <sub>IH</sub>	V <sub>IN</sub> = V <sub>DD</sub>	-10	—	10	
Input Voltage *1	V <sub>IL</sub>	—	0	—	0.8	V
	V <sub>IH</sub>	—	2.2	—	V <sub>DD</sub>	
Output Voltage *2	V <sub>OL1</sub>	I <sub>OL</sub> = 1.6 mA	0	—	0.4	
	V <sub>OH1</sub>	I <sub>OH</sub> = 400 μA	0.8V <sub>DD</sub>	—	V <sub>DD</sub>	
Output Voltage *3	V <sub>OL2</sub>	R <sub>L</sub> > 50 kΩ	0	—	0.4	
	V <sub>OH2</sub>	C <sub>L</sub> < 20 pF	0.6V <sub>DD</sub>	—	V <sub>DD</sub>	

\*1 ME, SD, CF, CT,  $\overline{FT}$ 

\*2 ST, RD, RT

\*3 MCK (NC: MSM6948V)

**Analog Interface Characteristics**

Transmit signal output (AO)

(V<sub>DD</sub> = 5 V ±5%, Ta = -25 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Carrier Frequency	f <sub>M</sub>	SD = "1" $\overline{FT}$ = "1"	1199	1200	1201	Hz
	f <sub>S</sub>	SD = "0"      ME = "1"	1799	1800	1801	
Carrier Level	V <sub>OX</sub>	R <sub>L</sub> ≥ 100 kΩ C <sub>L</sub> ≤ 40 pF $\overline{FT}$ = "1" ME = "1"	-2	0	+2	dBm
Output Resistance	R <sub>OX</sub>	f <sub>AO</sub> ≤ 4 kHz	—	—	1	kΩ
Output Load Resistance	R <sub>LX</sub>	—	100	—	—	
Output Load Capacitance	C <sub>LX</sub>	—	—	—	40	pF
Output DC Voltage	V <sub>OSX</sub>	—	$\frac{V_{DD}}{2} - 0.1$	$\frac{V_{DD}}{2}$	$\frac{V_{DD}}{2} + 0.1$	V

Note 0 dBm = 0.775 V<sub>rms</sub>

## Voice signal input (TI)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Voltage Gain	GT	$V_{AO}/V_{TI}$	$\overline{FT} = "1"$ $ME = "0"$	-2	0	+2	dB
Input Signal Level	$V_{TI}$	—		—	—	0	dBm
Input Resistance	$R_{TI}$	$f_{TI} \leq 4$ kHz		50	—	—	k $\Omega$

## Built-in signal ground (SG)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
DC Voltage	$V_{SG}$	Without DC Load	$\frac{V_{DD}}{2} - 0.1$	$\frac{V_{DD}}{2}$	$\frac{V_{DD}}{2} + 0.1$	V

## Receive signal input (AI)

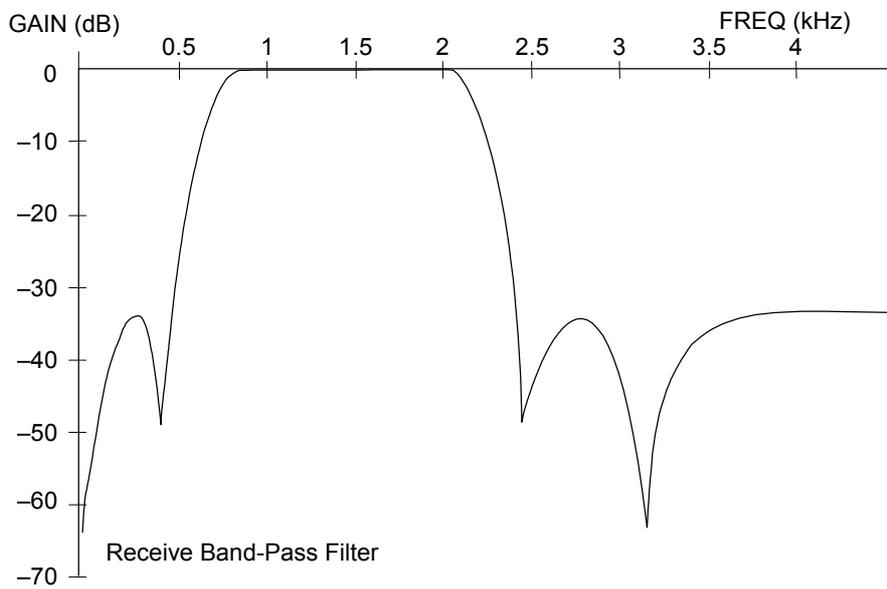
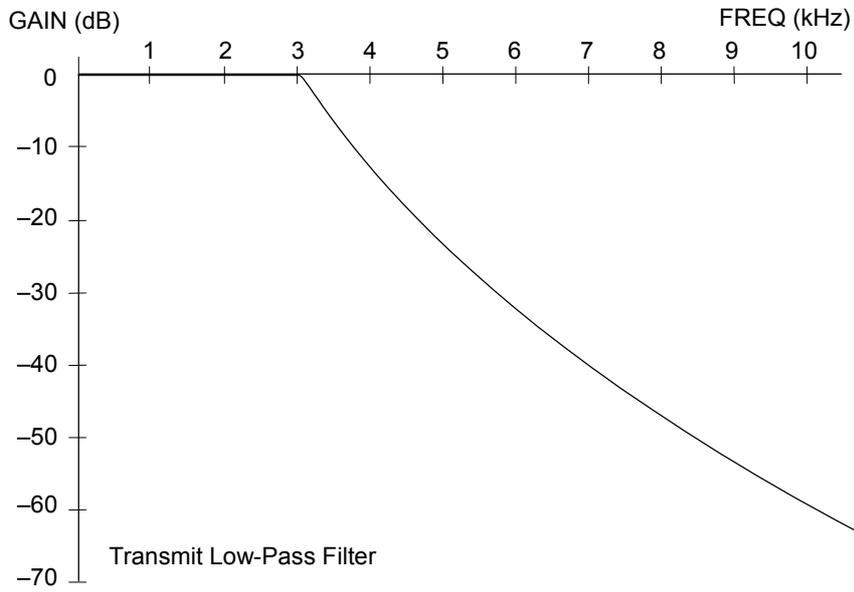
Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Input Resistance	$R_{IR}$	$f_{TI} \leq 4$ kHz		50	—	—	k $\Omega$
Receive Signal Level	$V_{IR}$	—		-30	—	0	dBm
Bit Error Rate	BER	S/N at AI	8 dB	—	$1 \times 10^{-3}$	—	N/N
			10 dB	—	$5 \times 10^{-5}$	—	

## Re-generated receive data timing clock output (RT)

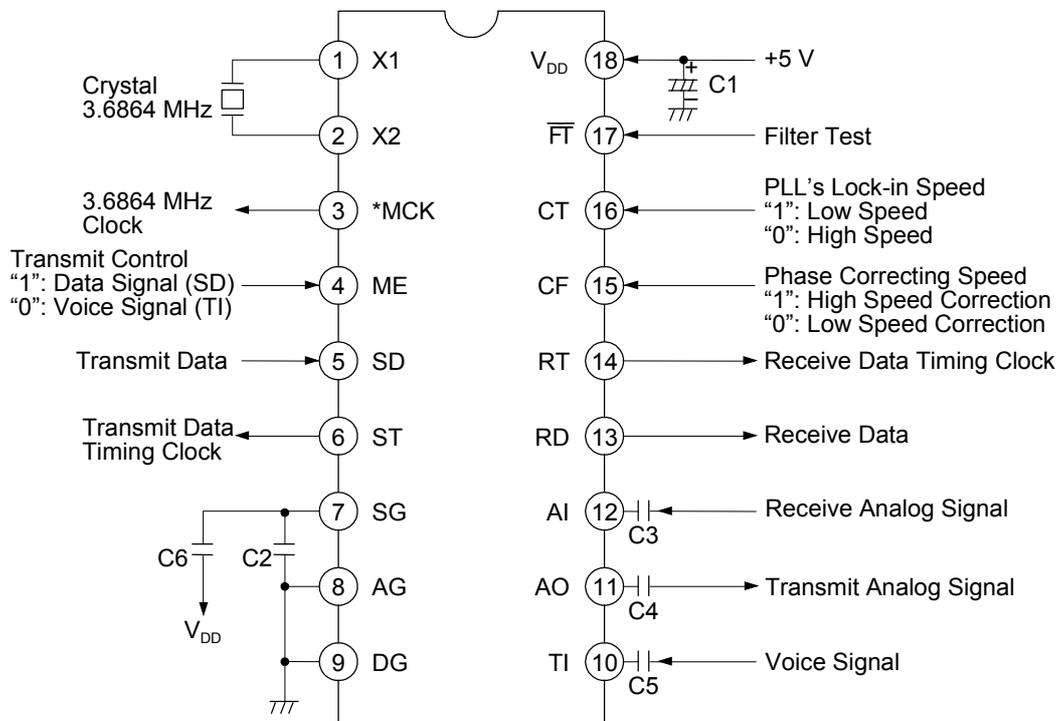
Parameter	Symbol	Condition			Min.	Typ.	Max.	Unit
Data Bit Number for PLL' Lock-in	$N_{PLL1}$ $N_{PLL2}$	CF = "1"	CT = "0"	*1	—	—	18	bit
			CT = "1"		—	—	50	

\*1 Data bit number to lock-in within 22.5 degree

**BUILT-IN FILTER FREQUENCY CHARACTERISTICS**



APPLICATION CIRCUIT



\*NC: MSM6948V

**PACKAGE DIMENSIONS**

(Unit: mm)

(Unit: mm)

#### Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.

Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

**REVISION HISTORY**

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
E2A0034-16-X1	Oct. 1996	—	—	1 <sup>st</sup> edition
FEDL6948_6948V-02	Jun. 8, 2005	6	6	Addition of Note about how the state of the AIN-pin should be on power-up

NOTICE

1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.
2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.
3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.
4. Oki assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum ratings or operation outside the specified operating range.
5. Neither indemnity against nor license of a third party's industrial and intellectual property right, etc. is granted by us in connection with the use of the product and/or the information and drawings contained herein. No responsibility is assumed by us for any infringement of a third party's right which may result from the use thereof.
6. The products listed in this document are intended for use in general electronics equipment for commercial applications (e.g., office automation, communication equipment, measurement equipment, consumer electronics, etc.). These products are not, unless specifically authorized by Oki, authorized for use in any system or application that requires special or enhanced quality and reliability characteristics nor in any system or application where the failure of such system or application may result in the loss or damage of property, or death or injury to humans.  
Such applications include, but are not limited to, traffic and automotive equipment, safety devices, aerospace equipment, nuclear power control, medical equipment, and life-support systems.
7. Certain products in this document may need government approval before they can be exported to particular countries. The purchaser assumes the responsibility of determining the legality of export of these products and will take appropriate and necessary steps at their own expense for these.
8. No part of the contents contained herein may be reprinted or reproduced without our prior permission.

Copyright 2005 Oki Electric Industry Co., Ltd.