OKI semiconductor
MSM6955GS

DIGITAL LINE TRANSCEIVER

The MSM6955 is a high performance, low power consumption type digital line transceiver LSI adopting time division two-wire (ping-pong) transmission method at a line bit rate of 512Kb/s. It realizes 144Kb/s (2B + D) two-way communication over a single pair of twisted wires.
This LSI has three ports: digital line port, voice/data port and control port. It can be used at both ends of a digital line by selecting the pin-controllable master or slave mode. It allows establishing high-speed voice/data transmission between a digital PBX and composite terminals, and can be used as a private communication high speed modem.

FEATURES

Digital line port

- Two-wire ping-pong transmission direction control, 8 KHz burst frequency, 512Kb/s transmission rate, and AMI transmission code.
- Coverage of B1 (64Kb/s) + B2 (64Kb/s) + D (16Kb/s) + K (8Kb/s) bidirectional transmission up to a line length of 2Km (at send pulse of 2 Vo-p through 0.5mmϕ twisted pair).
- AMI pulse transmission coder and peak detection type adaptive line equalization.

Voice/data and control ports

- Selectable Master/slave mode.
- Frame synchronization and receiving clock regeneration by DPLL.
- Reciprocal conversion of signal formats and bit rates between a digital line port and voice/data/control ports.
- Loop-back function in two modes: self loopback and line loopback.
- Transmission supervision and power down functions (usable for establishing transmission link).
- Selectable B1 and B2 channels in either serial or parallel I/O.
- B channels usable with system clock at 64 KHz to 2048 KHz (in master mode).
- Capability of bus connection with other MSM6955s.

Low power consumption type CMOS LSI (80mW: typ) using single power supply of 5V.

44-pin flat mold package

(These specifications are subject to change without notice.)

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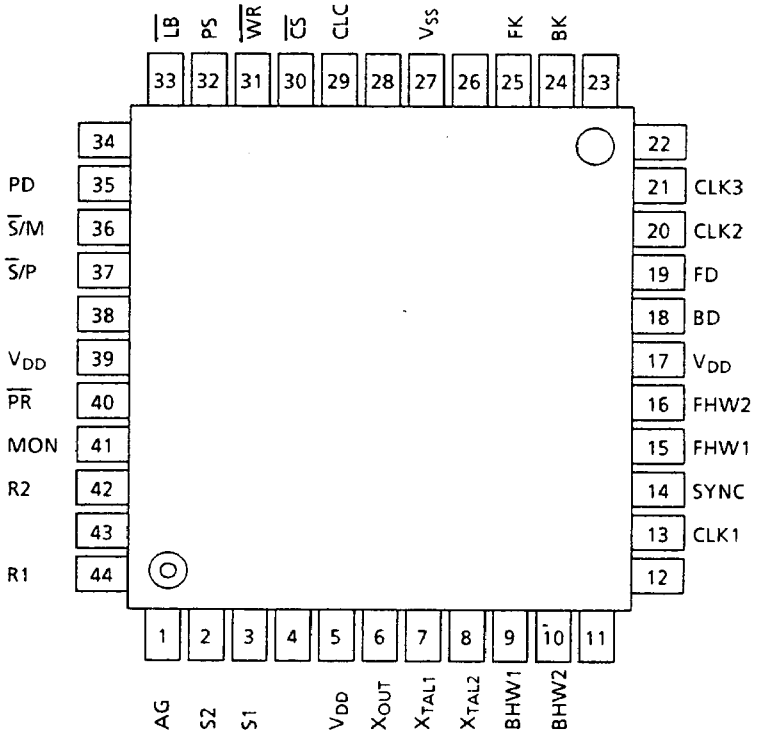
PIN ARRANGEMENT

(Top View) 44 Lead Plastic Flat Package

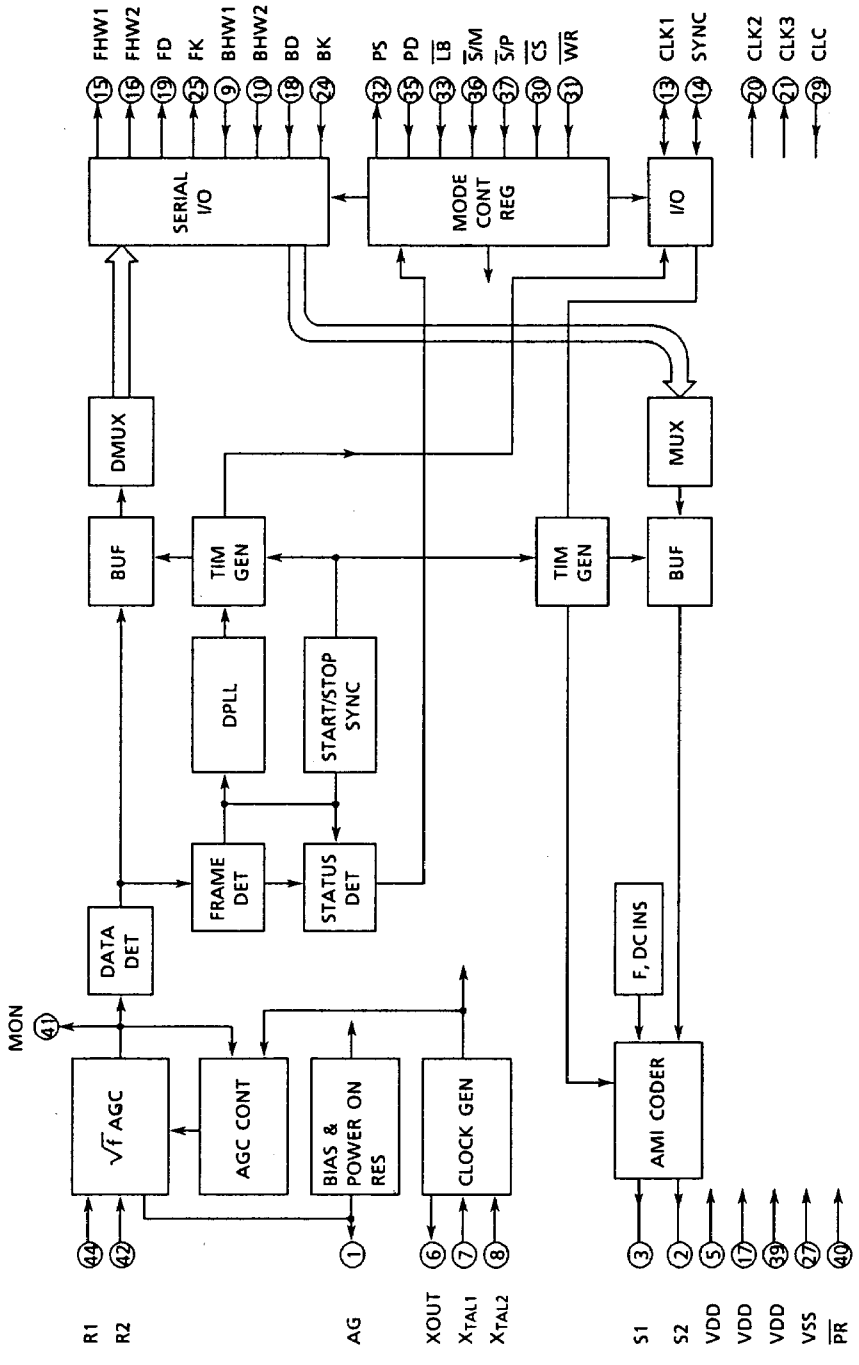


Note 1: Unnamed pins are NC pins.

Note 2: Connect Pins 17 and 39 to VDD (Pin 5) externally.

Note 3: the type name marking uses the abbreviated form of M6955.

CIRCUIT CONFIGURATION



ELECTRICAL PROPERTIES

• Absolute maximum ratings

PARAMETER	SYMBOL	TEST CONDITION	RATING	UNIT
Supply voltage	V_{DD}	Ta = 25°C	−0.3~7	V
Input/output voltage	V_I, V_O		−0.3~7	V
Input/output current	I_I, I_O		−10~10	mA
Operating temperature	Top		−10~80	°C
Storage temperature	Tstg		−55~150	°C

• Recommended operating conditions

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	APPLICATION PIN
Supply voltage	V_{DD}		4.5		5.5	V	V_{DD}
Operating temperature	Top		0		70	°C	
"H" input voltage	V_{IH}		V_{DD} x0.8		V_{DD}	V	X_{TAL1}, $\overline{PR}$
			2.4		V_{DD}	V	*1
"L" input voltage	V_{IL}		0		0.8	V	*1
							X_{TAL1}, $\overline{PR}$
Analog input voltage	V_{AIN}		V_{AG} − 1.0		V_{AG} + 1.0	V	R1
Main clock	f_{XI}		8.188	8.192	8.196	MHz	X_{TAL1}, X_{TAL2}
Clock 1 frequency	f_{CLK1}	Master mode	64		2048	KHz	CLK1
Clock 1 duty	D_{CLK1}	f_{XI} = 8.192 MHz		50		%	
SYNC signal frequency	f_{SYNC}		7.993	8	8.007	KHz	SYNC
SYNC signal pulse width	t_{WSYNC}		1/ f_{CLK1}		117	µs	
SYNC signal timing	t_{MS}		50			ns	
	t_{SM}		100			ns	

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	APPLICABLE PIN
BHW setup time	t_{SBHW}	Master mode			240	ns	BHW1, 2
BHW hold time	t_{HBHW}	f_{XI} = 8.192 MHz	240			ns	
BD setup time	t_{SBD}	(Note 1)			240	ns	BD
BD hold time	t_{HBD}		240			ns	
BK setup time	t_{SBK}				720	ns	BK
BK hold time	t_{HBK}		240			ns	
$\overline{WR}$ pulse	$t_{W\overline{WR}}$		600			ns	$\overline{WR}$
BHW setup time	t_{SBHW}	Slave mode			360	ns	BHW1, 2
BHW hold time	t_{HBHW}	f_{XI} = 8.192 MHz	360			ns	
BD setup time	t_{SBD}	(Note 2)			360	ns	BD
BD hold time	t_{HBD}		360			ns	
BK setup time	t_{SBK}				860	ns	BK
BK hold time	t_{HBK}		360			ns	

*1 BHW1, BHW2, CLK1, SYNC, BD, BK, $\overline{CS}$, $\overline{WR}$, $\overline{LB}$, PD, $\overline{S}$/M, $\overline{S}$/P

(Note 1) In the master mode, these values include the jitter 1/8.129 MHz = 122ns between fXI = 8.192 MHz and CLK1/CLK2/SYNC signal.

(Note 2) In the slave mode, these values include total 244 ns of 122 ns as the jitter of send pulse signal from the master and 122 ns as the jitter in the built-in DPLL (using slave fXI = 8.192 MHz).

• DC characteristics

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	APPLICABLE PIN
Supply current	I_{DD}			16	28	mA	VDD
"H" input current	I_{IH}	$V_{IH} = V_{DD}$	− 10		10	µA	*1
"L" input current	I_{IL}	$V_{IL} = 0V$	− 10		10	µA	
"H" output voltage	V_{OH}	$I_{OH} = -20\mu A$	2.4			V	*2
"L" output voltage	V_{OL}	$I_{OL} = 1.6mA$			0.4	V	*2
		$R_L = 1k\Omega$			0.5	V	FHW, FD, FK, PS
Output leak current	I_{OZ}				20	µA	FHW, FD, FK, PS
Analog midpoint voltage	V_{AG}		$\frac{V_{DD}}{2} - 0.1$	$\frac{V_{DD}}{2}$	$\frac{V_{DD}}{2} + 0.1$	V	AG

*1 BHW1, BHW2, CLK1, SYNC, BD, BK, $\overline{CS}$, $\overline{WR}$, $\overline{LB}$, PD, $\overline{S}$/M, $\overline{S}$/P

*2 S1, S2, CLK1, SYNC, CLK2, CLK3.

• Analog characteristics

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	APPLICABLE PIN
Minimum gain	A_{MIN}	A_{IN} = 256 KHz, V_{MON} = 2Vp-p, C_L = 20PF	1.9	2.9	3.9	dB	MON
Maximum gain	A_{MAX}		16.2	17.2	18.2	dB	

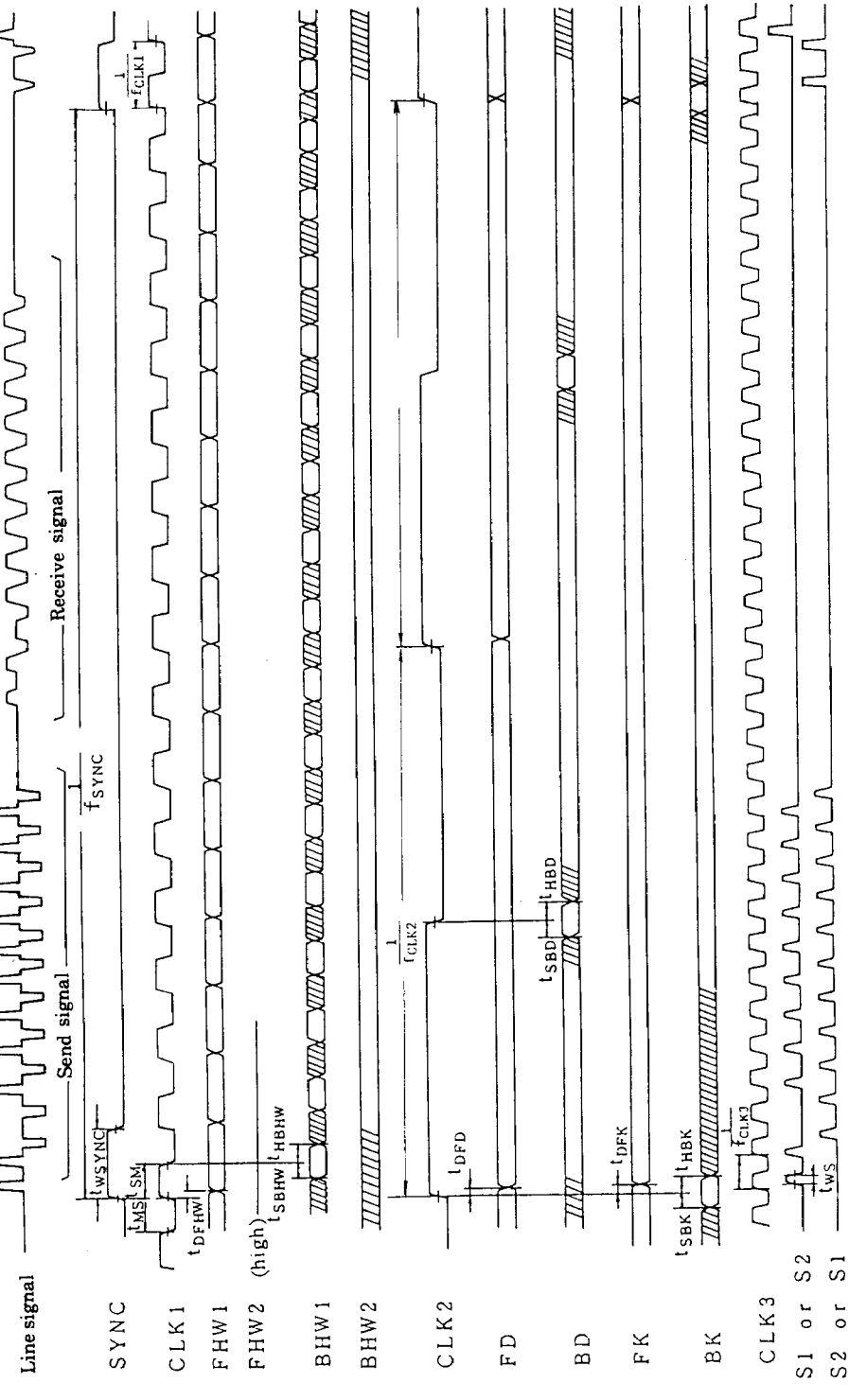
• Timing characteristics

PARAMETER	SYMBOL	CONDITION		MIN.	TYP.	MAX.	UNIT	APPLICABLE PIN
SYNC signal frequency	f_{SYNC}	(Note 2) Slave mode f_{XI} = 8.192MHz		7.983	8	8.017	KHz	SYNC
SYNC pulse width	f_{WSYNC}		Parallel mode	15.813	16.113	16.4	µs	
			Serial mode	8.0	8.3	8.6	µs	
Clock 1 frequency	f_{CLK1}		Parallel mode	62.54	64	67.12	KHz	CLK1
			Serial mode	122.30	128	134.25	KHz	
Clock 1 duty	D_{CLK1}				50		%	
Clock 2 frequency	f_{CLK2}	f_{XI} = 8.192MHz	Master mode (Note 1)	15.93	16	16.06	KHz	CLK2
			Slave mode (Note 2)	15.91	16	16.1	KHz	
Clock 2 duty	D_{CLK2}				50		%	
Clock 3 frequency	f_{CLK3}	f_{XI} = 8.192MHz	Master mode (Note 1)	241.06	256	272.90	KHz	CLK3
			Slave mode (Note 2)	234.17	256	282.3	KHz	
Clock 3 duty	D_{CLK3}				50		%	
FHW output delay	t_{DFHW}	f_{XI} = 8.192MHz (Note 3) R_L = 1KΩ C_L = 20pF			160	260	ns	FHW1, 2
FD output delay	t_{DFD}				160	260	ns	FD
FK output delay	t_{DFK}				160	260	ns	FK
Send signal pulse width	t_{WS}	f_{XI} = 8.192MHz C_L = 20pF		$\frac{1}{1.024MHz} - 120$	$\frac{1}{1.024MHz}$	$\frac{1}{1.024MHz} + 120$	ns	S1, S2

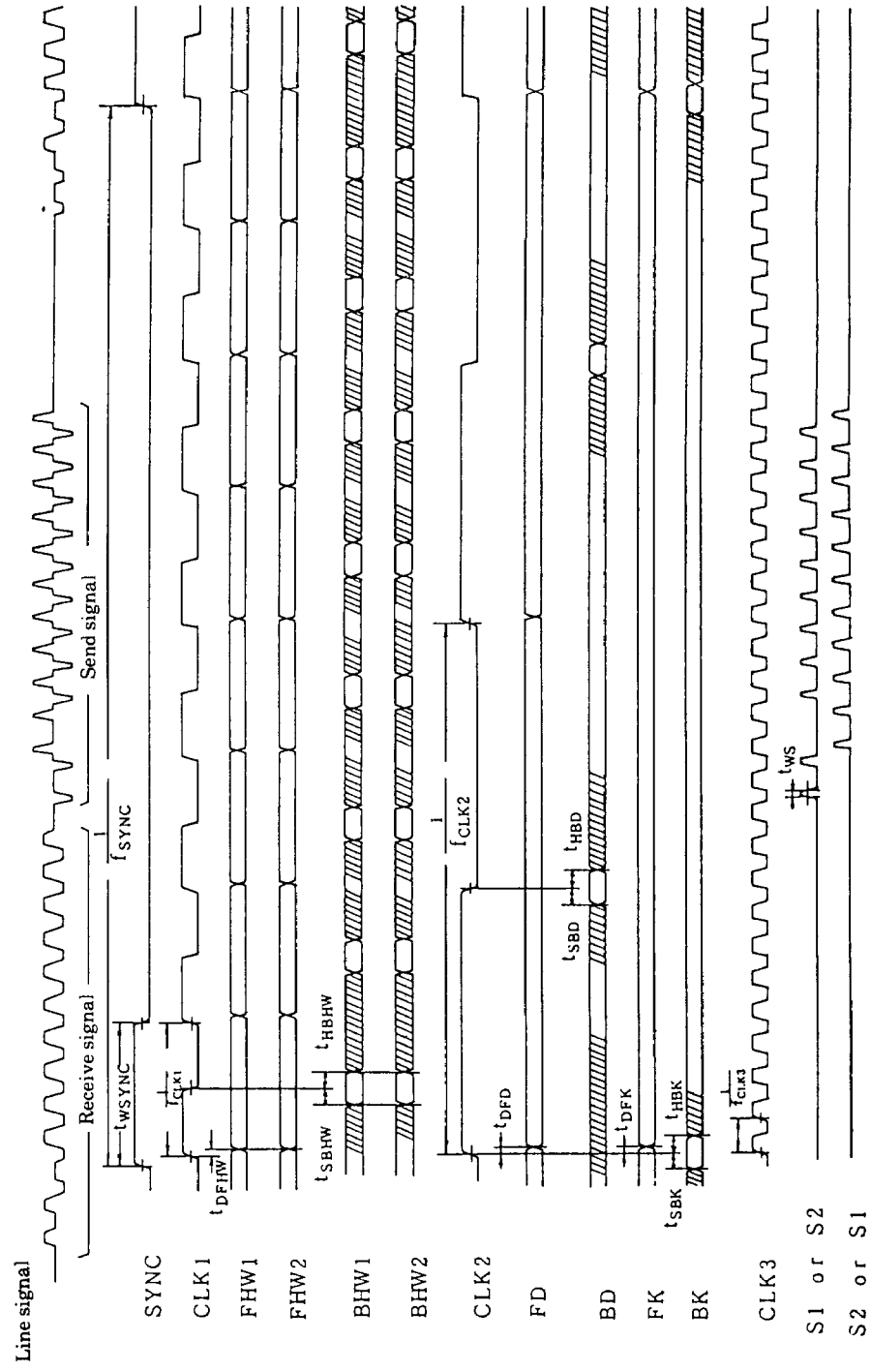
(Note 1) In the master mode, these values include the jitter of 1/8.192 MHz = 122ns between f_{XI} = 8.192 MHz and CLK1/SYNC signal.

(Note 2) In the slave mode, these values include total 244ns of 122ns as the jitter of the send pulse signal from the master and 122ns as the jitter of built-in DPLL (using slave f_{XI} = 8.192 MHz).

(Note 3) Since CLK1, CLK2 and SYNC cause the jitter in Notes 1 and 2, the jitter in these parameters arises in synchronism but no delay time jitter exists.



Master mode timing diagram (example for serial mode, $f_{CLK1} = 128$ KHz)



Slave mode timing diagram (parallel mode)

EXPLANATION OF INPUT/OUTPUT PINS

(1) Line pins

- S1 (pin 3) and S2 (Pin 2) See Fig. 1.

  These are send-signal output pins. These signals are output to the line after AMI coding through the pulse transformer. In the power up (PD = L) state, the frame signal F/P, housekeeping signal K, control signal D and voice/data signals B1 and B2 are sent according to the transmission format.
  In the power down state (PD = H), the S1 and S2 outputs go to "L" level and transmission to the line stops.

- AG (pin 1), R1 (pin 44) and R2 (pin 42)

  The AG pin outputs the 2.5V analog signal ground. The center level of the received AMI signal through the line is converted to the analog signal ground and input to the IC.
  The R1 and R2 pins are input pins for AMI signal received through the external filter.
  See Fig. 10 for the connection of S1, S2, R1, R2 and AG with the external circuit.

(2) Highway pins

- FHW1 (pin 15) and FHW2 (pin 16) See Figs. 2 to 6.

  These are output pins for signals B1 and B2 received from the line. They are output in synchronism with SYNC and at the bit rate of CLK1. These pins provide open drain outputs allowing wired-OR connections.
  Two types of bit rates in synchronism with the SYNC can be selected by the $\overline{S}$/P pin input.
  If $\overline{S}$/P = L, the FHW1 pin outputs 16 bit (B1 + B2) consecutive receive signals and the FHW2 pin output goes to the high impedance state.
  If $\overline{S}$/P = H, the FHW1 and FHW2 pins simultaneously output 8 bits of B1 and 8 bits of B2.
  The above mode is in the power up (PD = L) state. In the power down (PD = H) state, both FHW1 and FHW2 pin outputs go to the high impedance state irrespective of the $\overline{S}$/P pin level.

- BHW1 (pin 9) and BHW2 (pin 10) See Figs. 2 to 6.

  These are input pins for the B1 and B2 signals sent to the line. They are input at the bit rate of the CLK1. The B1 and B2 signals are read in at the falling edge of CLK1.
  Two types of bit rates in synchronism with SYNC can be selected by the $\overline{S}$/P pin.
  If $\overline{S}$/P = L, 16 bits consecutive (B1 + B2) signal is input to BHW1, and the input to BHW2 becomes don't care.
  If $\overline{S}$/P = H, 8 bits of B1 and 8 bits of B2 are input to BHW1 and BHW2 respectively at the same time.
  The above mode is in the power up (PD = L) state. In the power down (PD = H) state, input signals are invalid because transmission to the line stops.

- CLK1 (pin 13) See Figs. 5 and 6.

  This pin is an input/output pin for CLK1. The signals at FHW1, FHW2, BHW1 and BHW2 are input and output at the bit rate of this clock.
  The S/M and S/P signals control this terminal.
  S/M controls the CLK1 input/output, and S/P selects the clock frequency.
  In the master mode (S/M = H), CLK1 pin becomes the 64 to 2048 KHz clock input pin in both the serial (S/P = L) and parallel (S/P = H) modes.
  In the slave mode (S/M = L), CLK1 outputs 128 KHz clock in the serial mode (S/P = L) and 64 kHz clock in the parallel mode (S/P = H).
  If no signal is received from the line because of the power down of the connected master, the CLK1 pin output in the slave goes to the "H" level.

- SYNC (pin 14) See Figs 5 and 6.

  This is an input/output pin for the 8 KHz SYNC signal. The signals at FHW1, FHW2, BHW1 and BHW2 are input and output in synchronism with the SYNC signal.
  The S/M signal determines the input or output for the SYNC pin. In the master mode (S/M = H) the 8 KHz SYNC signal is input, and in the slave mode (S/M = L) the 8 KHz SYNC signal is output.

(3) Control pins

- FD (pin 19) and BD (pin 18)

  These are 16 Kb/s control signal output pin (FD) and input pin (BD). FD is output at the rising edge of CLK2, and BD is read in at the falling edge of CLK2. FD is an open drain output pin allowing wired-OR connection.
  If CS = L, the FD pin outputs the signal received from the line and the BD pin inputs the output signal to the line.
  If CS = H, the FD pin goes to the high impedance state and the BD pin becomes don't care. In this case, the D output to the line becomes the "H" level.
  The FD pin can output the signal received from the line even in the power down (PD = H) state, but the FD output becomes the "H" level when there is no receive burst signal on the line.

- CLK2 (pin 20) and CLK3 (pin 21)

  These are clock output pins for sending FD control signal and receiving BD control signal.
  CLK2 is the 16 KHz clock for synchronous transmission of FD and BD, and is supplied to the external serial I/O.
  CLK3 is the 256 KHz clock (16 KHz x 16) for asynchronous transmission of FD and BD, and is supplied to the external asysnchronous serial I/O.
  The CLK3 pin provides $\overline{CLK3}$ when CLC is set to the "L" level.
  The CLk2 and CLK3 outputs are constantly provided irrespective of the PD and $\overline{CS}$ controls.

- CLC (pin 29)

  This is an input pin to control the CLK3 pin.
  When this pin is open or the input to this pin is the "H" level, the CLk3 pin outputs CLK3 and when the input is the "L" level, this pin outputs $\overline{CLK3}$.
  Since this pin is conected to the V_{DD} through a high resistance in the IC, prevent noise input to this pin when it is used in open state. If it is used with the "L" level input, keep the input level at 0.2V or less.

- FK (pin 25) and BK (Pin 24)

  These are 8 Kb/s housekeeping signal output pin (FK) and input pin (BK). The FK pin provides open drain output allowing wired-OR conenction.
  If $\overline{CS}$ = L, FK signal can be sent and BK signal can be received.
  If $\overline{CS}$ = H, the FK pin goes to the high impedance state and the BK pin does not accept input signal.
  When $\overline{CS}$ = H, the K signal latched in the internal register at CS = L is sent to the line.
  The FK pin outputs the K signal received from the line in both PD = H and PD = L state.

- PD (pin 35) See Figs. 4, 7 and 8.

  This is an input pin for power down control.
  PD = H causes the power down mode. Because this mode makes the S1 and S2 outputs go to the "L "level and stop transmission to the other station, the power consumption by the external driver can be reduced. At the same time FHW1 and FHW2 go to the "H" level and the PS pin indicating the ping-pong transmission state goes to the "L" level.
  PD = L causes the ready state for transmission. S1, S2, FHW1, FHW2, BHW1 and BHW2 go to the active state.
  The PD signal is latched in an internal register when $\overline{CS}$ = L and $\overline{WR}$ = L. It is held in other states.
  Use of the FD and FK output signals enables handshaking of power down control.

- PS (pin 32)

  This is an output pin for monitoring ping-pong transmission.
  If PD = L, the DPLL built in the LSI establishes slave synchronization with the master and monitors the frame signal mutually between the master and slave. The PS signal goes to the "H" level when the normal ping-pong synchronization is established.
  PS goes to the "L" level if PD = H or step-out occurs.
  The PS output pin provides open drain output allowing wired-OR connection.

- $\overline{LB}$ (pin 33) See Fig. 9.

  This is a test control input pin.
  In the loopback mode ($\overline{LB}$ = L), two types of loopback tests are possible.
  In the power down (PD = H) state, the self loopback mode (TEST1) is established. BHW1,

BHW2, BD and BK signals are looped back to FHW1, FHW2, FD and FK, respectively. During communication (PD = L), the line loopback mode (TEST2) is established. The signals received from the line are looped back through the line to the other station. In this line loopback mode (TEST2), the line received signals D and K are output from the FD and FK pins, but the outputs FHW1 and FHW2 are set to the high impedance state.

- $\overline{S}/M$ (pin 36) See Figs. 5 and 6.

  This is an input pin for selecting a master or slave mode. $\overline{S}/M$ = H sets the master mode, and $\overline{S}/M$ = L sets the slave mode.
  This pin should be conencted to V_{DD} or GND.

- $\overline{S}/P$ (pin 37) See Figs. 2 and 3.

  This is an input pin for selecting the serial or parallel mode. $\overline{S}/P$ = H sets the parallel mode, and $\overline{S}/P$ = L sets the serial mode.
  The $\overline{S}/P$ signal is latched in an internal register when $\overline{CS}$ = L and $\overline{WR}$ = L. It is held in other states.

- $\overline{WR}$ (pin 31) See Fig. 7.

  This is the write control input pin for setting the state to the mode selecting register (PD, $\overline{LB}$ and $\overline{S}/P$).
  The level at the time of $\overline{CS}$ = L and $\overline{WR}$ = L is written in the mode selecting register. The register content is held in other states.

- $\overline{CS}$ (pin 30) See Fig. 7.

  This is a chip select input pin. If $\overline{CS}$ = L, the control signal input/output pins (FD, BD, FK and BK) and ping-pong transmission status output pin PS become active.

(4) Common pins

- X_{TAL1} (pin 7), X_{TAL2} (pin 8) and X_{OUT} (pin 6) See Fig. 10.

  X_{TAL1} is the 8.192 MHz clock input pin.
  Connecting an 8.192 MHz crystal oscillator to the X_{TAL1} and X_{TAL2} pins enables it to be used as the oscillating circuit. This clock is supplied to the internal circuit of the IC.
  X_{OUT} is an output pin for the above clock. This pin can be used for clock monitoring or clock supply to the external circuit.

- MON (pin 41)

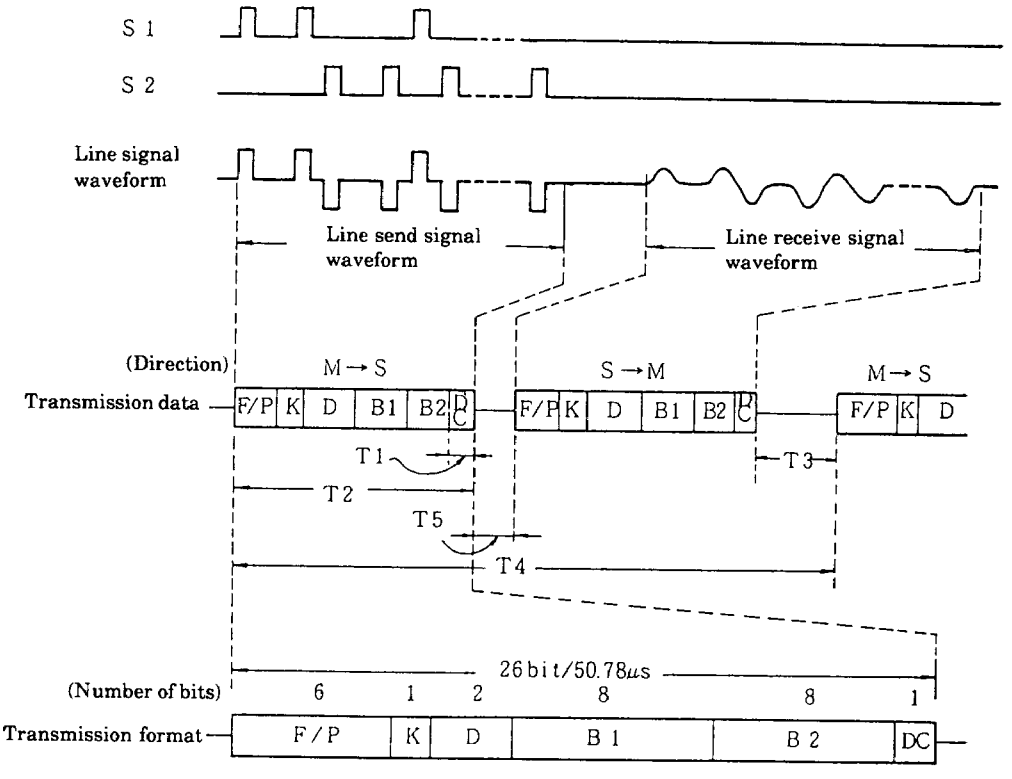
  This is the pin for monitoring the analog signal in the LSI. The received signal equalized through the $\sqrt{f}$ AGC circuit is output.

- $\overline{PR}$ (pin 40)

  This is an input pin for power-on-reset.
  When the $\overline{CS}$ pin or the $\overline{WR}$ pin is "H", if the $\overline{PR}$ pin is set to "L", the internal mode register gets the state, PD = H, $\overline{LB}$ = H, $\overline{S}$/P = H, and if the $\overline{PR}$ pin is turned to H, the register holds its contents.
  This pin is connected to the comparator which has a threshold level of $V_{DD}/2$, and to V_{DD} through a 20KΩ pull-up resistance. By connecting a capacitance between this $\overline{PR}$ pin and GND, this pin can be used as a power on reset circuit which sets PD = H, $\overline{LB}$ = H, $\overline{S}$/P = H to the internal mode register. This pin should be open or connected to V_{DD} if it isn't used or the $\overline{CS}$ and $\overline{WR}$ pins are used to set the mode state.

TIME DIAGRAM

- **Ping-pong transmission**



F/P : Frame synchronization and ping-pong transmission monitor bits
K : Housekeeping bit (8 Kb/s)
D : Control bits (16 Kb/s)
B1, 2 : Voice/data bits (64 Kb/s)
DC : DC balance bit

TIME	SYMBOL	MIN	TYP	MAX
1 bit time	T1	–	1.95 μs	–
Burst time	T2	–	50.78 μs	–
Send/receive switchover time	T3	0.925 μs	–	–
Transmission cycle	T4	–	125 μs	–
Transmission delay time (line length: 0 to 2 km)	T5	1.95 μs	–	21.49 μs

Fig. 1

- **Parallel mode ($\overline{S}$/P = H)**

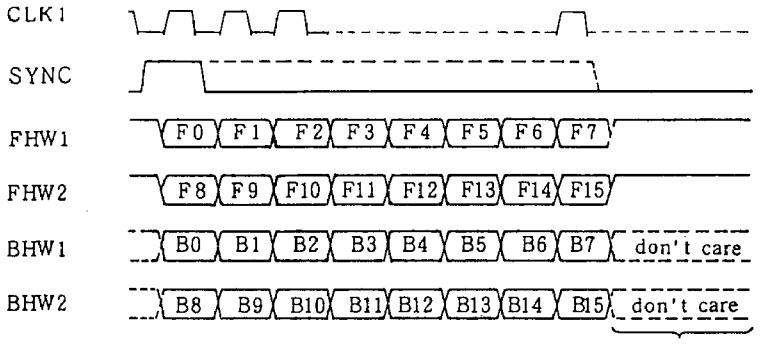


Fig. 2 When CLK is 128 KHz or above

- **Serial mode ($\overline{S}$/P = L)**

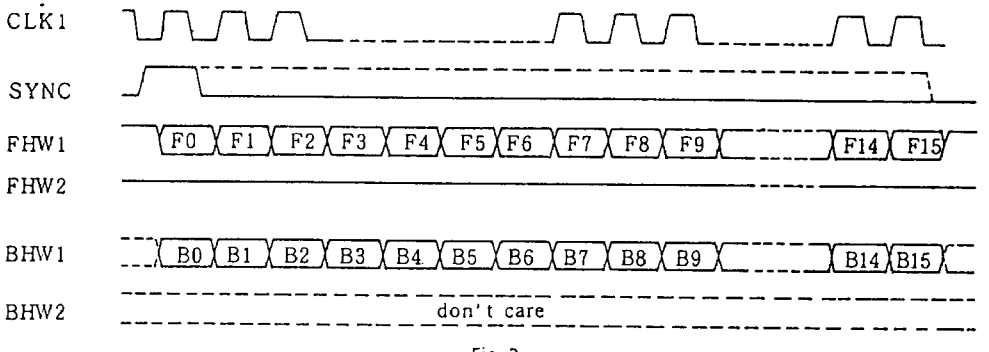


Fig. 3

- **Power down mode**

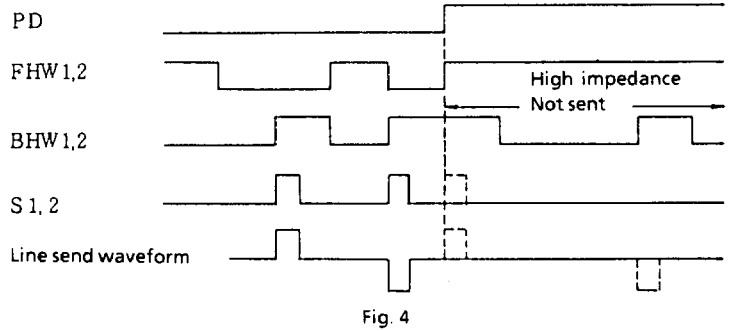
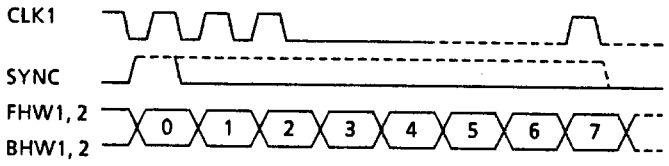


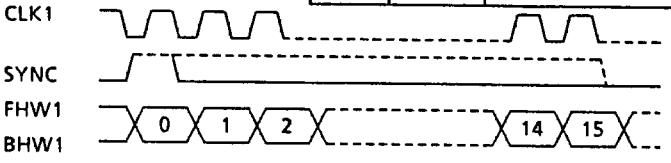
Fig. 4

- **Master mode (S/M = H)**



Parallel mode

	I/O	Frequency	Remarks
CLK1	Input	64 KHz~ 2048 KHz	duty 50%
SYNC	Input	8 KHz	$\frac{1}{CLK1}$ ~ 117μs width

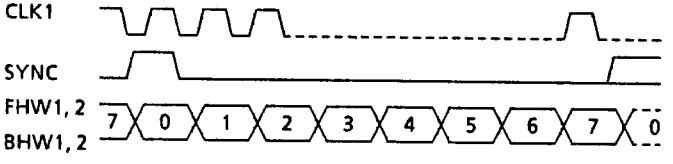


Serial mode

	I/O	Frequency	Remarks
CLK1	Input	128 KHz~ 2048 KHz	duty 50%
SYNC	Input	8 KHz	$\frac{1}{CLK1}$ ~ 117μs width

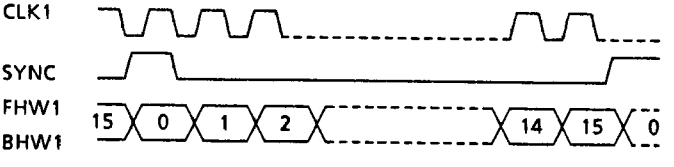
Fig. 5

- **Slave mode (S/M = L)**



Parallel mode

	I/O	Frequency	Remarks
CLK1	Output	64 KHz	duty 50%
SYNC	Output	8 KHz	16.113μs width



Serial mode

	I/O	Frequency	Remarks
CLK1	Output	128 KHz	duty 50%
SYNC	Output	8 KHz	8.3μs width

Fig. 6

- **Control signals**

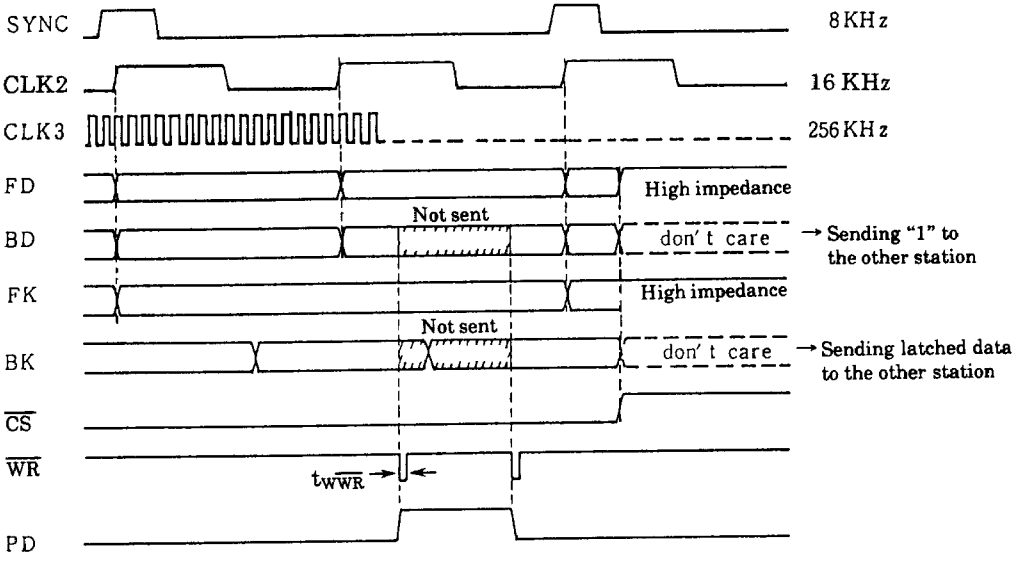


Fig. 7

- **Power down control**

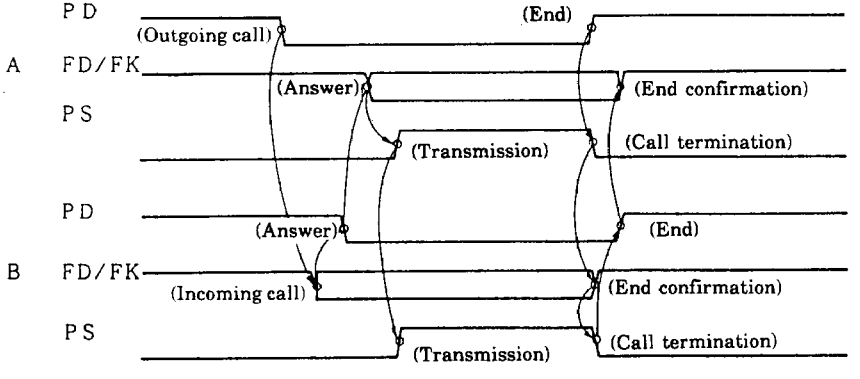


Fig. 8

- Loopback mode

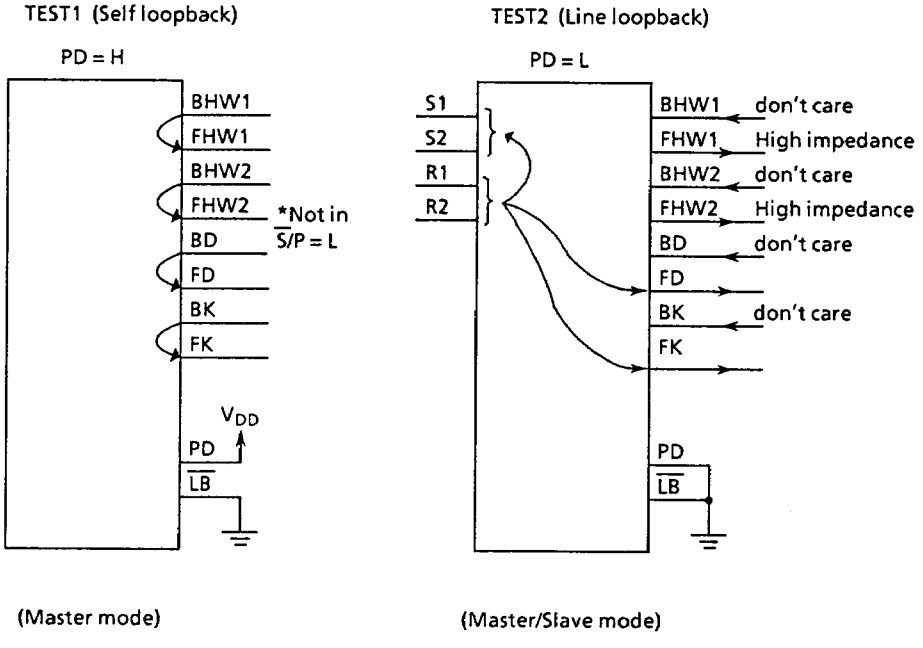


Fig. 9

TYPICAL EXTERNAL CONNECTION

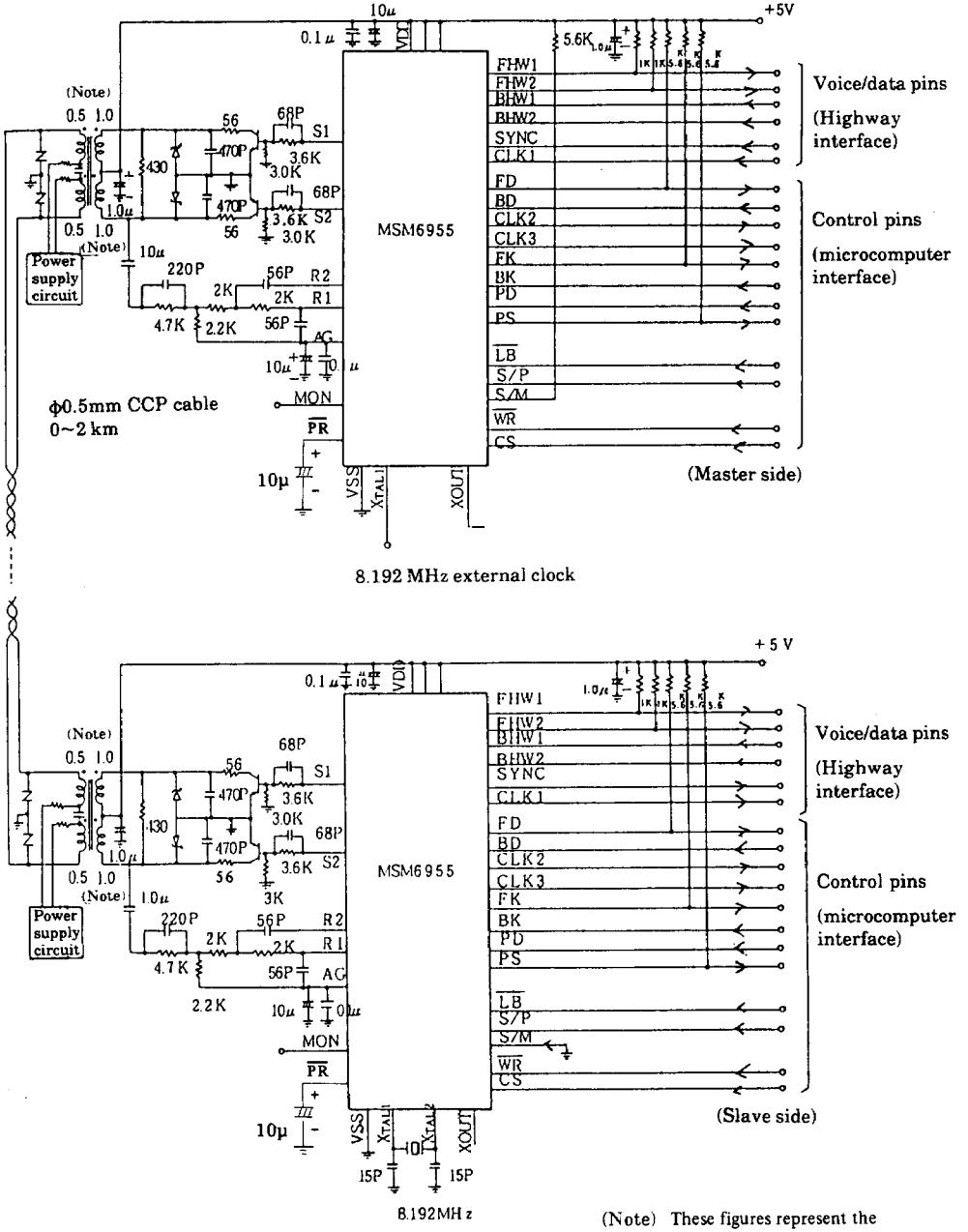


Fig. 10

(Note) These figures represent the turn-ratio of pulse transformer

GENERAL DESCRIPTION OF FUNCTIONS

Line transmission is possible up to 2 Km (through a two-wire twisted pair private cable). This LSI has an internal $\sqrt{f}$ AGC circuit, and the control is carried out in combination with the external CR circuit. The transmission format is B + B + D + K (B: 64 Kb/s, D: 16 Kb/s, K: 8 Kb/s). Ping-pong transmission using the AMI code is carried out at a bit rate of 512 KHz at intervals of 8 KHz (125 μs). This communication is carried out between the connected master and slave, and the slave is synchronized with the master by the DPLL mounted in the LSI. This LSI has the master/slave select pin ($\overline{S}$/M pin) for setting to either the master or slave.

As additional functions, the ping-pong transmission supervising pin (PS pin) and power down pin (PD pin) are provided. The transmission status can be supervised by using the PS pin output. Since external line driver operation can be stopped by the PD pin (power down mode), the power consumption in other than the communication state can be reduced.

The B signal interface on the master side can be operated by the system clock at 64 KHz to 2048 KHz. The serial/parallel mode select pin ($\overline{S}$/P pin) enables connection of 1 time slot (FHW1/FHW2, BHW1/BHW2) in the parallel mode, or 2 time slots (FHW1, BHW1) in the serial mode.

As regards B signals on the slave side, one set of 128 Kb/s input/output pins (FHW1, BHW1) in the serial mode or two sets of 64 Kb/s input/output pins (FHW1/FHW2, BHW1/BHW2) in the parallel mode can be selected.

The clock pins (CLK1 and SYNC) for synchronization input the clocks supplied from the system in the master mode. In the slave mode they output clocks to external devices.

The 16 Kb/s D signal and 8 Kb/s K signal are used as control signals.

For the D signal, the synchronous communication clock (CLK2: 16 KHz) and asynchronous communication clock (CLK3: 16 KHz x 16 = 256 kHz) are supported in consideration of the use of serial communication LSIs (SIO 8251, etc.).

Asynchronous input data at 16 Kb/s is converted to synchronous data at 16 Kb/s by the circuit in this LSI. The LSI also allows the use of the 8 Kb/s K signal as the housekeeping signal. Since this input pin (BK pin) configures a latch circuit, it is optimum for sending and receiving level signals.

The loopback test pin ($\overline{LB}$ pin) enables two types of tests. One is the self loop test in the power down state, and the other is the line loopback test during ping-pong communication.

This LSI allows selection of various modes. Mode selecting pins are the serial/parallel mode select pin ($\overline{S}$/P), power down mode selecting pin (PD), loopback mode selecting pin ($\overline{LB}$), and master/slave mode select pin ($\overline{S}$/M). The mode for the master/slave select pin ($\overline{S}$/M) is set directly.

The mode for each of the other pins is set by the chip select pin ($\overline{CS}$) and write pin ($\overline{WR}$).

This LSI also incorporates the consideration for external parts reduction and microprocessor interface.

All logical outputs excluding clock outputs (CLK2 and CLK3 as well as CLK1 and SYNC in slave mode) are open drain outputs to allow bus connection.

Control signal outputs (FD, FK and PS) become active only in the chip select state. Input pin BK latches the input only when the chip is selected. The status setting register ($\overline{S}$/P, PD, $\overline{LB}$) can also be connected to the bus for status setting by the chip select ($\overline{CS}$) and write ($\overline{WR}$) signals.

APPLICATION TO DIGITAL PBX

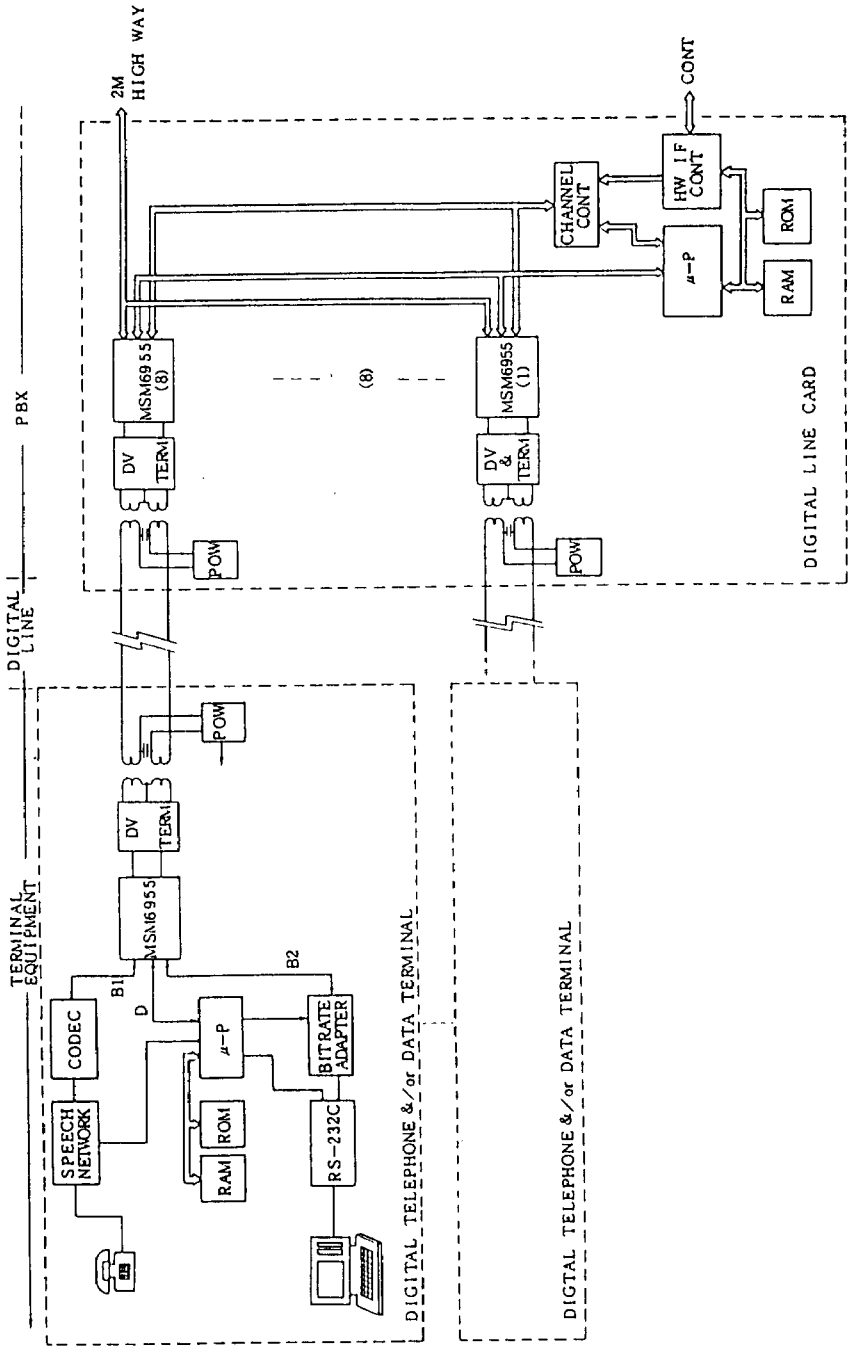


Fig. 11