

8-Input Data Selector/Multiplexer

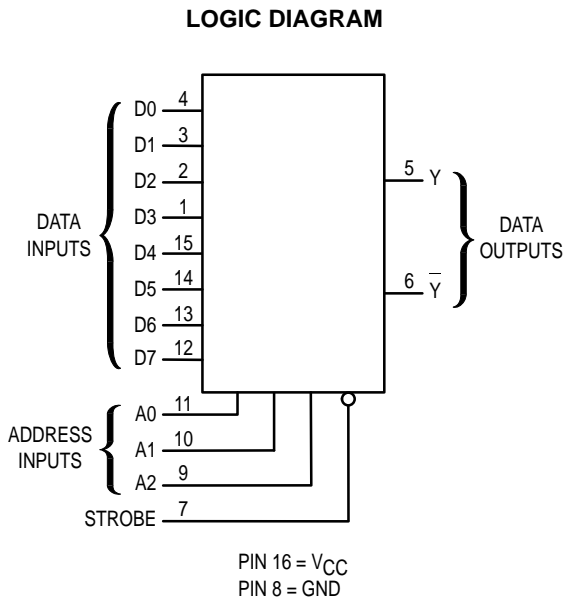
High-Performance Silicon-Gate CMOS

The MC74HC151 is identical in pinout to the LS151. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

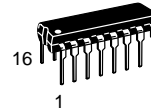
This device selects one of the eight binary Data Inputs, as determined by the Address Inputs. The Strobe pin must be at a low level for the selected data to appear at the outputs. If Strobe is high, the Y output is forced to a low level and the \bar{Y} output is forced to a high level.

The HC151 is similar in function to the HC251 which has 3-state outputs.

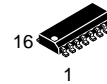
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 132 FETs or 33 Equivalent Gates



MC74HC151



N SUFFIX
PLASTIC PACKAGE
CASE 648-08

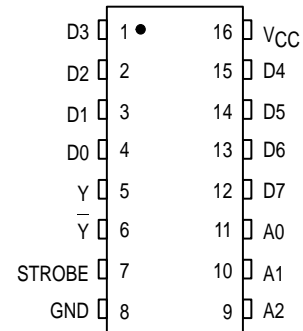


D SUFFIX
SOIC PACKAGE
CASE 751B-05

ORDERING INFORMATION

MC74HCXXXN Plastic
MC74HCXXXD SOIC

PIN ASSIGNMENT



FUNCTION TABLE

| Inputs | | | | Outputs | |
|--------|----|----|--------|---------|------------|
| A2 | A1 | A0 | Strobe | Y | \bar{Y} |
| X | X | X | H | L | \bar{H} |
| L | L | L | L | D0 | $\bar{D0}$ |
| L | L | H | L | D1 | $\bar{D1}$ |
| L | H | L | L | D2 | $\bar{D2}$ |
| L | H | H | L | D3 | $\bar{D3}$ |
| H | L | L | L | D4 | $\bar{D4}$ |
| H | L | H | L | D5 | $\bar{D5}$ |
| H | H | L | L | D6 | $\bar{D6}$ |
| H | H | H | L | D7 | $\bar{D7}$ |

D0, D1, ..., D7 = the level of the respective D input.



MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|------------------|--|--------------------------------|------|
| V _{CC} | DC Supply Voltage (Referenced to GND) | - 0.5 to + 7.0 | V |
| V _{in} | DC Input Voltage (Referenced to GND) | - 1.5 to V _{CC} + 1.5 | V |
| V _{out} | DC Output Voltage (Referenced to GND) | - 0.5 to V _{CC} + 0.5 | V |
| I _{in} | DC Input Current, per Pin | ± 20 | mA |
| I _{out} | DC Output Current, per Pin | ± 25 | mA |
| I _{CC} | DC Supply Current, V _{CC} and GND Pins | ± 50 | mA |
| P _D | Power Dissipation in Still Air Plastic DIP† SOIC Package† | 750 500 | mW |
| T _{stg} | Storage Temperature | - 65 to + 150 | °C |
| T _L | Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) | 260 | °C |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

† Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C

SOIC Package: - 7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit | |
|------------------------------------|--|---|-----------------|--------------------|----|
| V _{CC} | DC Supply Voltage (Referenced to GND) | 2.0 | 6.0 | V | |
| V _{in} , V _{out} | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | V _{CC} | V | |
| T _A | Operating Temperature, All Package Types | - 55 | + 125 | °C | |
| t _r , t _f | Input Rise and Fall Time (Figure 1) | V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V | 0 0 0 | 1000 500 400 | ns |

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | V _{CC} V | Guaranteed Limit | | | Unit |
|-----------------|--|---|--|------------------|--------|---------|------|
| | | | | - 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| V _{IH} | Minimum High-Level Input Voltage | V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA | 2.0 | 1.5 | 1.5 | 1.5 | V |
| | | | 4.5 | 3.15 | 3.15 | 3.15 | |
| | | | 6.0 | 4.2 | 4.2 | 4.2 | |
| V _{IL} | Maximum Low-Level Input Voltage | V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA | 2.0 | 0.3 | 0.3 | 0.3 | V |
| | | | 4.5 | 0.9 | 0.9 | 0.9 | |
| | | | 6.0 | 1.2 | 1.2 | 1.2 | |
| V _{OH} | Minimum High-Level Output Voltage | V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA | 2.0 | 1.9 | 1.9 | 1.9 | V |
| | | | 4.5 | 4.4 | 4.4 | 4.4 | |
| | | | 6.0 | 5.9 | 5.9 | 5.9 | |
| | | | V _{in} = V _{IH} I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA | 4.5 | 3.98 | 3.84 | |
| 6.0 | 5.48 | 5.34 | 5.20 | | | | |
| V _{OL} | Maximum Low-Level Output Voltage | V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA | 2.0 | 0.1 | 0.1 | 0.1 | V |
| | | | 4.5 | 0.1 | 0.1 | 0.1 | |
| | | | 6.0 | 0.1 | 0.1 | 0.1 | |
| | | | V _{in} = V _{IH} or V _{IL} I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA | 4.5 | 0.26 | 0.33 | |
| 6.0 | 0.26 | 0.33 | 0.40 | | | | |
| I _{in} | Maximum Input Leakage Current | V _{in} = V _{CC} or GND | 6.0 | ± 0.1 | ± 1.0 | ± 1.0 | μA |
| I _{CC} | Maximum Quiescent Supply Current (per Package) | V _{in} = V _{CC} or GND I _{out} = 0 μA | 6.0 | 8 | 80 | 160 | μA |

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

| Symbol | Parameter | VCC V | Guaranteed Limit | | | Unit |
|--|---|----------|------------------|--------|---------|------|
| | | | - 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, Input D to Output Y or Y (Figures 1, 3 and 6) | 2.0 | 185 | 230 | 280 | ns |
| | | 4.5 | 37 | 46 | 56 | |
| | | 6.0 | 31 | 39 | 48 | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, Input A to Output Y or Y (Figures 2 and 6) | 2.0 | 205 | 255 | 310 | ns |
| | | 4.5 | 41 | 51 | 62 | |
| | | 6.0 | 35 | 43 | 53 | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, Strobe to Output Y or Y (Figures 4, 5 and 6) | 2.0 | 125 | 155 | 190 | ns |
| | | 4.5 | 25 | 31 | 38 | |
| | | 6.0 | 21 | 26 | 32 | |
| t _{TLH} , t _{THL} | Maximum Output Transition Time, Any Output (Figures 1 and 6) | 2.0 | 75 | 95 | 110 | ns |
| | | 4.5 | 15 | 19 | 22 | |
| | | 6.0 | 13 | 16 | 19 | |
| C _{in} | Maximum Input Capacitance | — | 10 | 10 | 10 | pF |

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).
- Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

| C _{PD} | Power Dissipation Capacitance (Per Package)* | Typical @ 25°C, VCC = 5.0 V | | pF |
|-----------------|--|-----------------------------|--|----|
| | | 36 | | |
| | | | | |

* Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

PIN DESCRIPTIONS**INPUTS****D0, D1, ... , D7 (Pins 4, 3, 2, 1, 15, 14, 13, 12)**

Data inputs. Data on any one of these eight binary inputs may be selected to appear on the output.

CONTROL INPUTS**A0, A1, A2 (Pins 11, 10, 9)**

Address inputs. The data on these pins are the binary address of the selected input (see the Function Table).

Strobe (Pin 7)

Strobe. This input pin must be at a low level for the selected data to appear at the outputs. If the Strobe pin is high, the Y output is forced to a low level and the Y output is forced to a high level.

OUTPUTS**Y, \bar{Y} (Pins 5, 6)**

Data outputs. The selected data is presented at these pins in both true (Y output) and complemented (\bar{Y} output) forms.

SWITCHING WAVEFORMS

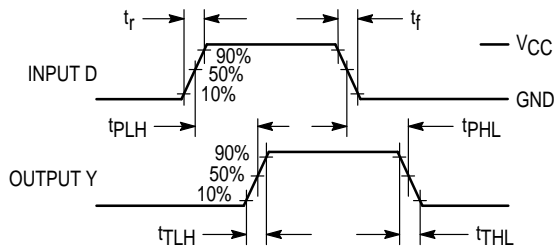


Figure 1.

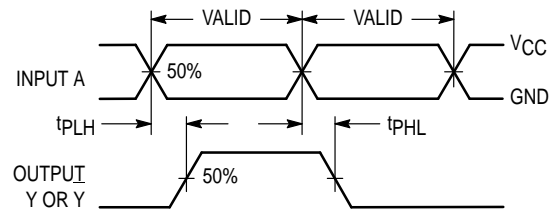


Figure 2.

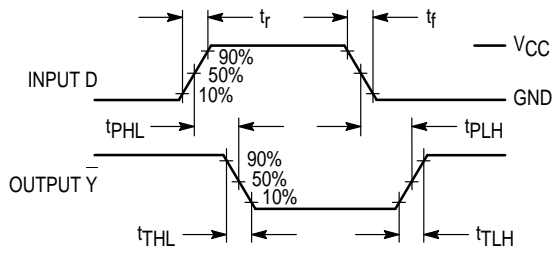


Figure 3.

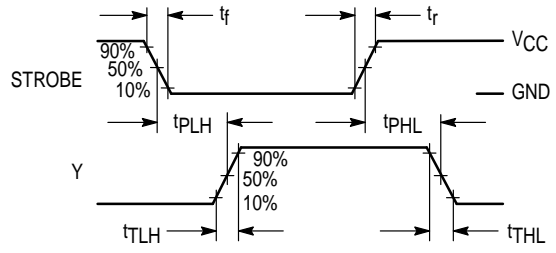


Figure 4.

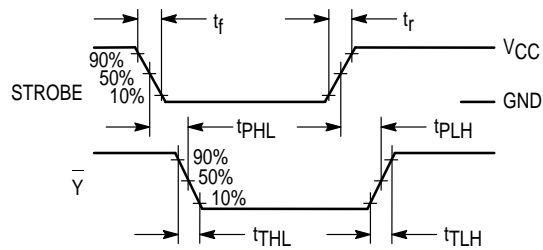
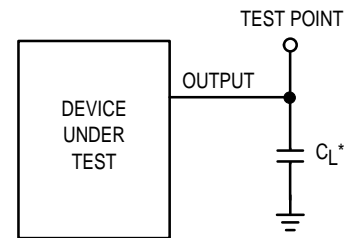


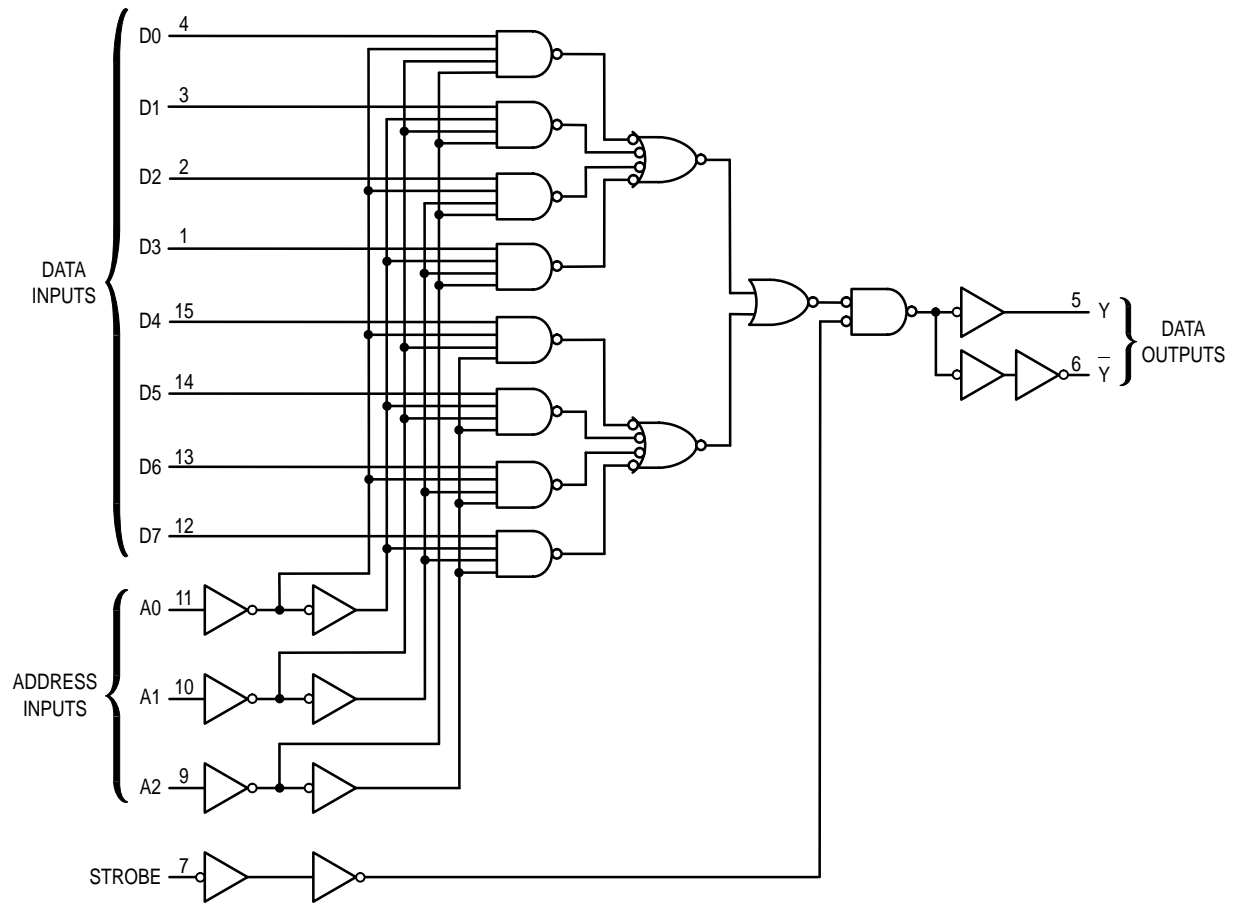
Figure 5.



* Includes all probe and jig capacitance

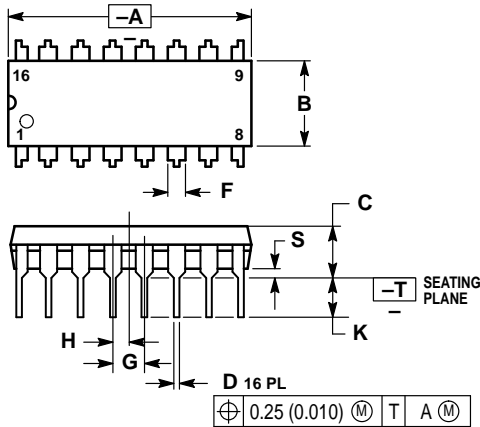
Figure 6. Test Circuit

EXPANDED LOGIC DIAGRAM



OUTLINE DIMENSIONS

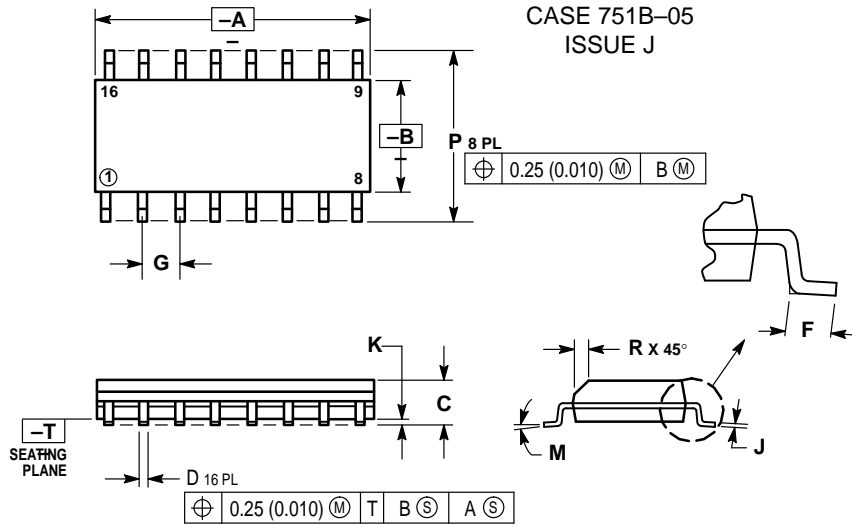
N SUFFIX
PLASTIC PACKAGE
CASE 648-08
ISSUE R



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
 5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.740 | 0.770 | 18.80 | 19.55 |
| B | 0.250 | 0.270 | 6.35 | 6.85 |
| C | 0.145 | 0.175 | 3.69 | 4.44 |
| D | 0.015 | 0.021 | 0.39 | 0.53 |
| F | 0.040 | 0.070 | 1.02 | 1.77 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.050 BSC | | 1.27 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.130 | 2.80 | 3.30 |
| L | 0.295 | 0.305 | 7.50 | 7.74 |
| M | 0° | 10° | 0° | 10° |
| S | 0.020 | 0.040 | 0.51 | 1.01 |

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B-05
ISSUE J



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

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