32 Mbit Concurrent SuperFlash + 2 / 4 Mbit SRAM ComboMemory
SST34HF3223B / SST34HF3243B

Preliminary Information

FEATURES:

- **Flash Organization: Two 1M x16**
- **Quad-Bank Architecture for Concurrent Read-While-Write Operation**
  - 12 Mbit + 4 Mbit + 12 Mbit + 4 Mbit
- **SRAM Organization:**
  - 2 Mbit: 256K x8 or 128K x16
  - 4 Mbit: 512K x8 or 256K x16
- **Single 2.7-3.3V Read-While-Write Operations**
- **Superior Reliability**
  - Endurance: 100,000 Cycles (typical)
  - Greater than 100 years Data Retention
- **Low Power Consumption:**
  - Active Current: 35 mA (typical)
  - Standby Current: 25 µA (typical)
- **Sector-Erase Capability**
  - Uniform 1 KWord sectors
- **Block-Erase Capability**
  - Uniform 32 KWord blocks
- **Read Access Time**
  - Flash: 70 and 90 ns
  - SRAM: 70 and 90 ns
- **Latched Address and Data**
- **Fast Erase and Word-Program:**
  - Sector-Erase Time: 18 ms (typical)
  - Block-Erase Time: 18 ms (typical)
  - Chip-Erase Time: 70 ms (typical)
  - Word-Program Time: 14 µs (typical)
  - Chip Rewrite Time: 30 seconds (typical)
- **Automatic Write Timing**
  - Internal V_{PP} Generation
- **End-of-Write Detection**
  - Toggle Bit
  - Data# Polling
- **CMOS I/O Compatibility**
- **JEDEC Standard Command Set**
- **Packages Available**
  - 56-ball LFBGA (10mm x 12mm x 1.4mm)

PRODUCT DESCRIPTION

The SST34HF3223B/3243B ComboMemory devices integrate four CMOS flash memory banks with a 256K x8 / 128K x16 or 512K x8 / 256K x16 CMOS SRAM memory bank in a Multi-Chip Package (MCP). These devices are fabricated using SST's proprietary, high-performance CMOS SuperFlash technology incorporating the split-gate cell design and thick oxide tunneling injector to attain better reliability and manufacturability compared with alternate approaches. The SST34HF3223B/3243B devices are ideal for applications such as cellular phones, PDAs and other portable electronic devices in a low power and small form factor system.

The SST34HF3223B/3243B features multiple flash memory bank architecture allowing for concurrent operations between the four flash memory banks and the SRAM. The devices can read data from either bank while an Erase or Program operation is in progress in the opposite bank. The four flash memory banks are partitioned as two 12 Mbit and two 4 Mbit for storing boot code, program code, configuration/parameter data and user data.

The SuperFlash technology provides fixed Erase and Program times, independent of the number of Erase/Program cycles that have occurred. Therefore, the system software or hardware does not have to be modified or de-rated as is necessary with alternative flash technologies, whose Erase and Program times increase with accumulated Erase/Program cycles. The SST34HF3223B/3243B devices offer a typical endurance of 100,000 cycles. Data retention is rated at greater than 100 years. With high performance Word-Program, the flash memory banks provide a typical Word-Program time of 14 µsec. The entire flash memory bank can be erased and programmed word-by-word in typically 30 seconds for the SST34HF3223B/3243B, when using interface features such as Toggle Bit or Data# Polling to indicate the completion of Program operation. To protect against inadvertent flash write, the SST34HF3223B/3243B devices contain on-chip hardware and software data protection schemes.

The flash and SRAM operate as two independent memory banks with respective bank enable signals. The memory bank selection is done by two bank enable signals. The SRAM bank enable signal, BES1# and BES2, selects the SRAM bank. The flash memory bank enable signal, BEF# (BEF1# or BEF2#), has to be used with Software Data Protection (SDP) command sequence when controlling the Erase and Program operations in the flash memory bank. The memory banks are superimposed in the same memory address space where they share common address lines, data lines, WE# and OE# which minimize power consumption and area.

Designed, manufactured, and tested for applications requiring low power and small form factor, the SST34HF3223B/3243B are offered in both commercial and extended temperatures and a small footprint package to meet board space constraint requirements.

Device Operation

The SST34HF3223B/3243B uses BES1#, BES2 and BEF# (BEF1# or BEF2#) to control operation of either the flash or the SRAM memory bank. When BEF# (BEF1# or BEF2#) is low, the flash bank is activated for Read, Program or Erase operation. When BES1# is low, and BES2 is high the SRAM is activated for Read and Write operation. BEF# (BEF1# or BEF2#) and BES1# cannot be at low level, and BES2 cannot be at high level at the same time. If all bank enable signals are asserted, bus contention will result and the device may suffer permanent damage. All address, data, and control lines are shared by flash and SRAM memory banks which minimizes power consumption and loading. The device goes into standby when BEF# (BEF1# and BEF2#) and BES1# bank enables are raised to V_{IHC} (Logic High) or when BEF# (BEF1# and BEF2#) are high and BES2 is low.

Concurrent Read/Write Operation

Quadruple bank architecture of SST34HF3223B/3243B devices allows the Concurrent Read/Write operation whereby the user can read from one bank while Program or Erase in the other bank. This operation can be used when the user needs to read system code in one bank while updating data in the other bank. See Figure 1 for Quad-Bank Memory Organization.

Flash Read Operation

The Read operation of the SST34HF3223B/3243B is controlled by BEF# (BEF1# or BEF2#) and OE#, both have to be low for the system to obtain data from the outputs. BEF# (BEF1# or BEF2#) is used for device selection. When BEF# (BEF1# or BEF2#) is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either BEF# (BEF1# or BEF2#) or OE# is high. Refer to the Read cycle timing diagram for further details (Figure 7).

Flash Word-Program Operation

The SST34HF3223B/3243B are programmed on a word-by-word basis. Before the Program operation, the memory must be erased first. The Program operation consists of three steps. The first step is the three-byte load sequence for Software Data Protection. The second step is to load word address and word data. During the Word-Program operation, the addresses are latched on the falling edge of either BEF# (BEF1# or BEF2#) or WE#, whichever occurs last. The data is latched on the rising edge of either BEF# (BEF1# or BEF2#) or WE#, whichever occurs first. The third step is the internal Program operation which is initiated after the rising edge of the fourth WE# or BEF# (BEF1# or BEF2#), whichever occurs first. The Program operation, once initiated, will be completed (typically) within 10 µs. See Figures 8 and 9 for WE# and BEF# (BEF1# or BEF2#) controlled Program operation timing diagrams and Figure 22 for flowcharts. During the Program operation, the only valid reads are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any commands issued during the internal Program operation are ignored.

Flash Sector/Block-Erase Operation

The Sector/Block-Erase operation allows the system to erase the device on a sector-by-sector or block-by-block basis. The SST34HF3223B/3243B offer both Sector-Erase and Block-Erase mode. The sector architecture is based on uniform sector size of 1 KWord. The Block-Erase mode is based on uniform block size of 32 KWord. The Sector-Erase operation is initiated by executing a six-byte command sequence with Sector-Erase command (30H) and sector address (SA) in the last bus cycle. The Block-Erase operation is initiated by executing a six-byte command sequence with Block-Erase command (50H) and block address (BA) in the last bus cycle. The sector or block address is latched on the falling edge of the sixth WE# pulse, while the command (30H or 50H) is latched on the rising edge of the sixth WE# pulse. The internal Erase operation begins after the sixth WE# pulse. See Figures 13 and 14 for timing waveforms. Any commands issued during the Sector- or Block-Erase operation are ignored.

Flash Chip-Erase Operation

The SST34HF3223B/3243B provide a Chip-Erase operation, which allows the user to erase all unprotected sectors/blocks to the “1” state. This is useful when the device must be quickly erased.

The Chip-Erase operation is initiated by executing a six-byte command sequence with Chip-Erase command (10H) at address 5555H in the last byte sequence. The Erase operation begins with the rising edge of the sixth WE# or BEF# (BEF1# or BEF2#), whichever occurs first. The selected flash bank, either BEF1# or BEF2# will complete the Chip-Erase operation. During the Erase operation, the only valid Read is Toggle Bit or Data# Polling. See Table 4

for the command sequence, Figure 12 for timing diagram, and Figure 25 for the flowchart. Any commands issued during the Chip-Erase operation are ignored.

Flash Write Operation Status Detection

The SST34HF3223B/3243B provide one hardware and two software means to detect the completion of a Write (Program or Erase) cycle, in order to optimize the system Write cycle time. The hardware detection uses the Ready/Busy# (RY/BY#) pin. The software detection includes two status bits: Data# Polling (DQ_7) and Toggle Bit (DQ_6). The End-of-Write detection mode is enabled after the rising edge of WE#, which initiates the internal Program or Erase operation.

The actual completion of the nonvolatile Write is asynchronous with the system; therefore, either a Ready/Busy# (RY/BY#), Data# Polling (DQ_7), or Toggle Bit (DQ_6) Read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ_7 or DQ_6. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

Ready/Busy# (RY/BY#)

The SST34HF3223B/3243B includes a Ready/Busy# (RY/BY#) output signal that applies to flash Bank 2 only. During any SDP initiated operation, e.g., Erase, Program, CFI or ID Read operation, RY/BY# is actively pulled low, indicating a SDP controlled operation is in progress. The status of RY/BY# is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector-, Block-, or Bank-Erase, the RY/BY# is valid after the rising edge of sixth WE# or (CE#) pulse. RY/BY# is an open drain output that allows several devices to be tied in parallel to V_{DD} via an external pull-up resistor. Ready/Busy# is in high impedance whenever OE# or CE# is high or RST# is low.

Flash Data# Polling (DQ_7)

When the SST34HF3223B/3243B are in the internal Program operation, any attempt to read DQ_7 will produce the complement of the true data. Once the Program operation is completed, DQ_7 will produce true data. Note that even though DQ_7 may have valid data immediately following the completion of an internal Write operation, the remaining data outputs may still be invalid: valid data on the entire data bus will appear in subsequent successive Read cycles. During internal Erase operation, any attempt to read DQ_7 will produce a '0'. Once the internal Erase operation is completed, DQ_7 will produce a '1'. The Data# Polling (DQ_7) is valid after the rising edge of fourth WE# or (BEF1# or BEF2#) pulse for Program operation. For Sector-, Block-, or Chip-Erase, the Data# Polling (DQ_7) is valid after the rising edge of sixth WE# or (BEF1# or BEF2#) pulse. See Figure 10 for Data# Polling (DQ_7) timing diagram and Figure 23 for a flowchart. There is a 1 µs bus recovery time (T_{BR}) required before valid data can be read on the data bus. New commands can be entered immediately after DQ_7 becomes true data.

Flash Toggle Bit (DQ_6)

During the internal Program or Erase operation, any consecutive attempts to read DQ_6 will produce alternating 1s and 0s, i.e., toggling between 1 and 0. When the internal Program or Erase operation is completed, the DQ_6 bit will stop toggling. The device is then ready for the next operation. The Toggle Bit (DQ_6) is valid after the rising edge of fourth WE# or (BEF1# or BEF2#) pulse for Program operation. For Sector-, Block- or Chip-Erase, the Toggle Bit (DQ_6) is valid after the rising edge of sixth WE# or (BEF1# or BEF2#) pulse. See Figure 11 for Toggle Bit timing diagram and Figure 23 for a flowchart. There is a 1 µs bus recovery time (T_{BR}) required before valid data can be read on the data bus. New commands can be entered immediately after DQ_6 no longer toggles.

Data Protection

The SST34HF3223B/3243B provide both hardware and software features to protect nonvolatile data from inadvertent writes.

Hardware Data Protection

Noise/Glitch Protection: A WE# or BEF# (BEF1# or BEF2#) pulse of less than 5 ns will not initiate a Write cycle.

Write Inhibit Mode: Forcing OE# low, BEF# (BEF1# or BEF2#) high, or WE# high will inhibit the Write operation. This prevents inadvertent writes during power-up or power-down.

Hardware Block Protection

The SST34HF3223B/3243B provide a hardware block protection which protects the outermost 4 KWord in Bank 1A. The block is protected when WP# is held low. See Figure 1 for Block-Protection location.

A user can disable block protection by driving WP# high thus allowing erase or program of data into the protected sectors. WP# must be held high prior to issuing the write command and remain stable until after the entire Write operation has completed.

Hardware Reset (RST#)

The RST# pin provides a hardware method of resetting the device to read array data. When the RST# pin is held low for at least T_{RP}, any in-progress operation will terminate and return to Read mode (see Figure 19). When no internal Program/Erase operation is in progress, a minimum period of T_{RHR} is required after RST# is driven high before a valid Read can take place (see Figure 18).

The Erase operation that has been interrupted needs to be reinitiated after the device resumes normal operation mode to ensure data integrity.

Software Data Protection (SDP)

The SST34HF3223B/3243B provide the JEDEC standard Software Data Protection scheme for all data alteration operations, i.e., Program and Erase. Any Program operation requires the inclusion of the three-byte sequence. The three-byte load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations, e.g., during the system power-up or power-down. Any Erase operation requires the inclusion of six-byte sequence. The SST34HF3223B/3243B are shipped with the Software Data Protection permanently enabled. See Table 4 for the specific software command codes. During SDP command sequence, invalid commands will abort the device to Read mode within T_{RC}. The contents of DQ_{15}-DQ_8 can be V_{IL} or V_{IH}, but no other value, during any SDP command sequence.

Product Identification

The Product Identification mode identifies the devices as the SST34HF3223B and SST34HF3243B and manufacturer as SST. **This mode may be accessed by software operations only. The hardware device ID Read operation, which is typically used by programmers cannot be used on this device because of the shared lines between flash and SRAM in the multi-chip package. Therefore, application of high voltage to pin A_9 may damage this device**. Users may use the software Product Identification operation to identify the part (i.e., using the device code) when using multiple manufacturers in the same socket. For details, see Tables 3 and 4 for software operation, Figure 15 for the software ID entry and Read timing diagram and Figure 24 for the ID entry command sequence flowchart.

TABLE 1: PRODUCT IDENTIFICATION

	Address	Data
Manufacturer's ID	0000H	00BFH
Device ID		
SST34HF3223B	0001H	2761M
SST34HF3243B	0001H	2761M

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Product Identification Mode Exit

In order to return to the standard Read mode, the Software Product Identification mode must be exited. Exit is accomplished by issuing the Software ID Exit command sequence, which returns the device to the Read mode. This command may also be used to reset the device to the Read mode after any inadvertent transient condition that apparently causes the device to behave abnormally, e.g., not read correctly. Please note that the Software ID Exit command is ignored during an internal Program or Erase operation. See Table 4 for software command codes, Figure 17 for timing waveform and Figure 24 for a flowchart.

SRAM Operation

With BES1# low, BES2 and BEF# (BEF1# and BEF2#) high, the SST34HF3223B operates as 256K x8 or 128K x16 CMOS SRAM, and the SST34HF3243B operates as 512K x8 or 256K x16 CMOS SRAM, with fully static operation requiring no external clocks or timing strobes. The CIOs pin configures the SRAM for x8 or x16 SRAM operation modes. The SST34HF3223B SRAM is mapped into the first 128 KWord address space of the device, and the SST34HF3243B SRAM is mapped into the first 256 KWord address space. When BES1#, BEF# (BEF1# and BEF2#) are high and BES2 is low, all memory banks are deselected and the device enters standby. Read and Write cycle times are equal. The control signals UBS# and LBS# provide access to the upper data byte and lower data byte. See Table 3 for SRAM Read and Write data byte control modes of operation.

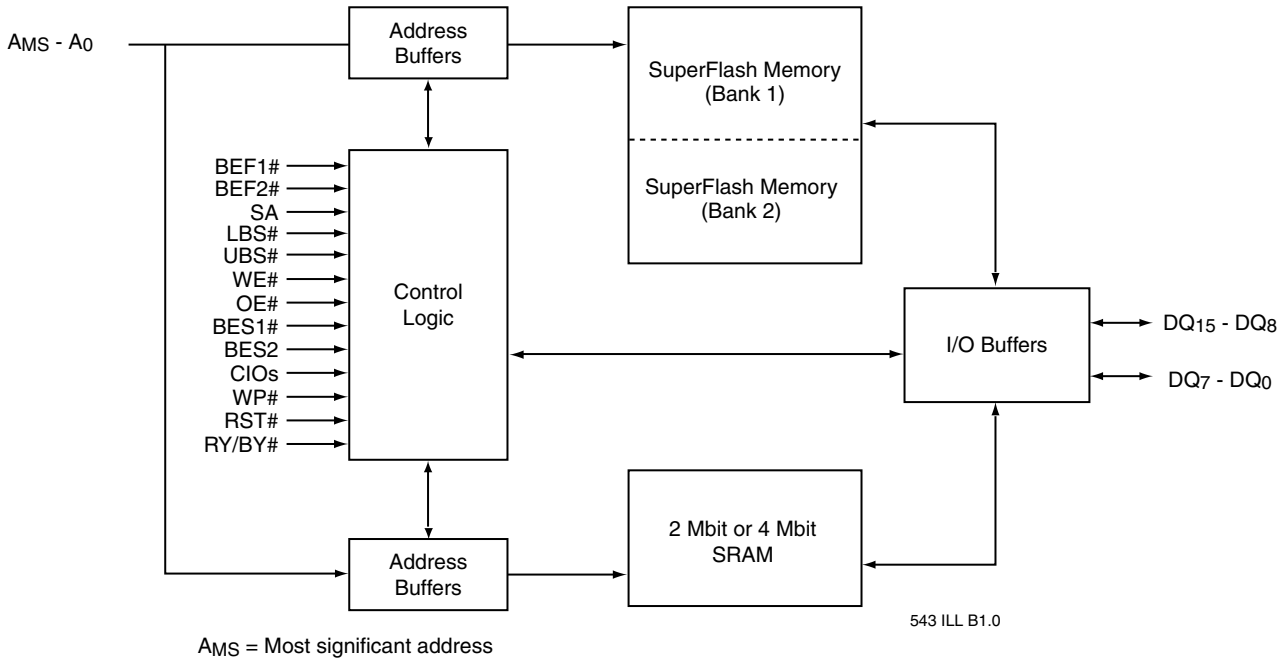
SRAM Read

The SRAM Read operation of the SST34HF3223B/3243B is controlled by OE# and BES1#, both have to be low with WE# and BES2 high for the system to obtain data from the outputs. BES1# and BES2 are used for SRAM bank selection. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when OE# is high. Refer to the Read cycle timing diagram, Figure 4, for further details.

SRAM Write

The SRAM Write operation of the SST34HF3223B/3243B is controlled by WE# and BES1#, both have to be low, BES2 has to be high for the system to write to the SRAM. During the Word-Write operation, the addresses and data are referenced to the rising edge of BES1# or WE# the falling edge of BES2 whichever occur first. The write time is measured from the last falling edge of BES1# or WE# or the rising edge of BES2 to the first rising edge of BES1# or WE# or the falling edge of BES2. Refer to the Write cycle timing diagram, Figures 5 and 6, for further details.

FUNCTIONAL BLOCK DIAGRAM



A_{MS} = Most significant address

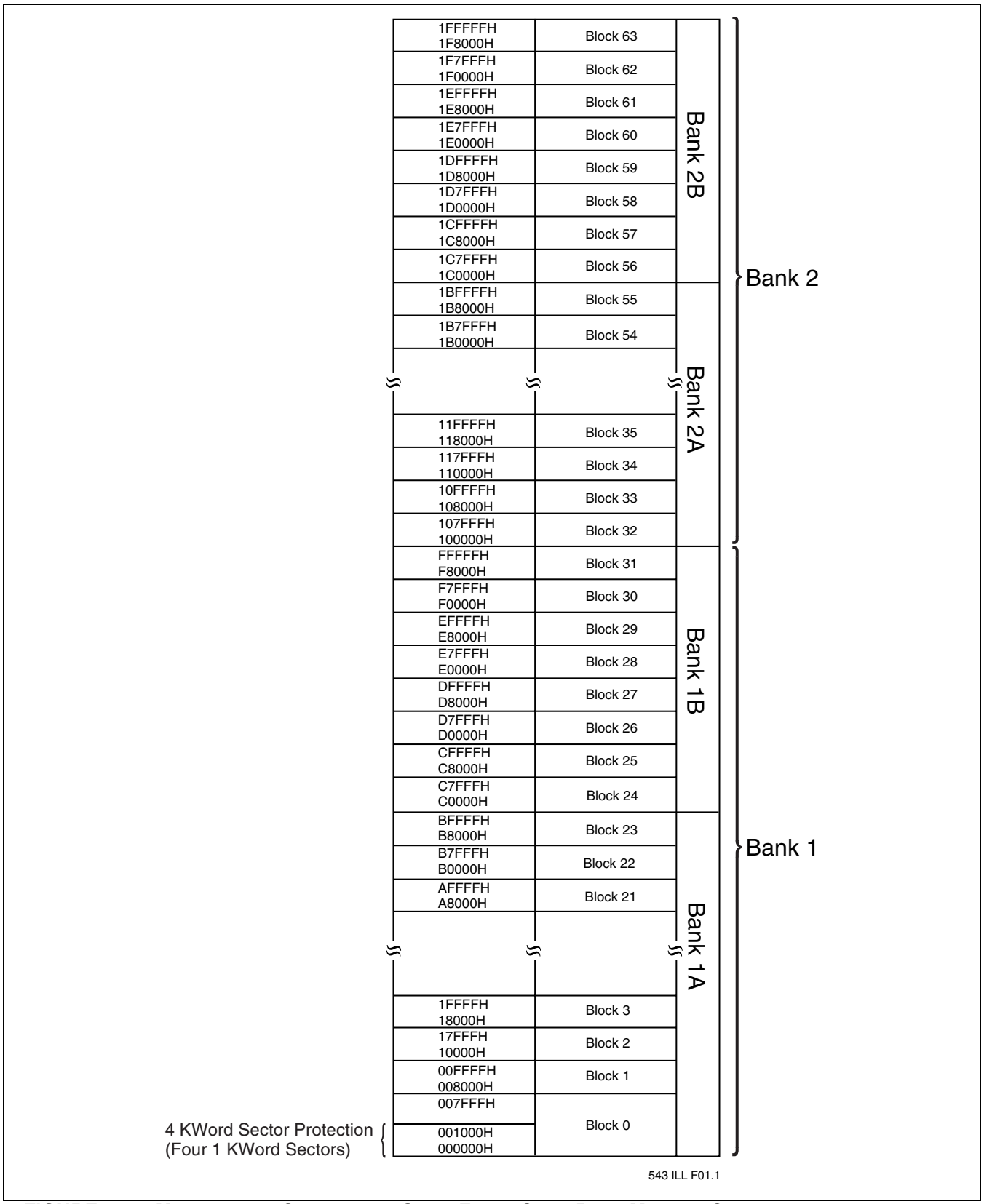


FIGURE 1: 2 MEGABIT X 16 CONCURRENT SUPERFLASH QUAD-BANK MEMORY ORGANIZATION

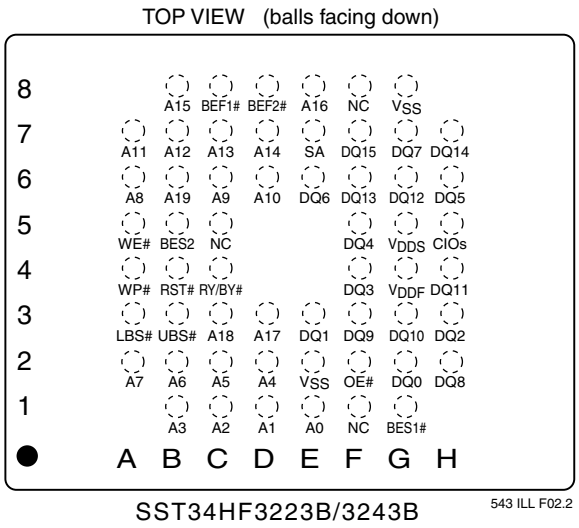


FIGURE 2: PIN ASSIGNMENTS FOR 56-BALL LFBGA (10MM X 12MM)

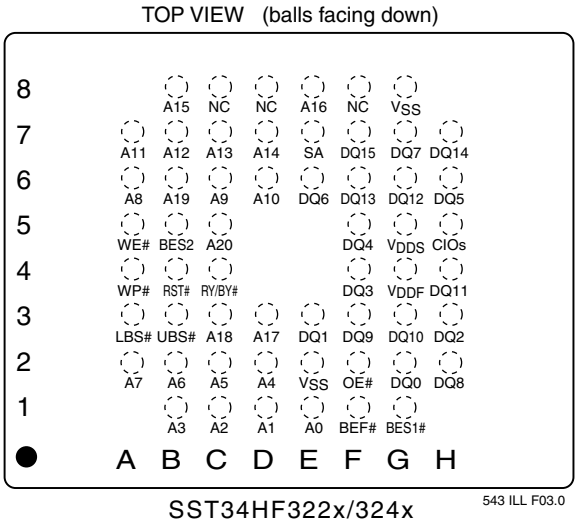


FIGURE 3: PIN ASSIGNMENTS FOR 56-BALL LFBGA (10MM X 12MM) APPLY TO FUTURE SST34HF322X/324X

Note: Please refer to application note, *Design-In SST34HF3223A/3243A/3223B/3243B Devices*, to achieve drop-in replacement when SST34HF322x/324x/328x becomes available.

TABLE 2: PIN DESCRIPTION

Symbol	Pin Name	Functions
A_{MS}[1] to A_0	Address Inputs	To provide flash address, A_{19}-A_0. To provide SRAM address, A_{16}-A_0 for 2M and A_{17}-A_0 for 4M
SA	Address Input (SRAM)	To provide SRAM address input in byte mode (x8). When CIOs is V_{IL}, the SRAM is in byte mode and SA provides the most significant address input. When CIOs is V_{IH}, the SRAM is in Word mode and SA becomes a "Don't Care" pin.
DQ_{15}-DQ_0	Data Inputs/Outputs	To output data during Read cycles and receive input data during Write cycles. Data is internally latched during a flash Erase/Program cycle. The outputs are in tri-state when OE# is high or BES1# is high/BES2 is low, and BEF# (BEF1# and BEF2#) is high.
BEF1#	Flash Memory Bank 1 Enable	To activate the flash memory bank 1 when BEF1# is low
BEF2#	Flash Memory Bank 2 Enable	To activate the flash memory bank 2 when BEF2# is low
BES1#	SRAM Memory Bank Enable	To activate the SRAM memory bank when BES1# is low
BES2	SRAM Memory Bank Enable	To activate the SRAM memory bank when BES2 is high
OE#	Output Enable	To gate the data output buffers
WE#	Write Enable	To control the Write operations
UBS#	Upper Byte Control (SRAM)	To enable DQ_{15}-DQ_8
LBS#	Lower Byte Control (SRAM)	To enable DQ_7-DQ_0
CIOs	I/O Configuration (SRAM)	CIOs = V_{IH} is Word mode (x16), CIOs = V_{IL} is Byte mode (x8)
WP#	Write Protect	To protect and unprotect sectors from Erase or Program operation (for Bank 1 only)
RST#	Reset	To Reset and return the device to Read mode
RY/BY#	Ready/Busy#	To output the status of the Program or Erase operation (for Bank 2 only). RY/BY# is an open drain output, so a 10KΩ-100KΩ pull-up resistor is required to allow RY/BY# to transition high indicating the device is ready to read.
V_{SS}	Ground	
V_{DDF}	Power Supply (flash)	Power Supply to flash only (2.7-3.3V)
V_{DDS}	Power Supply (SRAM)	Power Supply to SRAM only (2.7-3.3V)
NC	No Connection	Unconnected pins

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1. A_{MS} = Most Significant Address

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TABLE 3: OPERATIONAL MODES SELECTION

Mode	BEF#[1]	BES1#	BES2[2]	CIOs[3]	OE#	WE#	SA	LBS#	UBS#	DQ_{7-0}	DQ_{15-8}
Flash Read	V_{IL}	V_{IH}	X[4]	X	V_{IL}	V_{IH}	X	X	X	D_{OUT}	D_{OUT}
		X	V_{IL}								
Flash Write	V_{IL}	V_{IH}	X	X	V_{IH}	V_{IL}	X	X	X	D_{IN}	D_{IN}
		X	V_{IL}								
Flash Erase	V_{IL}	V_{IH}	X	X	V_{IH}	V_{IL}	X	X	X	X	X
		X	V_{IL}								
SRAM Read	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IH}	X	V_{IL}	V_{IL}	D_{OUT}	D_{OUT}
							X	V_{IH}	V_{IL}	HIGH-Z	D_{OUT}
							X	V_{IL}	V_{IH}	D_{OUT}	HIGH-Z
	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	SA	X	X	D_{OUT}	HIGH-Z
SRAM Write	V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	V_{IL}	X	V_{IL}	V_{IL}	D_{IN}	D_{IN}
							X	V_{IH}	V_{IL}	HIGH-Z	D_{IN}
							X	V_{IL}	V_{IH}	D_{IN}	HIGH-Z
	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	V_{IL}	SA	X	X	D_{IN}	HIGH-Z
Full Standby	V_{IH}	V_{IH}	X	X	X	X	X	X	X	HIGH-Z	HIGH-Z
		X	V_{IL}	X	X	X	X	X	X		
Output Disable	V_{IH}	V_{IL}	V_{IH}	X	V_{IH}	V_{IH}	X	X	X	HIGH-Z	HIGH-Z
		V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IH}	X	V_{IH}	V_{IH}		
	V_{IL}	V_{IH}	X	X	V_{IH}	V_{IH}	X	X	X	HIGH-Z	HIGH-Z
		X	V_{IL}								
Product Identification Software Mode	V_{IL}	V_{IH}	X	X	V_{IL}	V_{IH}	X	X	X	Manufacturer's ID[5]	
		X	V_{IL}							Device ID[5]	

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1. BEF# = BEF1# for operations that apply to flash Bank 1.
   BEF# = BEF2# for operations that apply to flash Bank 2.
2. Do not apply BEF# = V_{IL}, BES1# = V_{IL} and BES2 = V_{IH} at the same time
3. SRAM I/O configuration input CIOs; V_{IH} = x16 (Word mode), V_{IL} = x8 (Byte mode)
4. X can be V_{IL} or V_{IH}, but no other value.
5. With A_{19}-A_1 =0; SST Manufacturer's ID = 00BFH, is read with A_0 = 0,
   SST34HF3223B Device ID = 2761H, is read with A_0 = 1.
   SST34HF3243B Device ID = 2761H, is read with A_0 = 1.

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TABLE 4: SOFTWARE COMMAND SEQUENCE

Command Sequence	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]
Word-Program	5555H	AAH	2AAAH	55H	5555H	A0H	WA[3]	Data				
Sector-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA_X[4]	30H
Block-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	BA_X[4]	50H
Chip-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Software ID Entry[5]	5555H	AAH	2AAAH	55H	5555H	90H						
Software ID Exit[5,6]	5555H	AAH	2AAAH	55H	5555H	F0H						

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1. Address format A_{14}-A_0 (Hex), Address A_{19}-A_{15} can be V_{IL} or V_{IH}, but no other value, for Command sequence.
2. DQ_{15}-DQ_8 can be V_{IL} or V_{IH}, but no other value, for Command sequence.
3. WA = Program Word address.
4. SA_X for Sector-Erase; uses A_{19}-A_{11} address lines.
   BA_X for Block-Erase; uses A_{19}-A_{15} address lines.
5. The device does not remain in Software Product Identification Mode if powered down.
6. With A_{20}-A_1 = 0; SST Manufacturer's ID = 00BFH, is read with A_0 = 0
   SST34HF3223B/3243B Device ID = 2761H, is read with A_0 = 1.

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Operating Temperature . . . . . -20°C to +85°C
Storage Temperature . . . . . -65°C to +125°C
D. C. Voltage on Any Pin to Ground Potential . . . . . -0.5V to V_{DD} + 0.3V
Transient Voltage (<20 ns) on Any Pin to Ground Potential . . . . . -1.0V to V_{DD} + 1.0V
Package Power Dissipation Capability (Ta = 25°C) 1.0W
Output Short Circuit Current . . . . . 50 mA

OPERATING RANGE

Range	Ambient Temp	V_{DD}
Commercial	0°C to +70°C	2.7-3.3V
Extended	-20°C to +85°C	2.7-3.3V

AC CONDITIONS OF TEST

Input Rise/Fall Time	5 ns
Output Load	C_L = 30 pF
See Figures 20 and 21	

Preliminary Information

TABLE 5: DC OPERATING CHARACTERISTICS (V_{DD}[1] = 2.7-3.3V)

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{DD}	Active V_{DD} Current				Address input = V_{IL}/V_{IH}, at f=1/T_{RC} Min, V_{DD}=V_{DD} Max, all DQs open
	Read				OE#=V_{IL}, WE#=V_{IH}
	Flash		35	mA	BEF#=V_{IL}, BES1#=V_{IH} or BES2 = V_{IL}
	SRAM		20	mA	BEF#=V_{IH}, BES1#=V_{IL}, BES2 = V_{IH}
	Concurrent Operation		60	mA	BEF#=V_{IH}, BES#=V_{IL}
	Write[2]				WE#=V_{IL}
	Flash		40	mA	BEF#=V_{IL}, BES1#=V_{IH} or BES2 = V_{IL}, OE#=V_{IH}
	SRAM		20	mA	BEF#=V_{IH}, BES1#=V_{IL}, BES2 = V_{IH}
I_{SB}	Standby V_{DD} Current 3.0V		40	µA	V_{DD} = V_{DD} Max, BEF#=BES1#=V_{IHC}
	3.3V		75	µA	BES2 = V_{ILC}
I_{LI}	Input Leakage Current		1	µA	V_{IN}=GND to V_{DD}, V_{DD}=V_{DD} Max
I_{LO}	Output Leakage Current		1	µA	V_{OUT}=GND to V_{DD}, V_{DD}=V_{DD} Max
V_{IL}	Input Low Voltage		0.8	V	V_{DD}=V_{DD} Min
V_{ILC}	Input Low Voltage (CMOS)		0.3	V	
V_{IH}	Input High Voltage	0.7 V_{DD}		V	V_{DD}=V_{DD} Max
V_{IHC}	Input High Voltage (CMOS)	V_{DD}-0.3		V	
V_{OLF}	Flash Output Low Voltage		0.2	V	I_{OL}=100 µA, V_{DD}=V_{DD} Min
V_{OHF}	Flash Output High Voltage	V_{DD}-0.2		V	I_{OH}=-100 µA, V_{DD}=V_{DD} Min
V_{OLS}	SRAM Output Low Voltage		0.4		I_{OL}=1 mA, V_{DD}=V_{DD} Min
V_{OHS}	SRAM Output High Voltage	2.2		V	I_{OH}=-500 µA, V_{DD}=V_{DD} Min

T5.4 543

1. V_{DD} = V_{DDF} and V_{DDS}
2. I_{DD} active while Erase or Program is in progress.

Note: BEF# = BEF1# for operations that apply to flash Bank 1.
BEF2# for operations that apply to flash Bank 2.

TABLE 6: RECOMMENDED SYSTEM POWER-UP TIMINGS

Symbol	Parameter	Minimum	Units
$T_{PU-READ}$	Power-up to Read Operation	100	µs
$T_{PU-WRITE}$	Power-up to Write Operation	100	µs

T6.0 543

TABLE 7: CAPACITANCE (Ta = 25°C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	24 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	12 pF

T7.0 543

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 8: FLASH RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}[1]	Endurance	10,000	Cycles	JEDEC Standard A117
T_{DR}[1]	Data Retention	100	Years	JEDEC Standard A103
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

T8.0 543

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

AC CHARACTERISTICS

TABLE 9: SRAM READ CYCLE TIMING PARAMETERS

Symbol	Parameter	SST34HF3223B/3243B-70		SST34HF3223B/3243B-90		Units
		Min	Max	Min	Max	
T_{RCS}	Read Cycle Time	70		90		ns
T_{AAS}	Address Access Time		70		90	ns
T_{BES}	Bank Enable Access Time		70		90	ns
T_{OES}	Output Enable Access Time		35		45	ns
T_{BYES}	UBS#, LBS# Access Time		70		90	ns
T_{BLZS}[1]	Bank Enable to Active Output	0		0		ns
T_{OLZS}[1]	Output Enable to Active Output	0		0		ns
T_{BYLZS}[1]	UBS#, LBS# to Active Output	0		0		ns
T_{BHZS}[1]	Bank Enable to High-Z Output		25		35	ns
T_{OHZS}[1]	Output Disable to High-Z Output		25		35	ns
T_{BYHZS}[1]	UBS#, LBS# to High-Z Output		35		45	ns
T_{OHS}	Output Hold from Address Change	10		10		ns

T9.0 543

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 10: SRAM WRITE CYCLE TIMING PARAMETERS

Symbol	Parameter	SST34HF3223B/3243B-70		SST34HF3223B/3243B-90		Units
		Min	Max	Min	Max	
T_{WCS}	Write Cycle Time	70		90		ns
T_{BWS}	Bank Enable to End-of-Write	60		80		ns
T_{AWS}	Address Valid to End-of-Write	60		80		ns
T_{ASTS}	Address Set-up Time	0		0		ns
T_{WPS}	Write Pulse Width	60		80		ns
T_{WRS}	Write Recovery Time	0		0		ns
T_{BYWS}	UBS#, LBS# to End-of-Write	60		80		ns
T_{ODWS}	Output Disable from WE# Low		30		40	ns
T_{OEWS}	Output Enable from WE# High	0		0		ns
T_{DSS}	Data Set-up Time	30		40		ns
T_{DHS}	Data Hold from Write Time	0		0		ns

T10.0 543

TABLE 11: FLASH READ CYCLE TIMING PARAMETERS V_{DD} = 2.7-3.3V

Symbol	Parameter	SST34HF3223B/3243B-70		SST34HF3223B/3243B-90		Units
		Min	Max	Min	Max	
T_{RC}	Read Cycle Time	70		90		ns
T_{CE}	Chip Enable Access Time		70		90	ns
T_{AA}	Address Access Time		70		90	ns
T_{OE}	Output Enable Access Time		35		45	ns
T_{CLZ}[1]	CE# Low to Active Output	0		0		ns
T_{OLZ}[1]	OE# Low to Active Output	0		0		ns
T_{CHZ}[1]	CE# High to High-Z Output		20		30	ns
T_{OHZ}[1]	OE# High to High-Z Output		20		30	ns
T_{OH}[1]	Output Hold from Address Change	0		0		ns
T_{RP}[1]	RST# Pulse Width	500		500		ns
T_{RHR}[1]	RST# High before Read	50		50		ns
T_{RY}[1,2]	RST# Pin Low to Read Mode		150		150	µs

T11.6 543

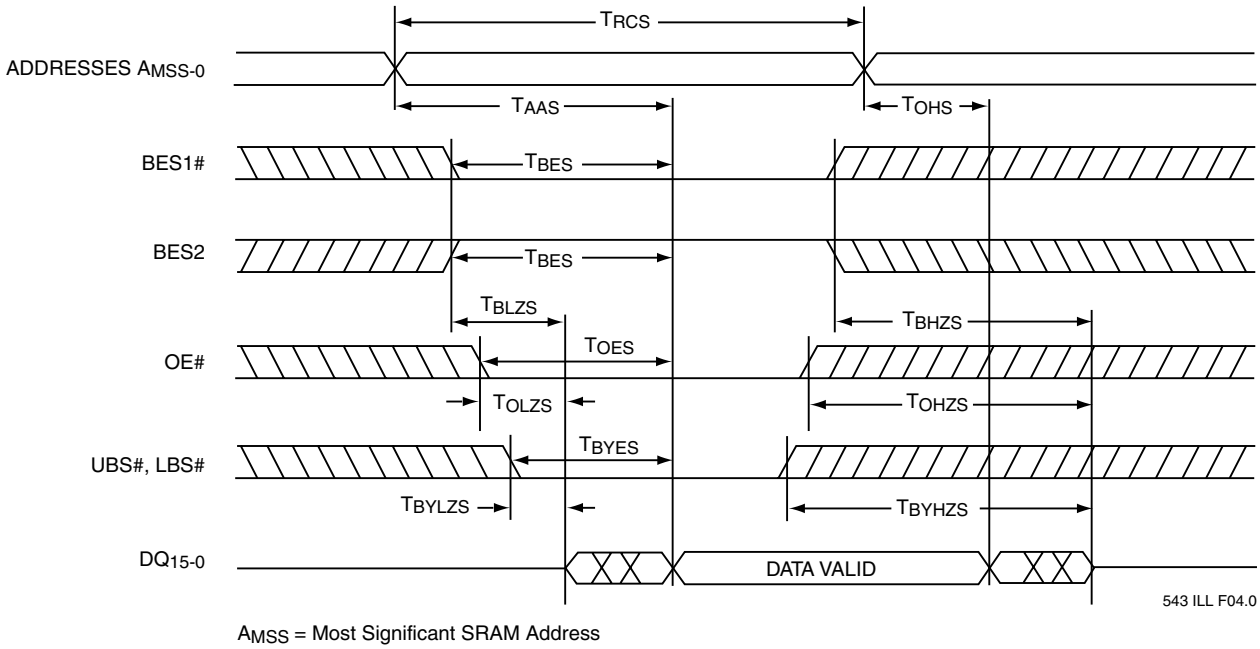
1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.
2. This parameter applies to Sector-Erase, Block-Erase, and Program operations. This parameter does not apply to Chip-Erase.

TABLE 12: FLASH PROGRAM/ERASE CYCLE TIMING PARAMETERS

Symbol	Parameter	Min	Max	Units
T_{BP}	Word-Program Time		20	µs
T_{AS}	Address Setup Time	0		ns
T_{AH}	Address Hold Time	40		ns
T_{CS}	WE# and CE# Setup Time	0		ns
T_{CH}	WE# and CE# Hold Time	0		ns
T_{OES}	OE# High Setup Time	0		ns
T_{OEH}	OE# High Hold Time	10		ns
T_{CP}	CE# Pulse Width	40		ns
T_{WP}	WE# Pulse Width	40		ns
T_{WPH}[1]	WE# Pulse Width High	30		ns
T_{CPH}[1]	CE# Pulse Width High	30		ns
T_{DS}	Data Setup Time	30		ns
T_{DH}[1]	Data Hold Time	0		ns
T_{IDA}[1]	Software ID Access and Exit Time		150	ns
T_{SE}	Sector-Erase		25	ms
T_{BE}	Block-Erase		25	ms
T_{SCE}	Chip-Erase[2]		100	ms
T_{BY}[1,3]	RY/BY# Delay Time	90		ns
T_{BR}[1]	Bus Recovery Time		1	µs

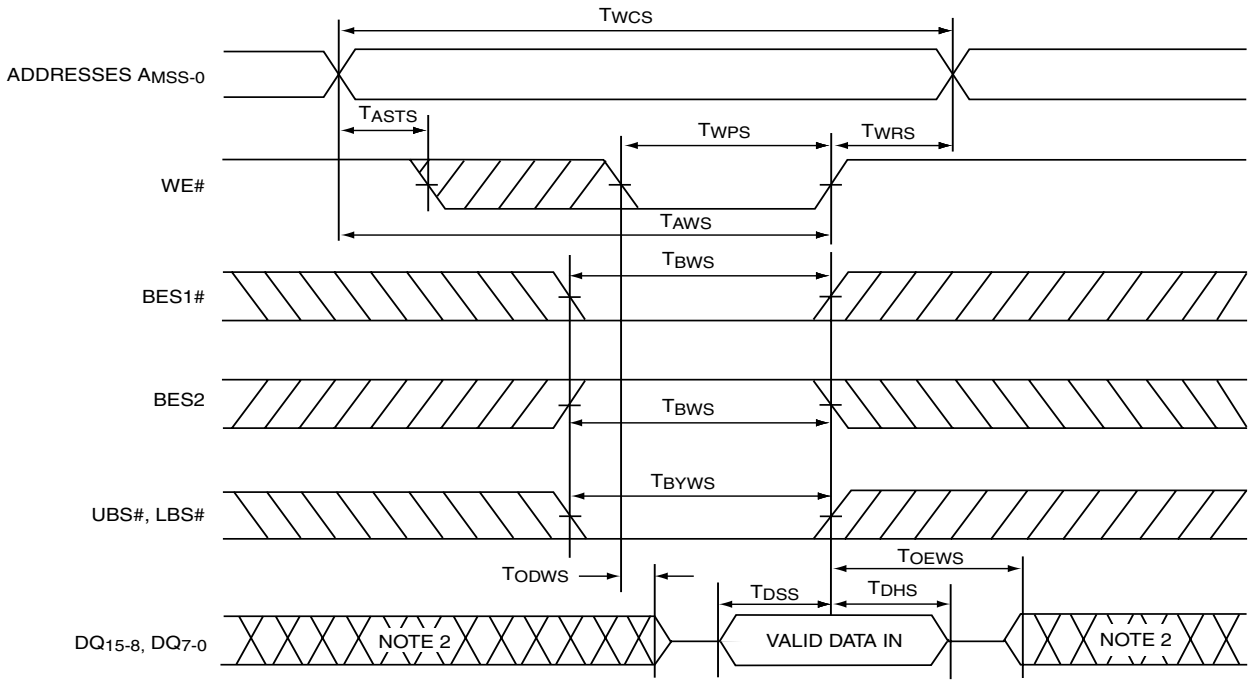
T12.6 543

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.
2. Chip-Erase operation needs to be done to each individual bank (BEF1# and BEF2#).
3. This parameter applies to Sector-Erase, Block-Erase, and Program operations. This parameter does not apply to Chip-Erase.



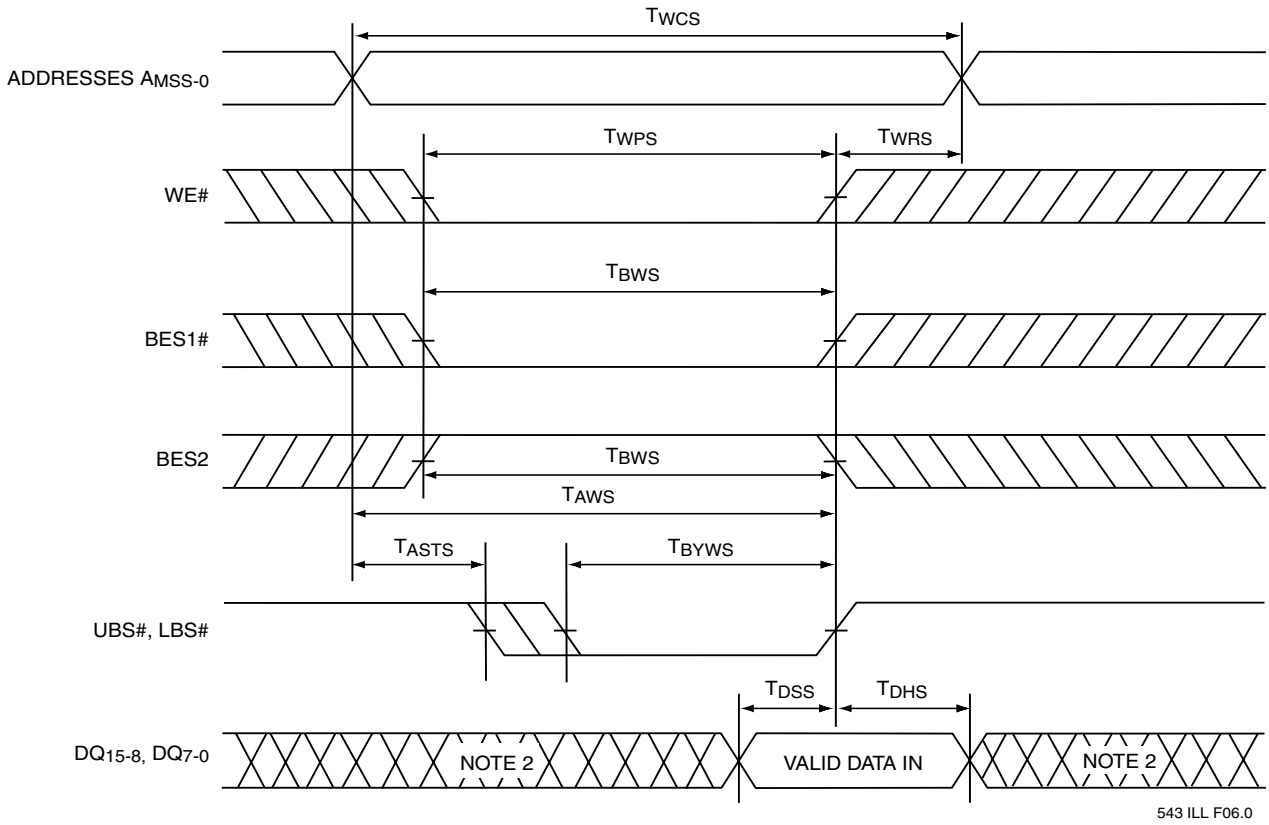
A_{MSS} = Most Significant SRAM Address

FIGURE 4: SRAM READ CYCLE TIMING DIAGRAM



Notes: 1. If OE# is High during the Write cycle, the outputs will remain at high impedance.
2. If BES1# goes Low or BES2 goes High coincident with or after WE# goes Low, the output will remain at high impedance.
If BES1# goes High or BES2 goes Low coincident with or before WE# goes High, the output will remain at high impedance.
Because DIN signals may be in the output state at this time, input signals of reverse polarity must not be applied.

FIGURE 5: SRAM WRITE CYCLE TIMING DIAGRAM (WE# CONTROLLED)[1]



Notes: 1. If OE# is High during the Write cycle, the outputs will remain at high impedance.
2. Because DIN signals may be in the output state at this time, input signals of reverse polarity must not be applied.

FIGURE 6: SRAM WRITE CYCLE TIMING DIAGRAM (UBS#, LBS# CONTROLLED)[1]

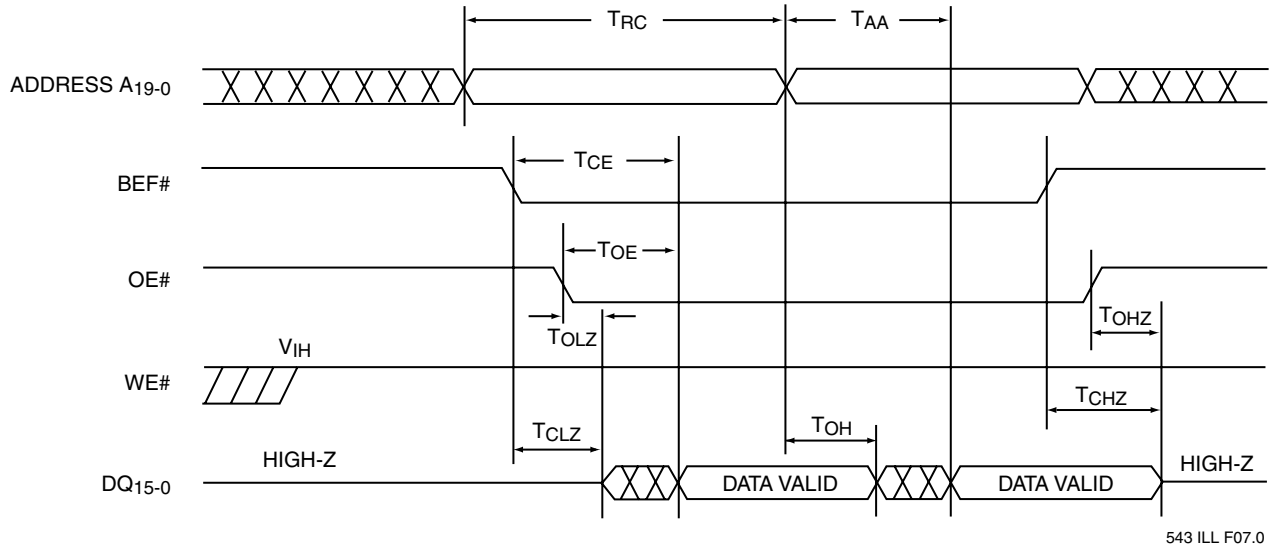
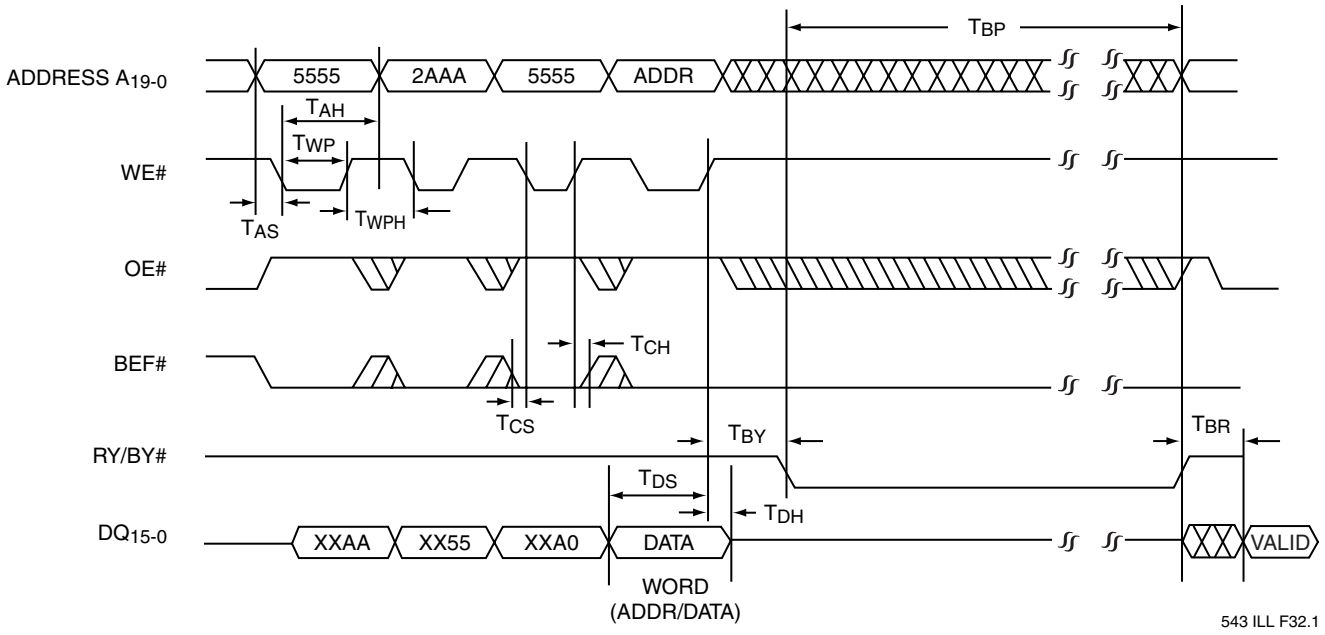
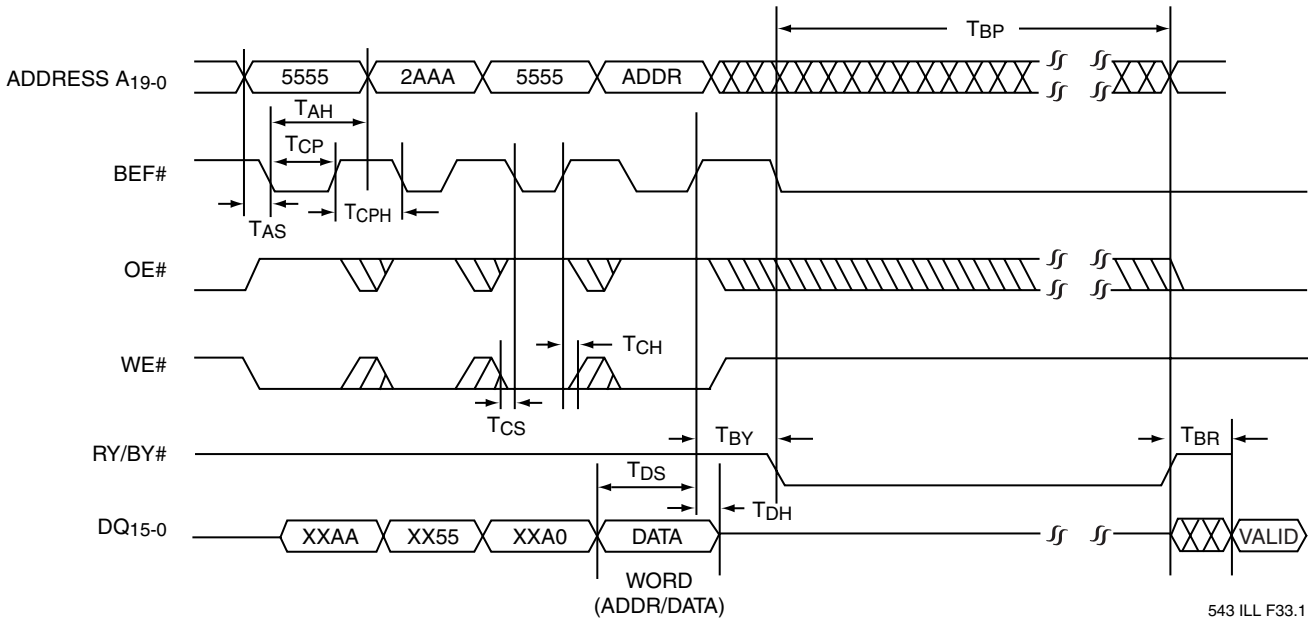


FIGURE 7: FLASH READ CYCLE TIMING DIAGRAM



Note: X can be V_{IL} or V_{IH}, but no other value.

FIGURE 8: FLASH WE# CONTROLLED WORD-PROGRAM CYCLE TIMING DIAGRAM



Note: X can be V_{IL} or V_{IH}, but no other value.

FIGURE 9: FLASH BEF# CONTROLLED WORD-PROGRAM CYCLE TIMING DIAGRAM

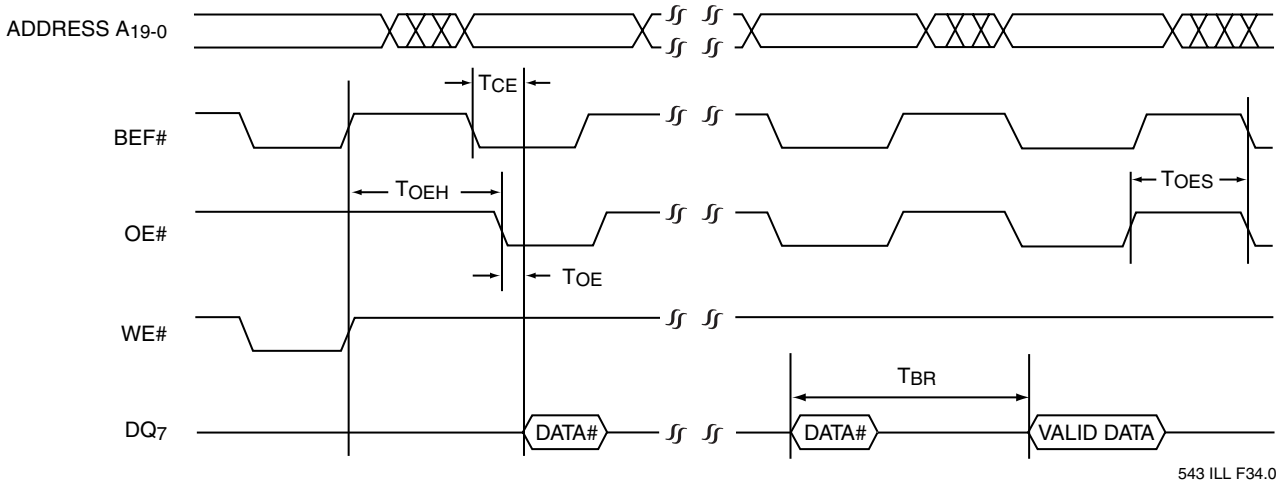


FIGURE 10: FLASH DATA# POLLING TIMING DIAGRAM

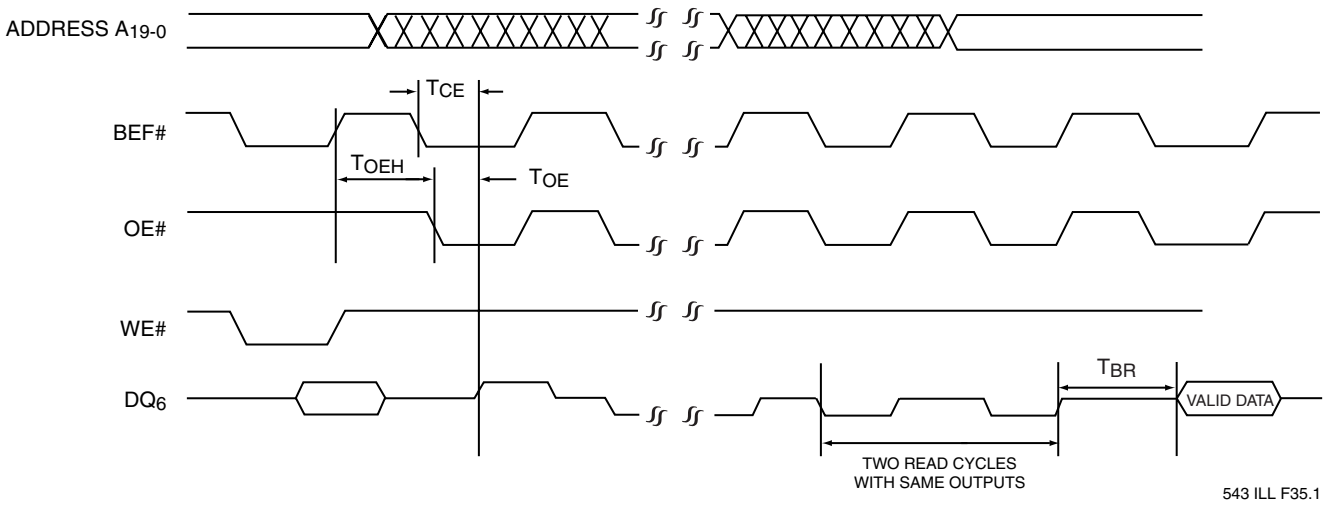
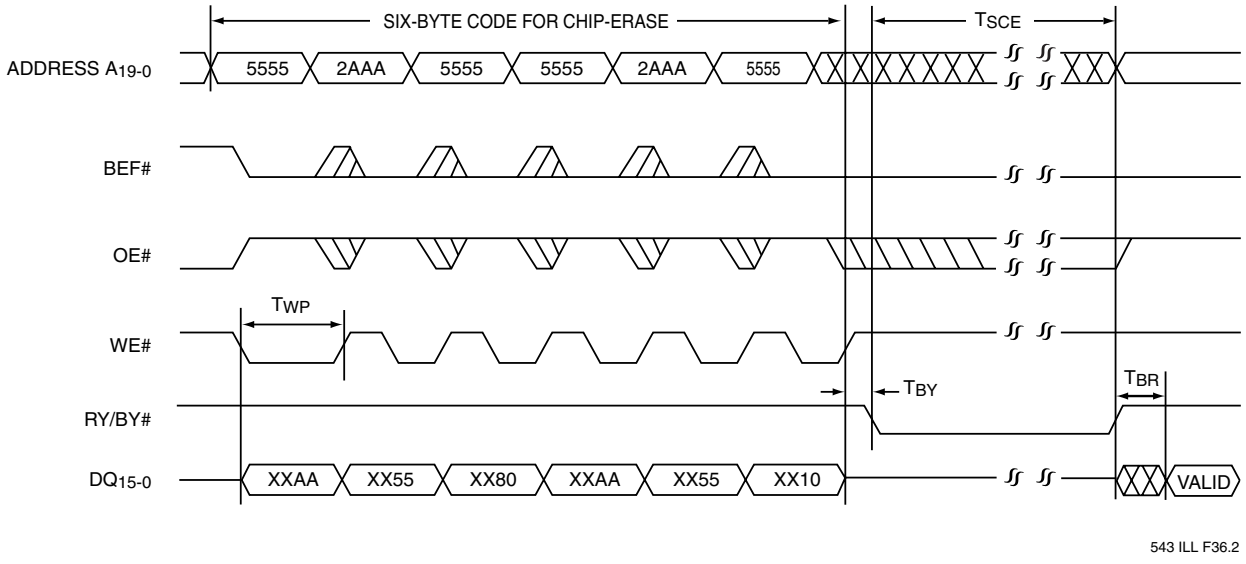
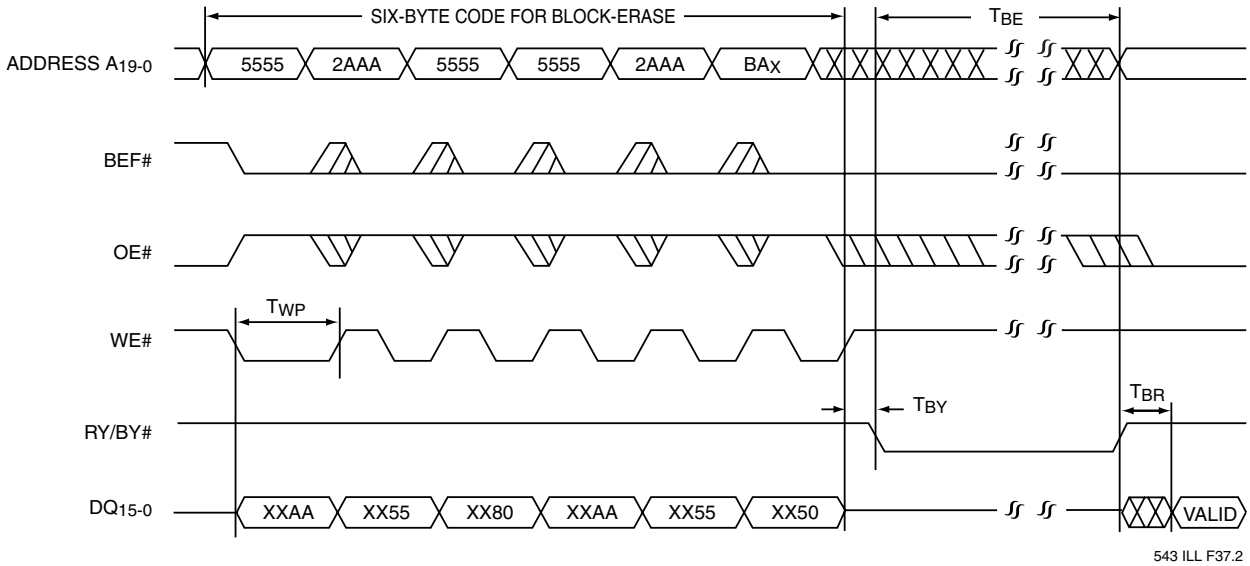


FIGURE 11: FLASH TOGGLE BIT TIMING DIAGRAM



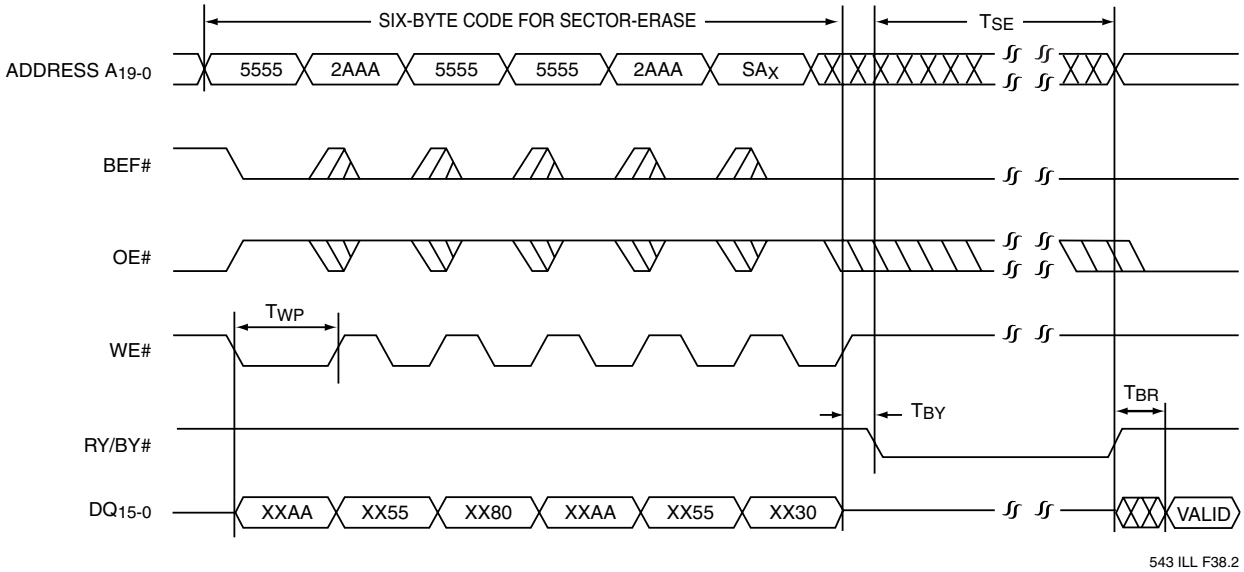
Note: This device also supports BEF# controlled Chip-Erase operation. The WE# and BEF# signals are interchageable as long as minimum timings are met. (See Table 12)
X can be V_{IL} or V_{IH}, but no other value.

FIGURE 12: FLASH WE# CONTROLLED CHIP-ERASE TIMING DIAGRAM



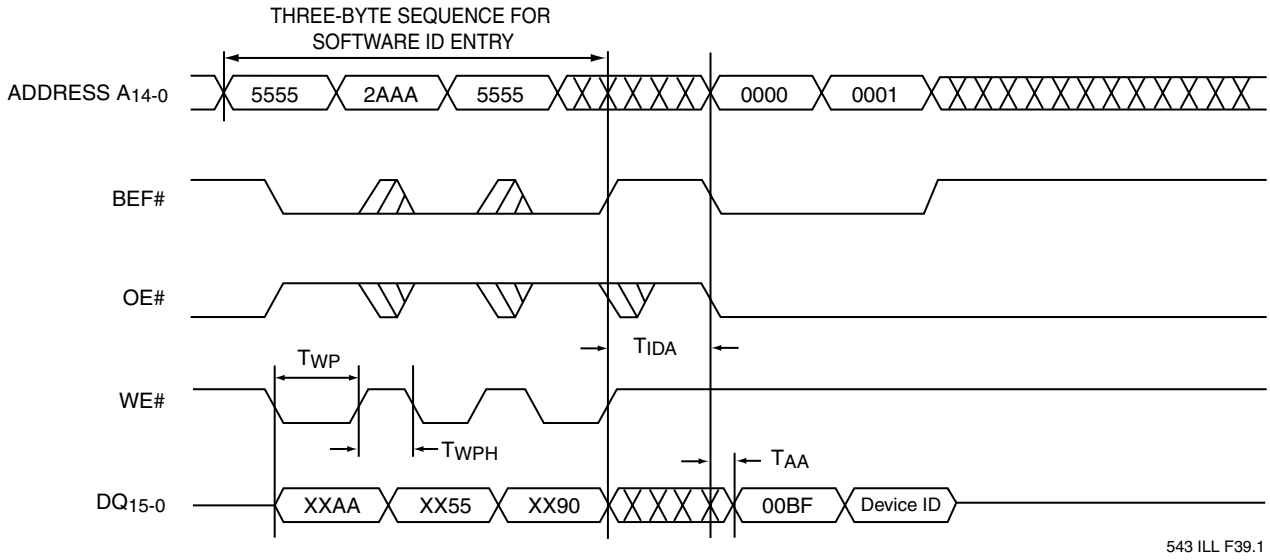
Note: This device also supports BEF# controlled Block-Erase operation. The WE# and BEF# signals are interchageable as long as minimum timings are met. (See Table 12)
BA_X = Block Address
X can be V_{IL} or V_{IH}, but no other value.

FIGURE 13: FLASH WE# CONTROLLED BLOCK-ERASE TIMING DIAGRAM



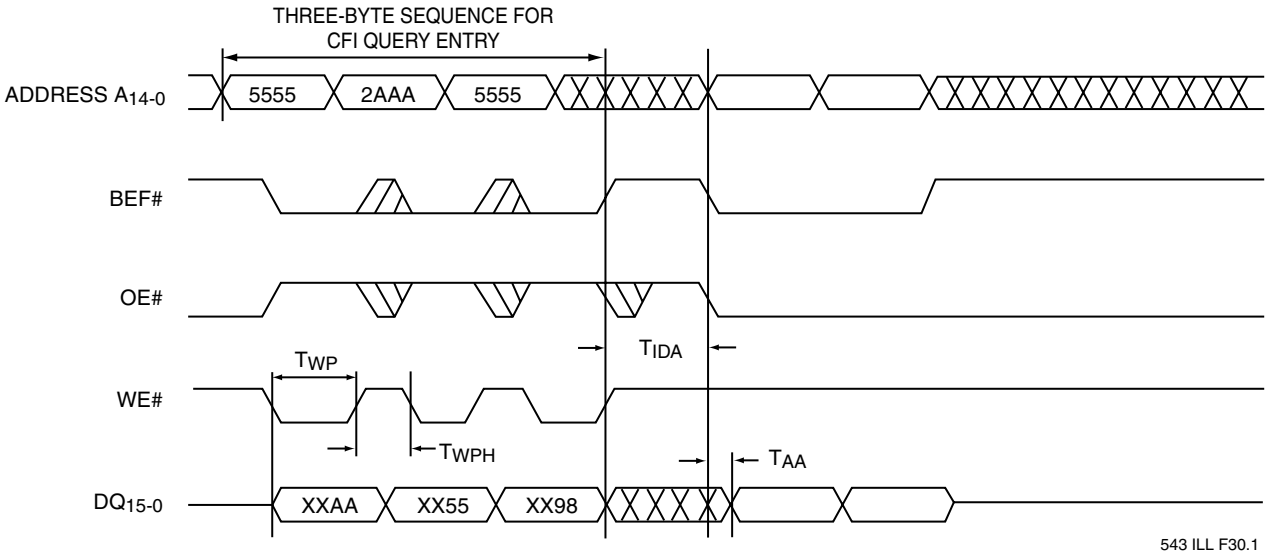
Note: This device also supports BEF# controlled Sector-Erase operation. The WE# and BEF# signals are interchageable as long as minimum timings are met. (See Table 12)
SA_X = Sector Address
X can be V_{IL} or V_{IH}, but no other value.

FIGURE 14: FLASH WE# CONTROLLED SECTOR-ERASE TIMING DIAGRAM



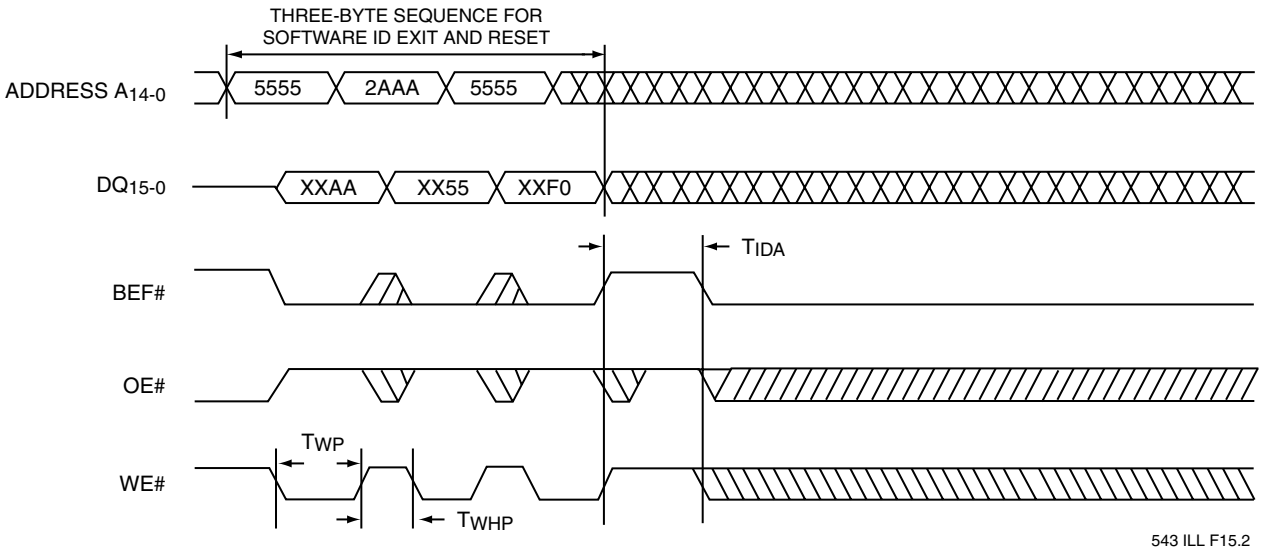
Device ID = 2761H for SST34HF3223B and 2761H for SST34HF3243B
Note: X can be V_{IL} or V_{IH}, but no other value.

FIGURE 15: FLASH SOFTWARE ID ENTRY AND READ



Note: X can be V_{IL} or V_{IH}, but no other value.

FIGURE 16: CFI ENTRY AND READ



Note: X can be V_{IL} or V_{IH}, but no other value.

FIGURE 17: FLASH SOFTWARE ID EXIT/CFI EXIT

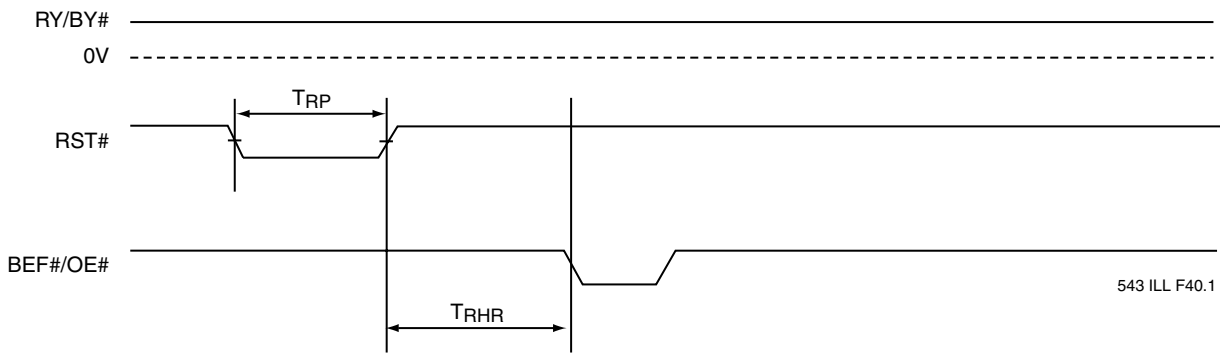


FIGURE 18: RST# TIMING DIAGRAM (WHEN NO INTERNAL OPERATION IS IN PROGRESS)

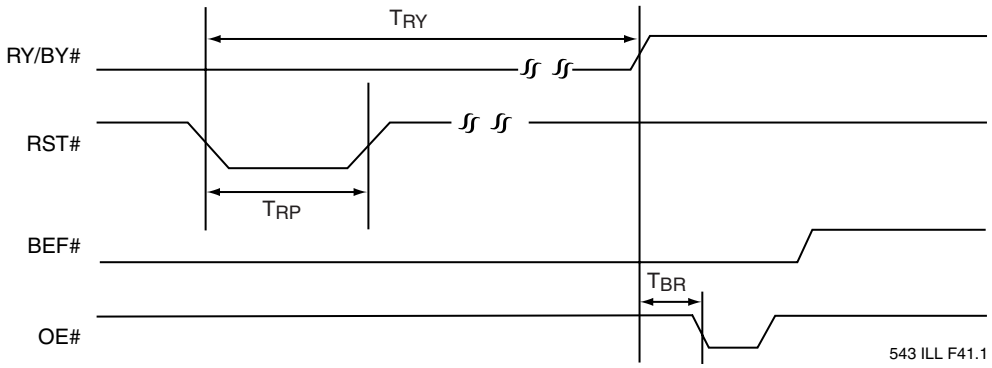
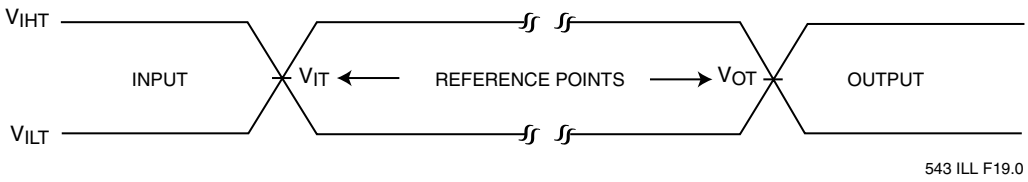


FIGURE 19: RST# TIMING DIAGRAM (DURING SECTOR- OR BLOCK-ERASE OPERATION)



AC test inputs are driven at V_{IHT} (0.9 V_{DD}) for a logic "1" and V_{ILT} (0.1 V_{DD}) for a logic "0". Measurement reference points for inputs and outputs are V_{IT} (0.5 V_{DD}) and V_{OT} (0.5 V_{DD}). Input rise and fall times (10% ↔ 90%) are <5 ns.

Note: V_{IT} - V_{INPUT} Test
V_{OT} - V_{OUTPUT} Test
V_{IHT} - V_{INPUT} HIGH Test
V_{ILT} - V_{INPUT} LOW Test

FIGURE 20: AC INPUT/OUTPUT REFERENCE WAVEFORMS

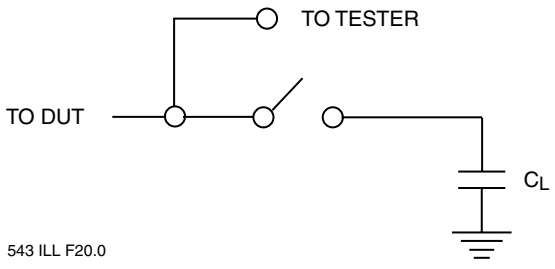
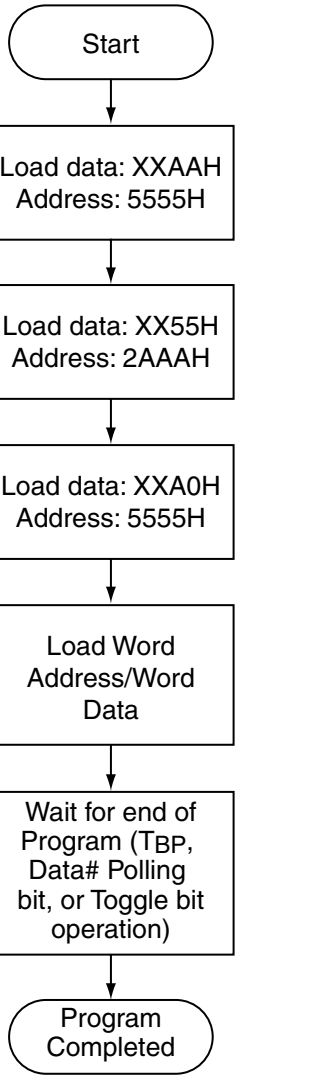


FIGURE 21: A TEST LOAD EXAMPLE



Note: X can be V_{IL} or V_{IH}, but no other value.

FIGURE 22: WORD-PROGRAM ALGORITHM

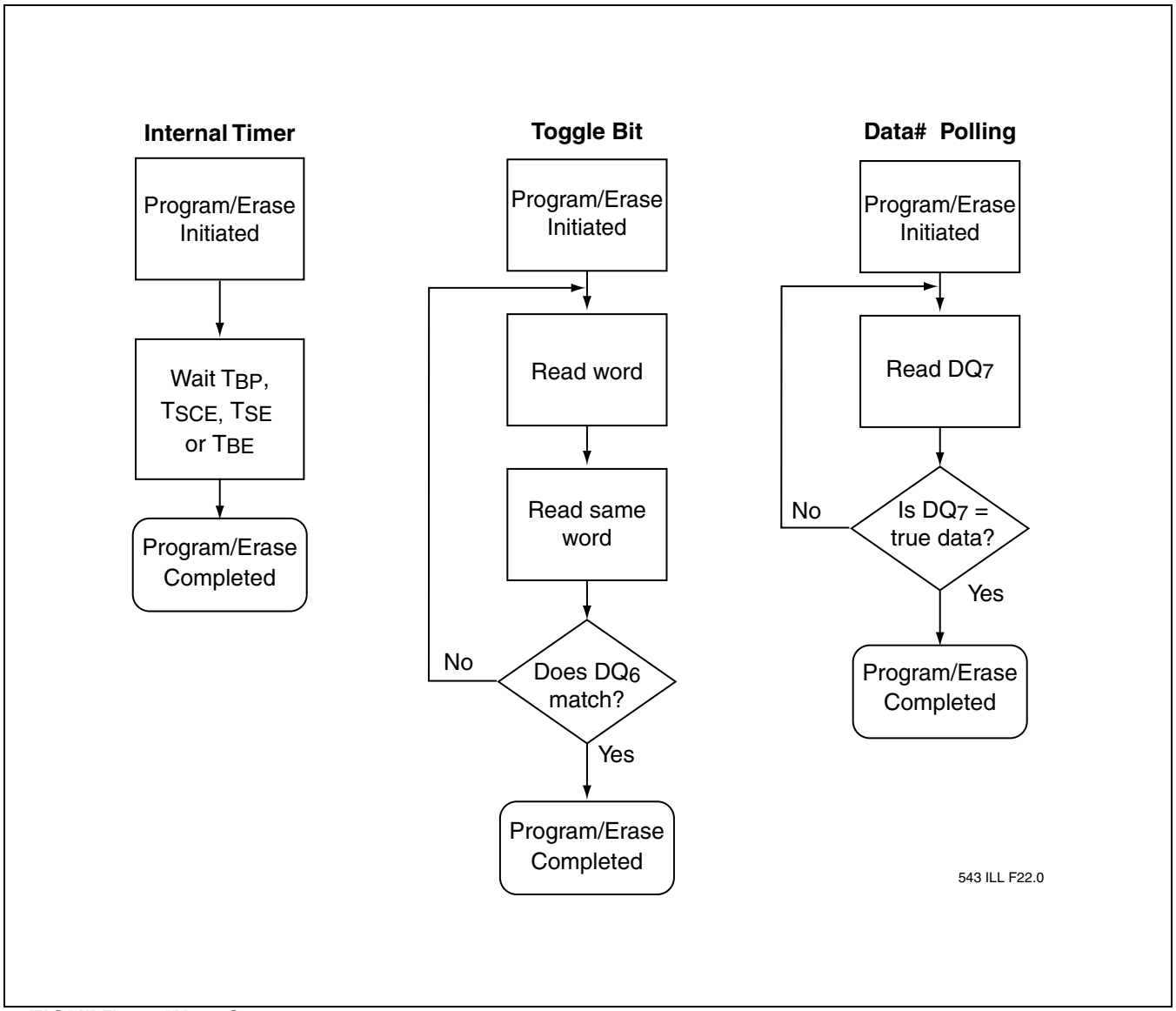
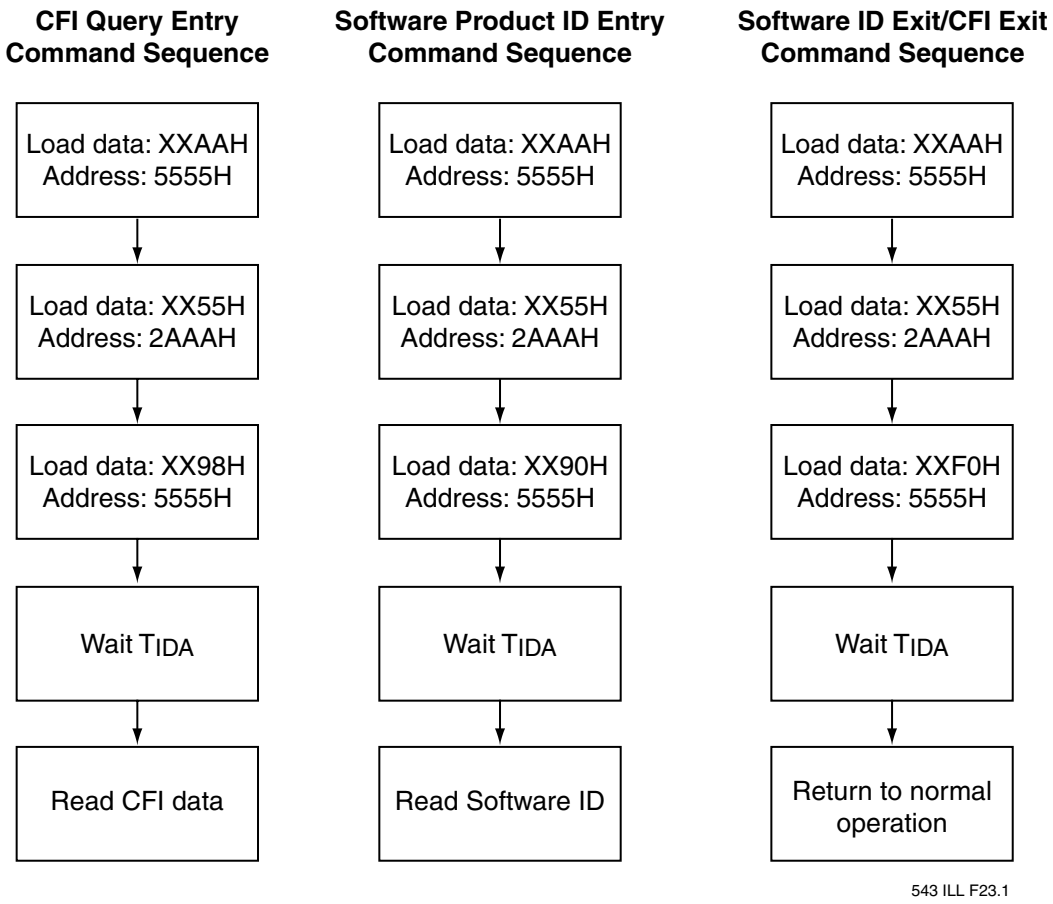
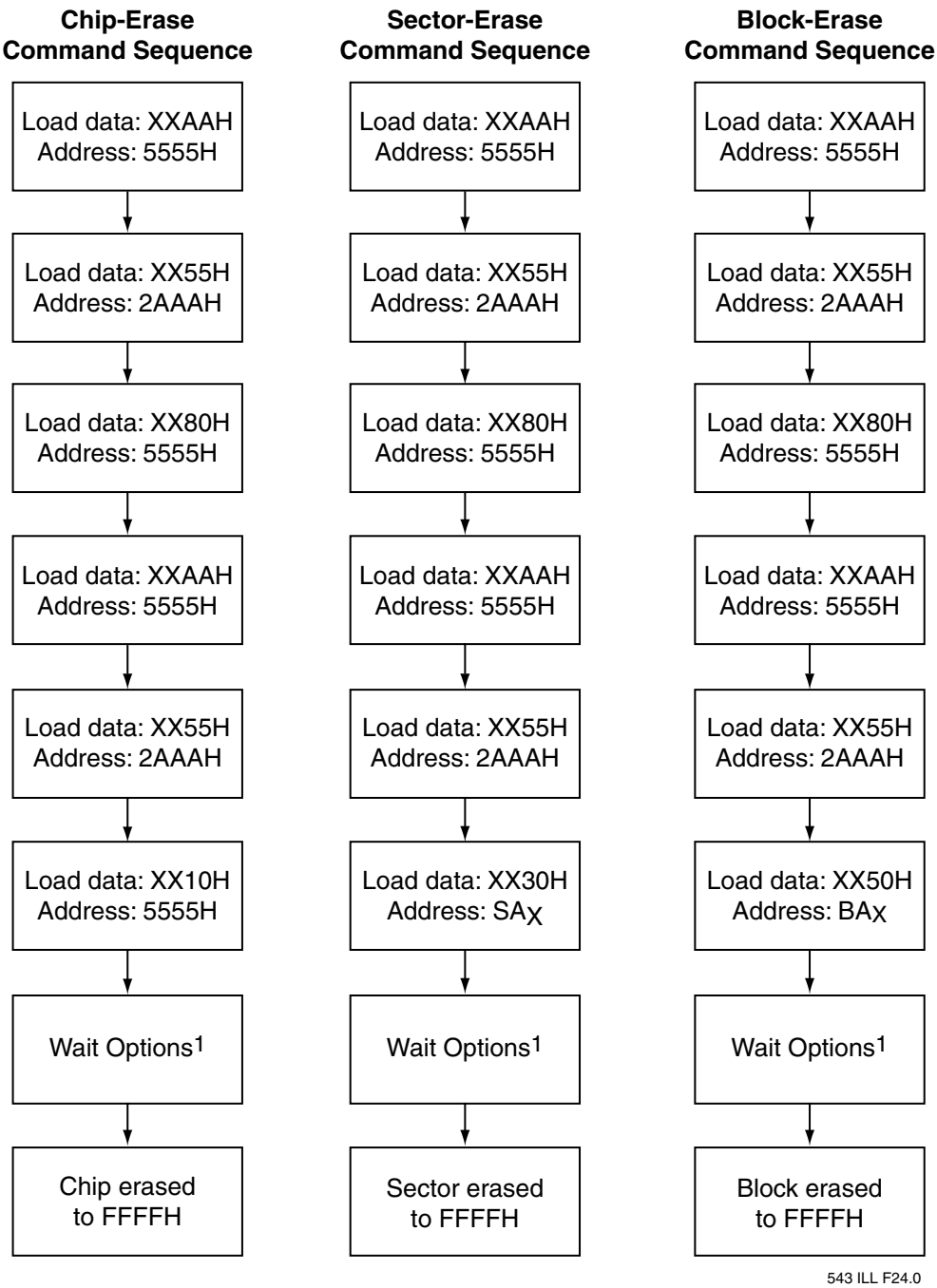


FIGURE 23: WAIT OPTIONS



Note: X can be V_{IL} or V_{IH}, but no other value.

FIGURE 24: SOFTWARE PRODUCT ID/CFI COMMAND FLOWCHARTS



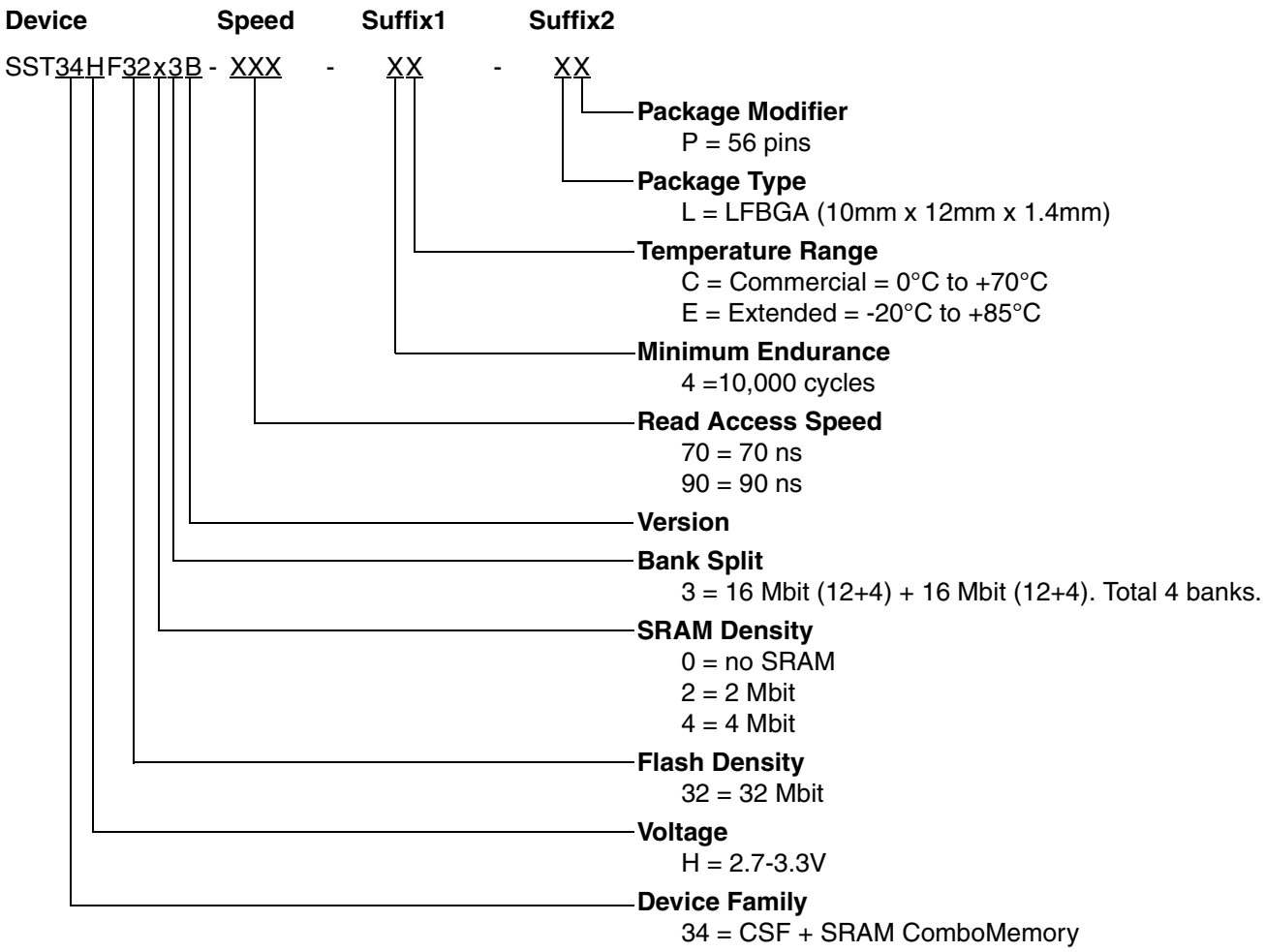
Note: X can be V_{IL} or V_{IH}, but no other value.

Refer to Figure 23

FIGURE 25: ERASE COMMAND SEQUENCE

Preliminary Information

PRODUCT ORDERING INFORMATION



Valid combinations for SST34HF3223B

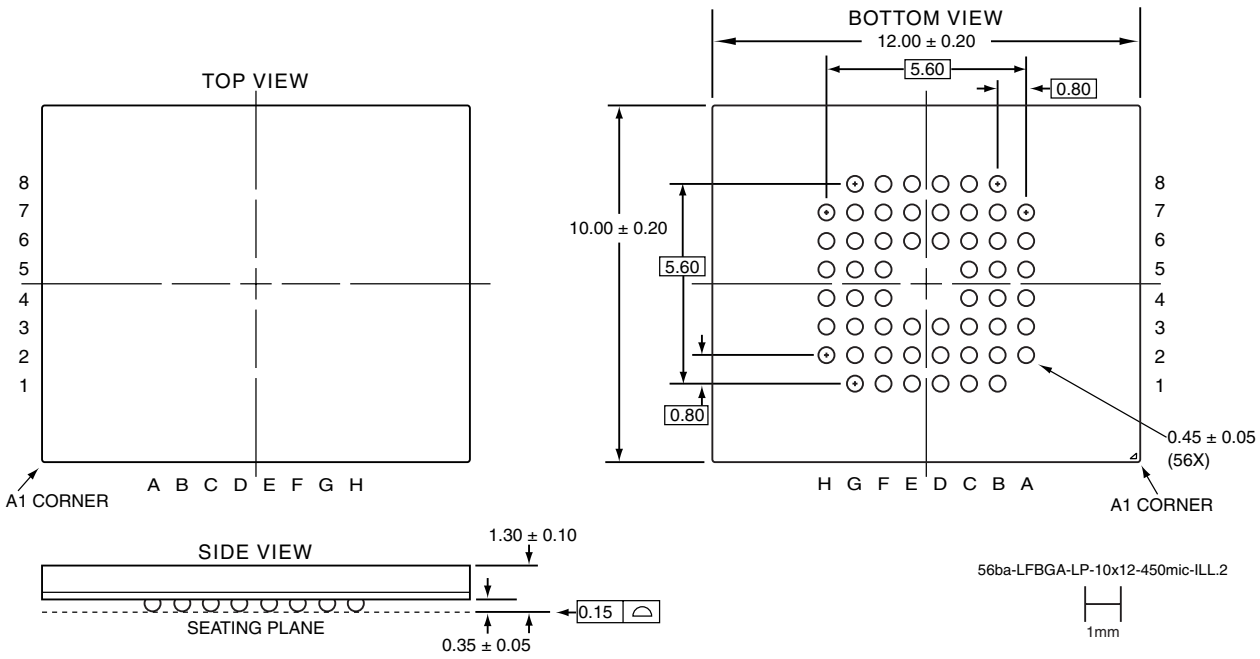
SST34HF3223B-70-4C-LP
SST34HF3223B-90-4C-LP
SST34HF3223B-70-4E-LP
SST34HF3223B-90-4E-LP

Valid combinations for SST34HF3243B

SST34HF3243B-70-4C-LP
SST34HF3243B-90-4C-LP
SST34HF3243B-70-4E-LP
SST34HF3243B-90-4E-LP

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

PACKAGING DIAGRAMS



Note: 1. Although many dimensions are similar to those of JEDEC Publication 95, MO-210, this specific package is not registered.
2. All linear dimensions are in millimeters (min/max).
3. Coplanarity: 0.1 (±.05) mm.
4. The actual shape of the corners may be slightly different than as portrayed in the drawing.

56-BALL LOW-PROFILE, FINE-PITCH BALL GRID ARRAY (LFBGA) 10MM X 12MM (64 POSSIBLE BALL POSITIONS)
SST PACKAGE CODE: LP