



Digitally Programmable 8 to 25 Multiplex LCD Controller & Driver

Description

The EM6124 is a low power CMOS LCD controller and driver. The 8, 16, 20 and 24 way multiplex are digitally programmable by the command byte. One additional line can be added for Icons or Inverted Video by programming 9, 17, 21 or 25 way multiplex. The display refresh is handled on chip by an internal RC oscillator via one selectable 25 x 116 RAM which holds the LCD content driven by the driver. LCD pixels (or segments) are addressed on a one to one basis with the 25 x 116 bit RAM (a set bit corresponds to an activated LCD pixel). The EM6124 has very low dynamic current consumption, typically 70 μ A at $V_{DD} = 2$ V, $V_{LCD} = 7$ V making it particularly attractive for portable and battery powered products. The wide operating range on supply voltages and temperature offers much application flexibility. The LCD voltage, bias generation and frame frequency are generated on chip. The clock signal can be used to shift and to latch the data into the RAM.

Applications

- Mobile phones (GSM, DECT)
- Smart cards
- Automotive displays
- Portable, battery operated products
- Balances and scales, utility meters

Features

- Slim IC for chip-on-board, with gold bumps for Chip-On-Glass and Chip-On-Flex technologies
- Very simple 2-wire interface
- Digitally programmable multiplex rates: 8 x 113, 9 x 112, 16 x 105, 17 x 104, 20 x 101, 21 x 100, 24 x 97, 25 x 96
- No lost pads while row driver from 8 up to 25
- On chip: Voltage multiplier, V_{LCD} up to 7 V (3 to 6 V at 25 °C), 64 V_{LCD} digitally programming steps, 4 V_{LCD} temperature compensation factors, bias generation, V_{ON} / V_{OFF} generation, frame frequency, display refresh RAM
- No busy state
- High noise immunity in inputs
- No external components needed, except a V_{LCD} capacitor
- Digitally reversing row data
- Digitally reversing column data
- Inverting data function
- Blank function
- Set function
- Checker and Inverted Checker functions
- Sleep modes
- Low LCD operating current consumption
- Wide V_{DD} voltage supply range, 2 to 5 V
- Wide temperature range: -40 to + 85 °C
- Direct display of RAM data through the display data RAM

(To cascade ICs, please see Fig. 19 and contact EM Microelectronic-Marín S.A.)

Typical Operating Configuration

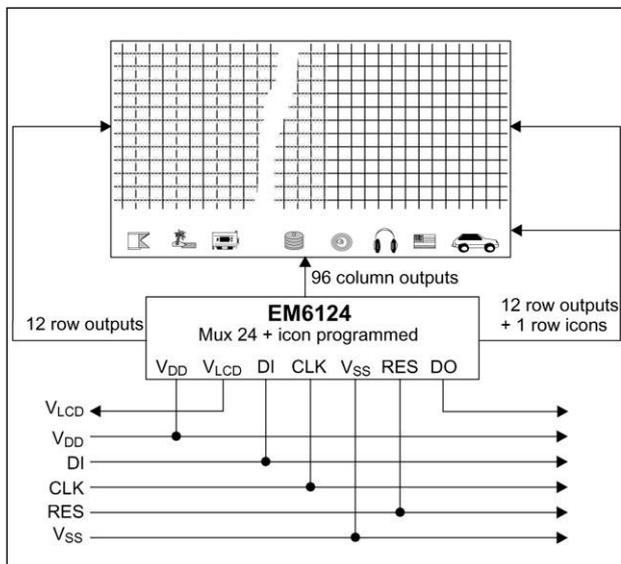


Fig. 1

Pad Assignment

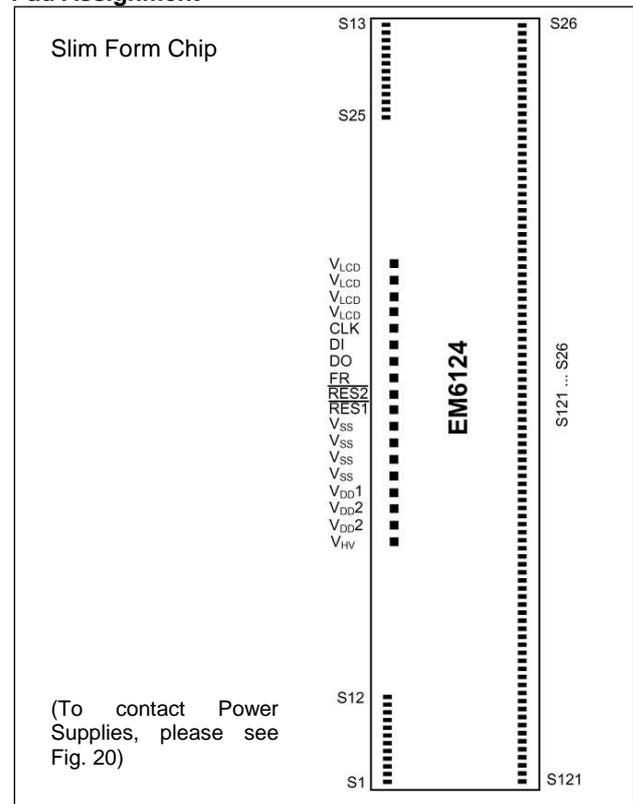


Fig. 2



Absolute Maximum Ratings

Parameter	Symbol	Conditions
Supply voltage range	V _{DD1,2}	-0.3V to 6V
Supply high voltage range	V _{HV}	-0.3V to 6V
Internal generated V _{LCD}	V _{LCD}	7V
Voltage at DI, DO, CLK, FR, RES	V _{LOGIC}	-0.3V to V _{DD} +0.3V
Voltage at S1 to S121	V _{DISP}	-0.3V to V _{LCD} +0.3V
Storage temperature range	T _{STO}	-65 to +150°C
Electrostatic discharge max. to MIL-STD-883C method 3015.7 with ref. to V _{SS}	V _{Smax}	1000V
Maximum soldering conditions	T _{Smax}	250°C x 10s

Stresses above these listed maximum ratings may cause permanent damages to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Electrical Characteristics

V_{DD1} = V_{DD2} = 3V, V_{HV} = 2.5 to 5V and T_A = -40 to +85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Standby supply current	I _{DD}	See note 1		16	22	μA
Standby supply current	I _{HV}	See note 1, V _{LCD} step 30 (hexa)		65	170	μA
Dynamic supply current	I _{DD}	See note 2		57	75	μA
Standby supply current	I _{HV}	See note 3, V _{LCD} Step 00 (hexa)		35	140	μA
Sleep mode supply current	I _{DD}			0.1		μA
Sleep mode supply current	I _{HV}			0.1		μA
Control Signals DI, CLK, FR, RES1, RES2						
Input leakage	I _{IN}	V _{DD1,2} or V _{SS}	-1		1	μA
Input capacitance	C _{IN}	at T _A = 25°C		8		pF
Low level input voltage	V _{IL}		0		0.3 V _{DD1,2}	V
High level input voltage	V _{IH}		0.7 V _{DD1,2}		V _{DD1,2}	V
DC output component	±VDC	See table 4		30	100	mV
V _{LCD} (internally generated)	V _{LCD}	See note 4		6.15		
V _{LCD}	V _{LCD}	See note 5		3.15-7.09		V
	V _{LCD} Step			62.5		mV

Table 3

Note 1: All outputs open, DI and CLK at V_{SS}, mux ratio = 24, checker pattern.

Note 2: All outputs open, DI at V_{SS}, f_{CLK} = 1 MHz, mux ratio = 24, checker pattern.

Note 3: DI and CLK at V_{SS}, checker pattern, mux ratio = 8.

Note 4: Initialization bits 18 to 23 = 110000 and initialization bits 10, 11 = 00; laser trimming on request.

Note 5: Initialization bits 18 to 23 = 000000/111111.

DC Output Component

Output	Frame	Logic Data	Measured*	Guaranteed
Row Driver	n	0L	V _{LCD} - V ₂	V ₁ = 0.83 x V _{LCD} ± 100 mV V ₂ = 0.66 x V _{LCD} ± 100 mV
	n + 1	0L	V ₄ - V _{SS}	
Column Driver	n	0L	V _{LCD} - V ₂	V ₃ = 0.34 x V _{LCD} ± 100 mV V ₄ = 0.17 x V _{LCD} ± 100 mV
	n + 1	0L	V ₃ - V _{SS}	

Table 4

$$*V_x = \frac{V_x(\text{load} = +1\mu\text{A}) + V_x(\text{load} = -1\mu\text{A})}{2}, \text{ mux 24 or 25 programmed, VLCD} = 6\text{V, TA} = 25^\circ\text{C}$$

Test is performed for multiplex rate = 25. All multiplex rate ≠ 25 are guaranteed by design. If multiplex rate ≠ 25, test will be performed on request.

Timing Characteristics

V_{DD1} = V_{DD2} = 2 to 3V, V_{HV} = 2.5 to 5V and T_A = -40 to +85°C

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Clock high pulse width	t_{CH}		70			ns
Clock low pulse width	t_{CL}		110			ns
Clock period	t_{per}		550			ns
Reset1 pulse width	t_{RES1}		10			μ s
Reset2 pulse width	t_{RES2}		130			ns
Clock and FR rise time	t_{CR}				200	ns
Clock and RF fall time	t_{CF}				200	ns
Data input setup time	t_{DS}		20			ns
Data input hold time	t_{DH}		260			ns
FR (internal frame frequency)	f_{FR} (note 1)			75		Hz

Table 5a

Note 1: EM6124 (n), FR = n times the desired LCD refresh rate where n is the EM6124 mux mode number; laser trimming on request
See Fig. 17.01 and 17.02 for more details concerning the frame frequency

$V_{DD1} = V_{DD2} = 3$ to $5V$, $V_{HV} = 2.5$ to $5V$ and $T_A = -40$ to $+85^\circ C$

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Clock high pulse width	t_{CH}		50			ns
Clock low pulse width	t_{CL}		55			ns
Clock period	t_{per}		350			ns
Reset1 pulse width	t_{RES1}		10			μ s
Reset2 pulse width	t_{RES2}		80			ns
Clock and FR rise time	t_{CR}				200	ns
Clock and RF fall time	t_{CF}				200	ns
Data input setup time	t_{DS}		20			ns
Data input hold time	t_{DH}		140			ns
FR (internal frame frequency)	f_{FR} (note 1)			75		Hz

Table 5b

Note 1: EM6124 (n), FR = n times the desired LCD refresh rate where n is the EM6124 mux mode number; laser trimming on request

Timing Waveforms

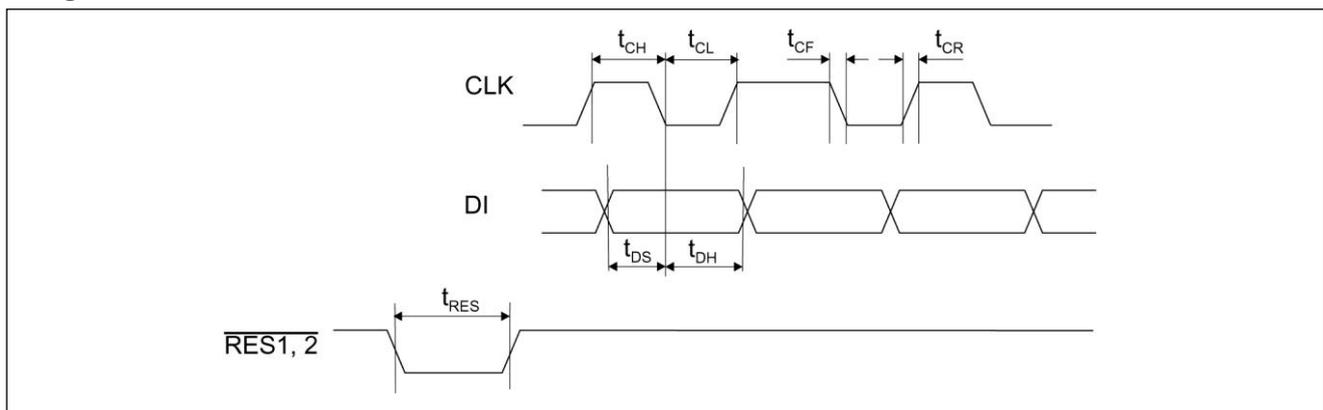


Fig. 3



1 Bit Interface Description

This 1 bit interface is very simple to use. There are three modes to load data into the EM6124.

Command byte only mode

To validate this mode, 8 bits must be shifted with bit 3 to bit 7 set to 1L. This mode is used for blank, set or sleep mode functions.

Command byte and initialization mode

To validate this mode, 32 bits must be shifted with bit 0 and bit 1 set to 1L. Bit 2 (sleep) can be active or inactive. Bit 3 to bit 7 (RAM address) can be in any state but it is important that they are not all simultaneously set to 1L, otherwise the chip will be in command byte only mode.

Command byte and display information mode

To validate this mode, 128 bits must be shifted, eight first bits are for command byte, all the other are RAM data depending of col bit mode and multiplex ratio. There are also x bits don't care in each loading depending on the programming of the chip (see Fig. 4 for more details).

In each RAM's data loading, the command byte has to be introduced for the RAM address. Before loading any data into the RAM the chip has to be initialized.

Command Byte

Command Bits 0 to 7								
0	1	2	3	4	5	6	7	
Blank	Set	Sleep	RAM address					

Table 6

Cmdbit 0: Blank bit forces all column outputs off.

Cmdbit 1: Set bit forces all column output on.

Note: If bit 0 and bit 1 are both to 1L, the chip will be in initialization mode. See remarks below.

Cmdbit 2: Sleep mode bit, stops the voltage booster and the internal oscillator, active bit col forces all outputs to V_{SS}.

Cmdbits 3-7: RAM address bits. See table 6.

If Cmdbits 3-7 are set to 1L, EM6124 is in Cmd byte only mode.

Initialization Bits

Initialization Bits 8 to 15							
8	9	10	11	12	13	14	15
Mux Mode		Temp. Coeff.		Checker	Inv. Checker	Col	Inv.Row
Initialization Bits 16 to 23							
16	17	18	19	20	21	22	23
M/LSB	Video	Step 1	Step 2	Step 3	Step 4	Step 5	Step 6
Initialization Bits 24 to 31							
24	25	26	27	28	29	30	31
Icon	Sleep 2	Test 6	Test 5	Test 4	Test 3	Test 2	Fr_ext

Table 7

Mux ratio (Init. bit 8, 9)		
8	9	mux mode
0	0	8
0	1	16
1	0	20
1	1	24

Table 8

Init.bit 8-9: Mux mode bits. The multiplex ratio is selected by these two bits. Table 8 shows the corresponding values.

Init.bit 10-11: V_{LCD} temperature coefficient is selected by these two bits. Table 11 shows the corresponding values.

Init.bit 12: Checker bit gives the possibility to force all outputs segments in checked form (see Fig. 10 and Fig. 18.14).

Init.bit 13: Inverse Checker bit gives the possibility to force all outputs segments in inverse checked form (see Fig. 10 and Fig. 18.15).

Init.bit 14: Col bit configures the EM6124 on row and column driver or column driver only. In this mode the frame frequency must be external.

Init.bit 15: Row inversion, possibility to inverse the order of the row outputs (see Table 10 and Fig. 18.12).

Init.bit 16: M/LSB, possibility to inverse the order loading for RAM data (see Fig. 4).

Init.bit 17: Video bit, possibility to inverse the content of the RAM. All the 0L pass to 1L and all the 1L pass to 0L (see Fig. 18.11).

Init.bit 18-23: V_{LCD} 64 steps programming bits. See Fig. 8.

Bit 18 (step 1) for MSB and bit 23 (step 6) for LSB.

Init.bit 24: Icon bit adds one line more to the selected mux mode ratio for icon segments outputs.

Init.bit 25: Sleep 2. Set all outputs at V_{SS}.

Init.bit 26-30: Must be set to 0L.

Init.bit 31: Fr_ext give the possibility to supply frame to EM6124 externally. If Fr_ext=1L then FR is input pin and user must supply signal frame. If Fr_ext=0L then FR is output pin, the signal frame is internally generated. (**Init.bit 14:** has the priority)

Reset 1

Power-up: Must be followed by a RESET cycle. After the reset 1 pulse the LCD controller driver is set to the following status:

- All outputs at V_{SS}
- Blank & Set (cmdbits 0,1) = 0L
- Sleep mode (cmdbit 2) = 0L
- RAM address (cmdbits 3 to 7) = 0L
- Multiplex ratio (init.bits 8, 9) = 0L
- Temperature coefficient (init.bits 10,11) = 0L
- Checker & Inv.Checker (init.bits 12, 13) = 0L
- Col Mode (init.bit 14) = 1L
- Inv. Row (init.bit 15) = 0L
- M/LSB (init.bit 16) = 1L
- Video (init.bit 17) = 1L
- V_{LCD} step (init.bits 18 to 23) = 0L
- Icon (init.bit 24) = 0L
- Sleep 2 (init.bit 25) = 1L
- The content of the RAM remains unchanged
- Frame internally generated (init.bit 31) = 0L

An initialization should take place after reset (32 bits sent).

Pin Assignment

Name	Function
S1..S121	LCD outputs, see Fig.4
FR	AC I/O signal for LCD driver output
DI	Serial data input
DO	Serial data output
CLK	Data clock input
RES1	General reset
RES2	Reset the serial interface counter
V _{LCD}	Internal generated voltage output
V _{DD1}	Power supply for logic
V _{DD2}	Power supply for analogic
V _{HV}	Power supply for high voltage
V _{SS}	Supply GND

Table 9

Data Transfer Cycle

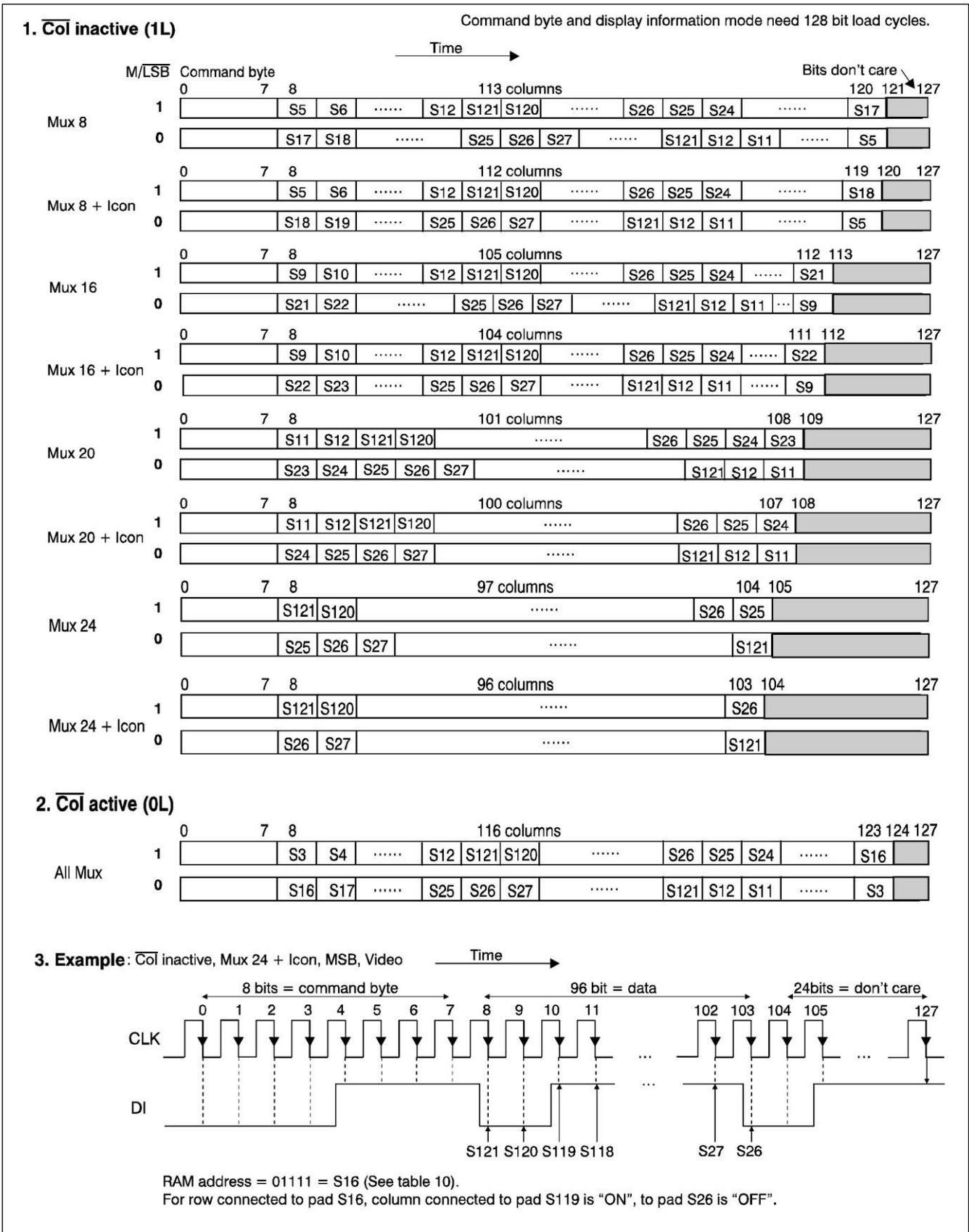


Fig. 4

Output Row Assignments

Row	RAM Address					Mux Mode															
						Mu 8		Mux 8 + Icon		Mux 16		Mux 16 + Icon		Mux 20		Mux 20 + Icon		Mux 24		Mux 24 + Icon	
	Inv. Row		Inv. Row		Inv. Row		Inv. Row		Inv. Row		Inv. Row		Inv. Row		Inv. Row						
	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
1	0	0	0	0	0	S1	S16	S1	S17	S1	S20	S1	S21	S1	S22	S1	S23	S1	S24	S1	S25
2	0	0	0	0	1	S2	S15	S2	S16	S2	S19	S2	S20	S2	S21	S2	S22	S2	S23	S2	S24
3	0	0	0	1	0	S3	S14	S3	S15	S3	S18	S3	S19	S3	S20	S3	S21	S3	S22	S3	S23
4	0	0	0	1	1	S4	S13	S4	S14	S4	S17	S4	S18	S4	S19	S4	S20	S4	S21	S4	S22
5	0	0	1	0	0	S13	S4	S13	S13	S5	S16	S5	S17	S5	S18	S5	S19	S5	S20	S5	S21
6	0	0	1	0	1	S14	S3	S14	S4	S6	S15	S6	S16	S6	S17	S6	S18	S6	S19	S6	S20
7	0	0	1	1	0	S15	S2	S15	S3	S7	S14	S7	S15	S7	S16	S7	S17	S7	S18	S7	S19
8	0	0	1	1	1	S16	S1	S16	S2	S8	S13	S8	S14	S8	S15	S8	S16	S8	S17	S8	S18
9	0	1	0	0	0			S17	S1	S13	S8	S13	S13	S9	S14	S9	S15	S9	S16	S9	S17
10	0	1	0	0	1					S14	S7	S14	S8	S10	S13	S10	S14	S10	S15	S10	S16
11	0	1	0	1	0					S15	S6	S15	S7	S13	S10	S13	S13	S11	S14	S11	S15
12	0	1	0	1	1					S16	S5	S16	S6	S14	S9	S14	S10	S12	S13	S12	S14
13	0	1	1	0	0					S17	S4	S17	S5	S15	S8	S15	S9	S13	S12	S13	S13
14	0	1	1	0	1					S18	S3	S18	S4	S16	S7	S16	S8	S14	S11	S14	S12
15	0	1	1	1	0					S19	S2	S19	S3	S17	S6	S17	S7	S15	S10	S15	S11
16	0	1	1	1	1					S20	S1	S20	S2	S18	S5	S18	S6	S16	S9	S16	S10
17	1	0	0	0	0							S21	S1	S19	S4	S19	S5	S17	S8	S17	S9
18	1	0	0	0	1									S20	S3	S20	S4	S18	S7	S18	S8
19	1	0	0	1	0									S21	S2	S21	S3	S19	S6	S19	S7
20	1	0	0	1	1									S22	S1	S22	S2	S20	S5	S20	S6
21	1	0	1	0	0											S23	S1	S21	S4	S21	S5
22	1	0	1	0	1													S22	S3	S22	S4
23	1	0	1	1	0													S23	S2	S23	S3
24	1	0	1	1	1													S24	S1	S24	S2
25	1	1	0	0	0															S25	S1

Table 10

Command Byte Only Mode

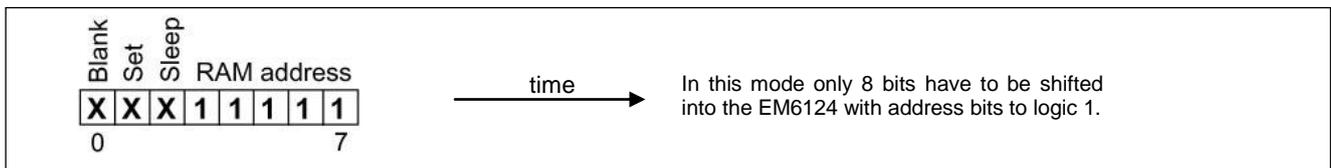


Fig. 5

Command Byte and Initialization Mode

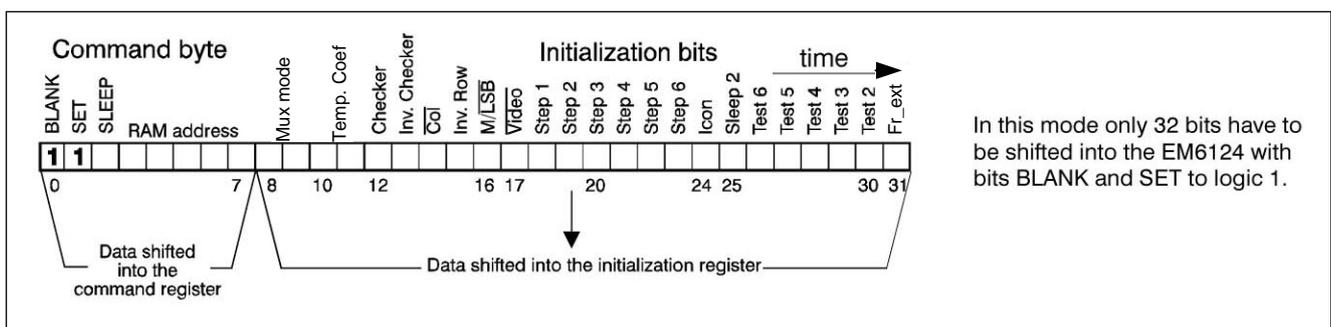


Fig. 6

Command Byte and Display Information Mode

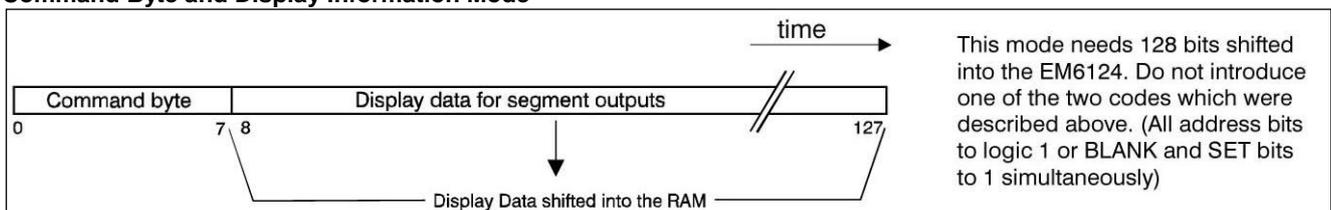


Fig. 7

Typical V_{LCD} Programming

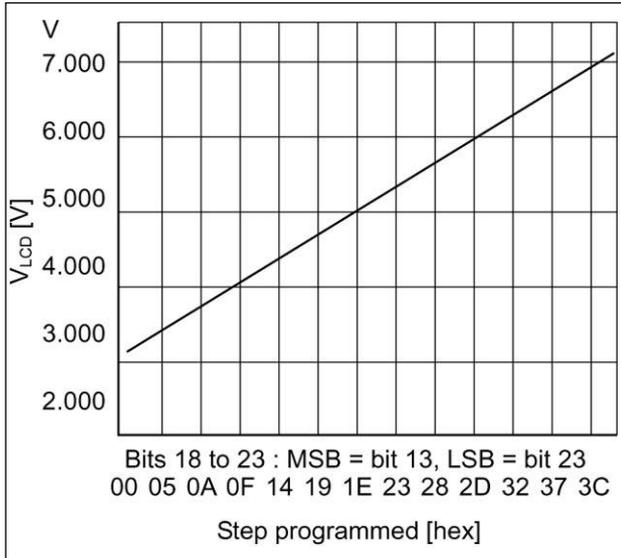


Fig. 8

Temperature Control

Due to the temperature dependency of liquid crystals viscosity the LCD controlling voltage V_{LCD} must be increased for lower temperatures to maintain optimal contrast. The EM6124 is available with 4 different temperature coefficients (see Fig. 9). The coefficient is selected by 2 bits in the initialization code TC bits 10 and 11. Table 11 shows the typical values of the different temperature coefficients. They are proportional to the programmed V_{LCD} .

Typical Values of the Temperature Coefficients

Bit 10, Bit 11	Value	Unit
0 0	$-0.2 \times V_{LCD}$	mV/°C
0 1	$-0.52 \times V_{LCD}$	mV/°C
1 0	$-1.16 \times V_{LCD}$	mV/°C
1 1	$-1.82 \times V_{LCD}$	mV/°C

Table 11

Temperature Coefficients

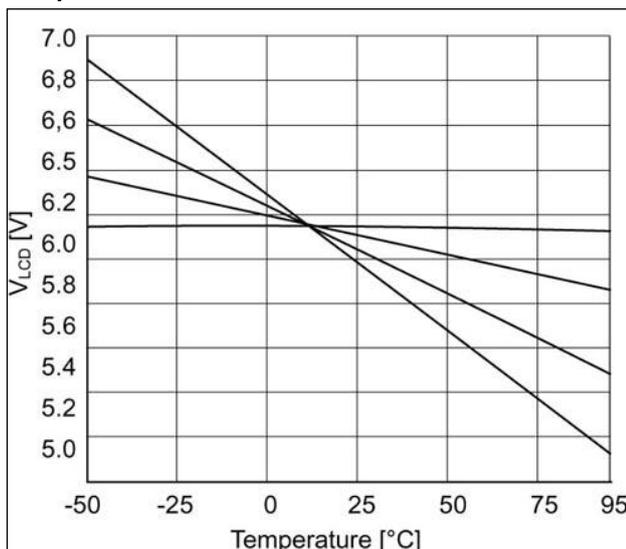


Fig. 9

Checker and Checker Inverse

A fast check display can be easily created setting initialization bits 12 and 13 (called “Checker” and “Inv. Checker”). The display is completely checked with only 2 initialization sequences, one “Checker” and one “Inv. Checker”. For Checker, the pattern fills the display with alternately ON and OFF pixels as shown in Fig. 10. For Inv. Checker, everything is inverted (see Fig.18.14 and 18.15).

Pattern of Checker Mode

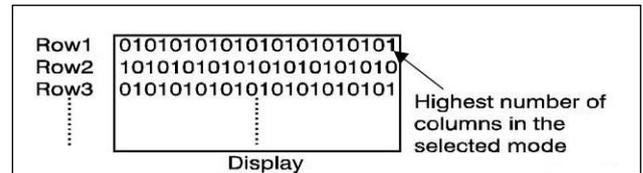


Fig. 10

Internally Generated V_{LCD} versus Temperature

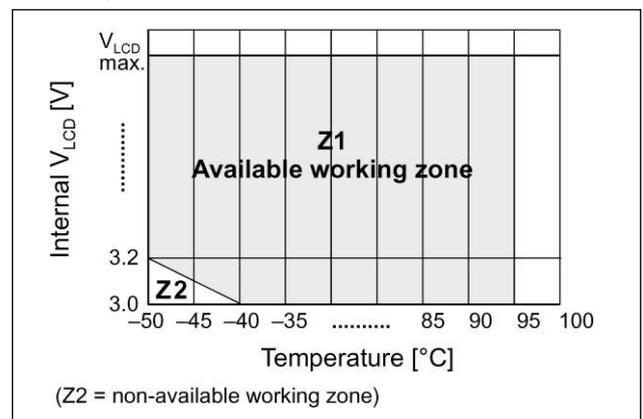


Fig. 11



Display Functions

Bit	State	
	Logic 0	Logic 1
8 - 9: Mux Mode	See table 8	
10 - 11: Temp.Coeff.	See table 11	
12: Checker	Inactive	Chess display
13: Inv. Checker	Inactive	Inverse chess display
14: Col	Column driver only	Row and column driver
15: Inv. Row	Increment rows (example for mux 24: row 1, 2, 3, ..., 24, 1, 2, ...)	Decrement rows (example for mux 24: row 24, 23, 22, ..., 2, 1, 24, 23, ...)
16: M/LSB	Loading in LSB mode	Loading in MSB mode
17: Video	Inverse content of RAM	Inactive
18 - 23: V _{LCD} step	See Fig. 8	
24: Icon	Inactive	Add one line more to selected mux mode
25: Sleep	Inactive	All outputs at V _{ss}
26 - 30:	Must be at 0L	
31: Fr_ext	Frame internally generated	External frame to be supplied

Table 12

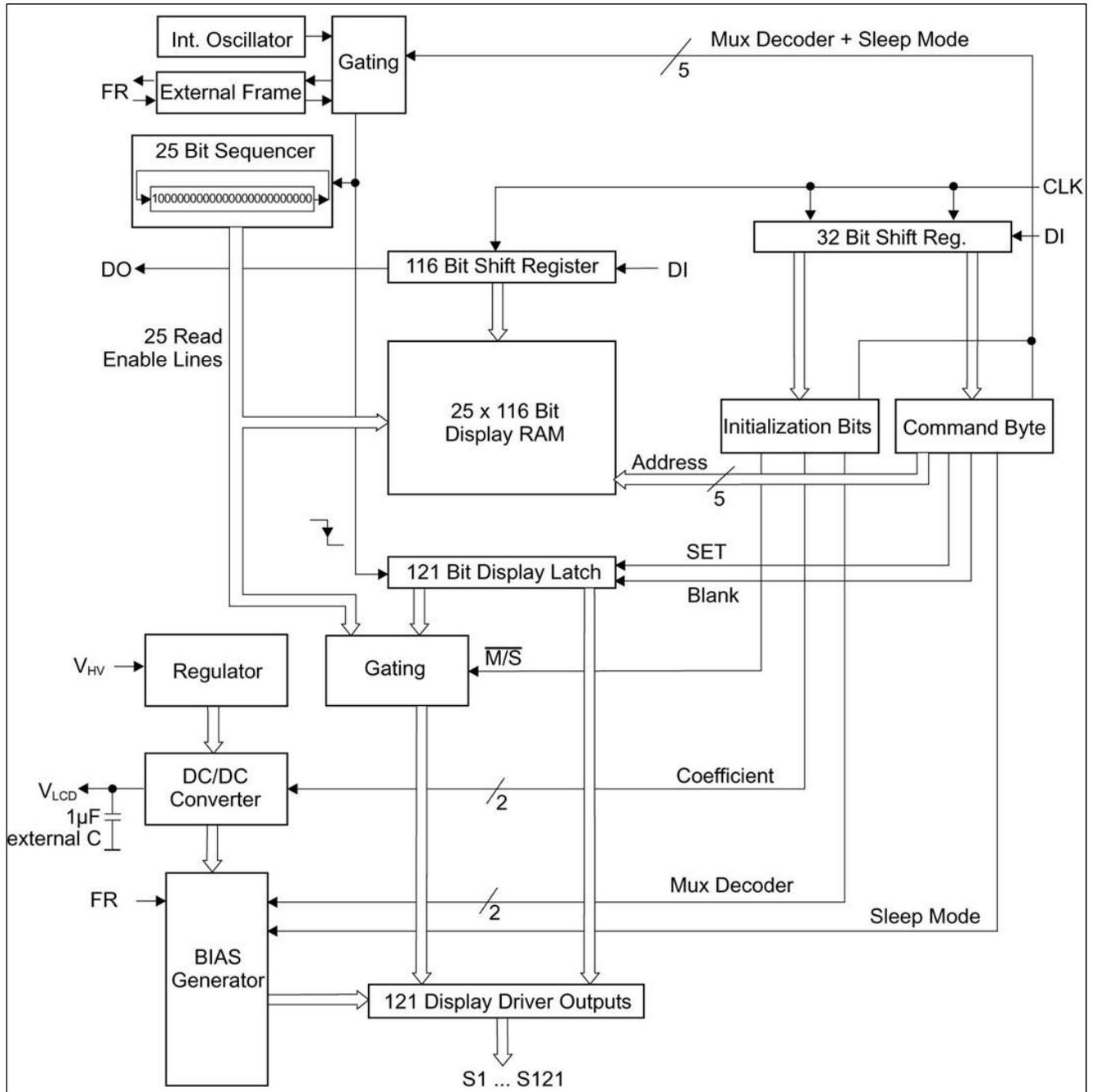
Block Diagram


Fig. 12



LCD Voltage Bias Levels

LCD Drive Type	LCD Bias Configuration	$\frac{V_{OP}}{V_{OFF}(rms)}$	$\frac{V_{ON}(rms)}{V_{OFF}(rms)}$
EM6124 (24) n=24 1:24 MUX	6 Levels	$\sqrt{\frac{\sqrt{n}(\sqrt{n}+1)^2}{2(\sqrt{n}-1)}} = 4.68$	$\sqrt{\frac{\sqrt{n}+1}{\sqrt{n}-1}} = 1.230$
EM6124 (20) n=20 1:20 MUX	6 Levels	$\sqrt{\frac{\sqrt{n}(\sqrt{n}+1)^2}{2(\sqrt{n}-1)}} = 4.39$	$\sqrt{\frac{\sqrt{n}+1}{\sqrt{n}-1}} = 1.255$
EM6124 (16) n=16 1:16 MUX	1/5 Bias 6 Levels	$\sqrt{\frac{\sqrt{n}(\sqrt{n}+1)^2}{2(\sqrt{n}-1)}} = 4.08$	$\sqrt{\frac{\sqrt{n}+1}{\sqrt{n}-1}} = 1.291$
EM6124 (8) n=8 1:8 MUX	1/4 Bias 6 Levels	$\frac{4}{\sqrt{1+\frac{3}{n}}} = 3.4$	$\sqrt{\frac{n-15}{n+3}} = 1.446$

Table 13

Optimum LCD Bias Voltages

Multiplex Rate	V _{LCD}	V1	V2	V3	V4	V _{SS}
1:24	1	0.930	0.660	0.340	0.170	0
1:20	1	0.817	0.634	0.366	0.183	0
1:16	1	0.800	0.600	0.400	0.200	0
1:8	1	0.750	0.500	0.250	-	0'

V_{LCD} > V1 > V2 > V3 > V4 > V_{SS}

The values in the above table are given in reference to V_{LCD} eg. 0.5 means 0.5 x V_{LCD}

Table 14

Row and Column Multiplexing Waveform EM6124 (8)

$$V_{CP} = V_{LCD} - V_{SS}, V_{STATE} = V_{COL} - V_{ROW}$$

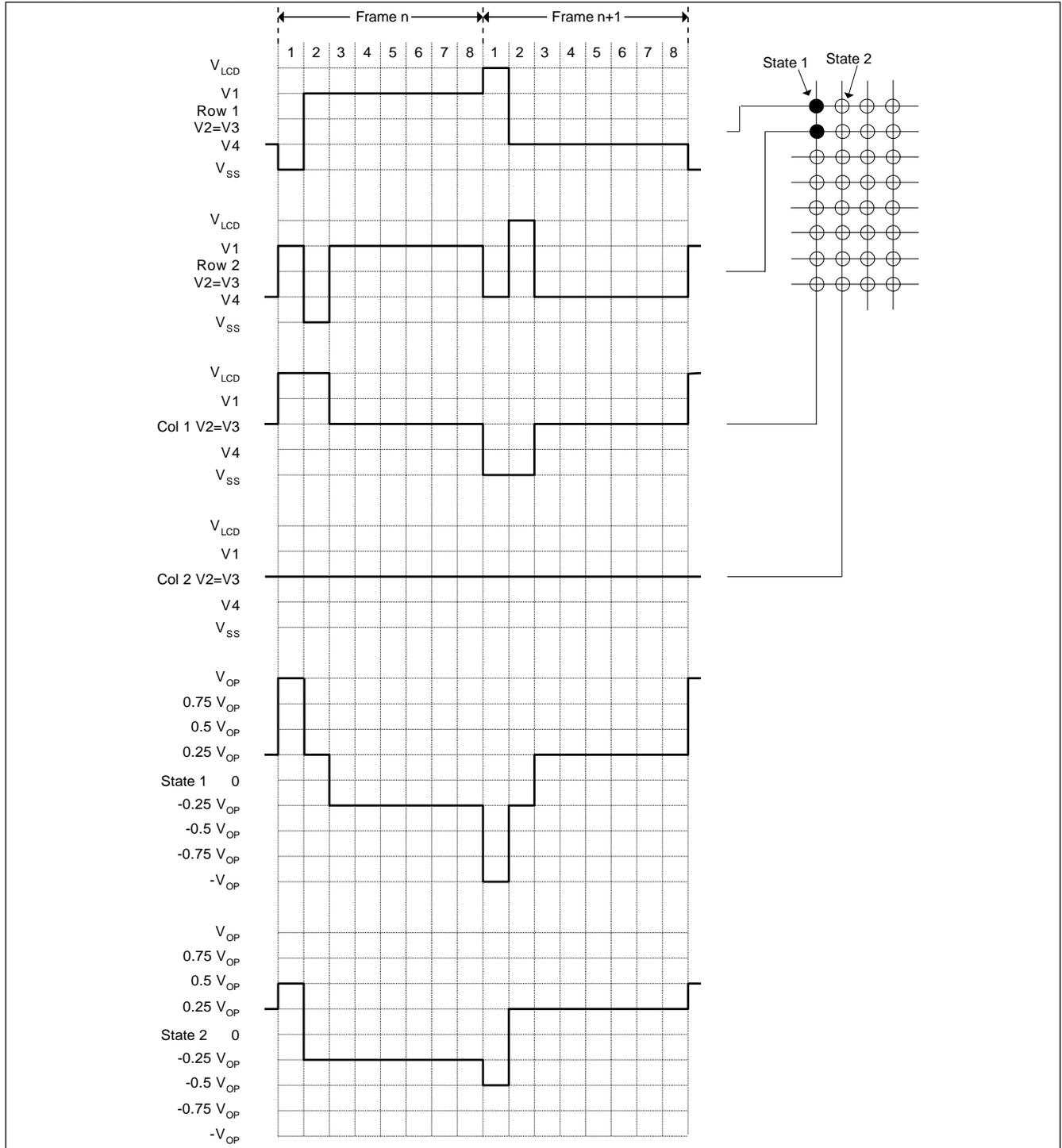


Fig. 13

Row and Column Multiplexing Waveform EM6124 (16)

$$V_{CP} = V_{LCD} - V_{SS}, V_{STATE} = V_{COL} - V_{ROW}$$

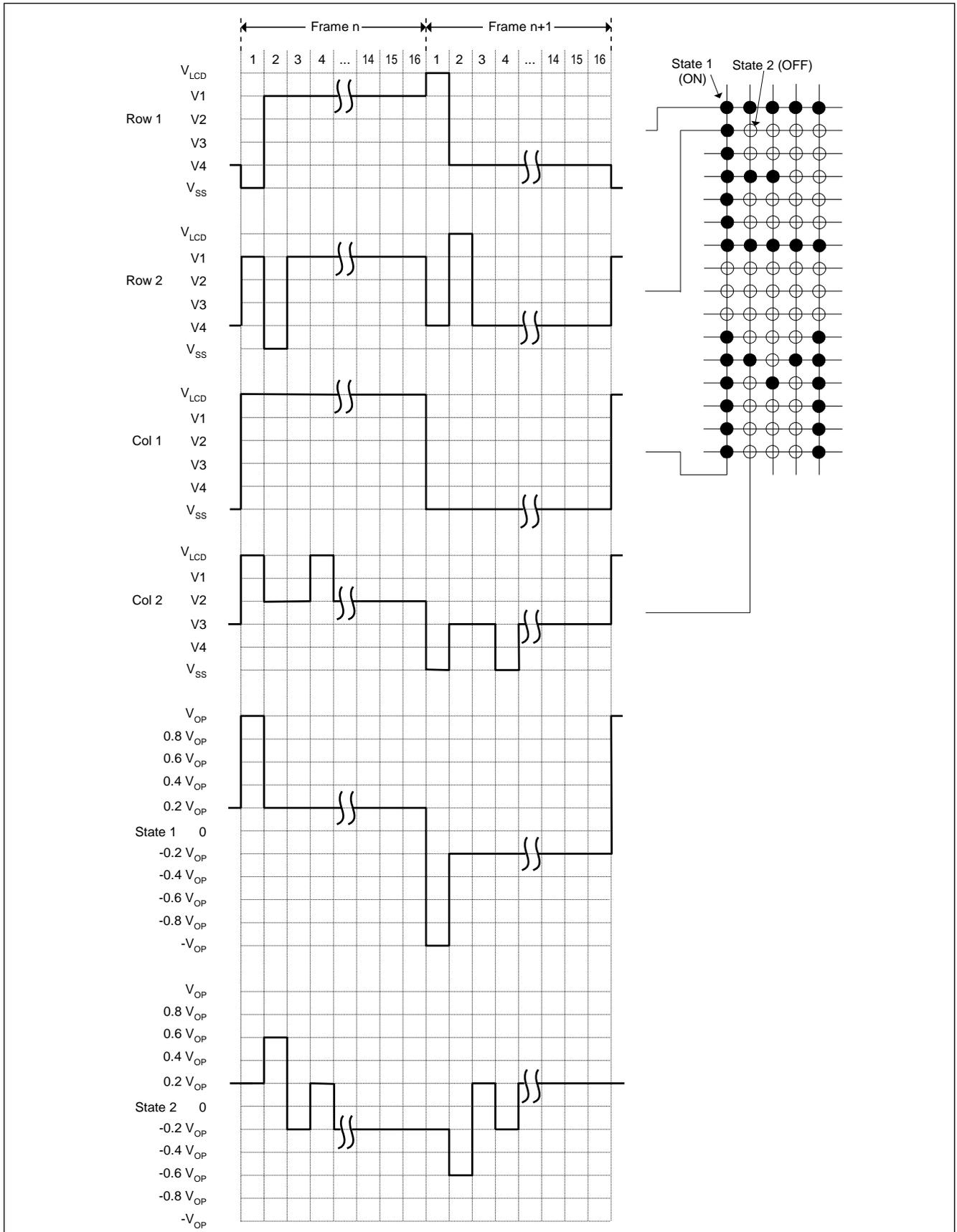


Fig. 14

Row and Column Multiplexing Waveform EM6124 (20)

$$V_{CP} = V_{LCD} - V_{SS}, V_{STATE} = V_{COL} - V_{ROW}$$

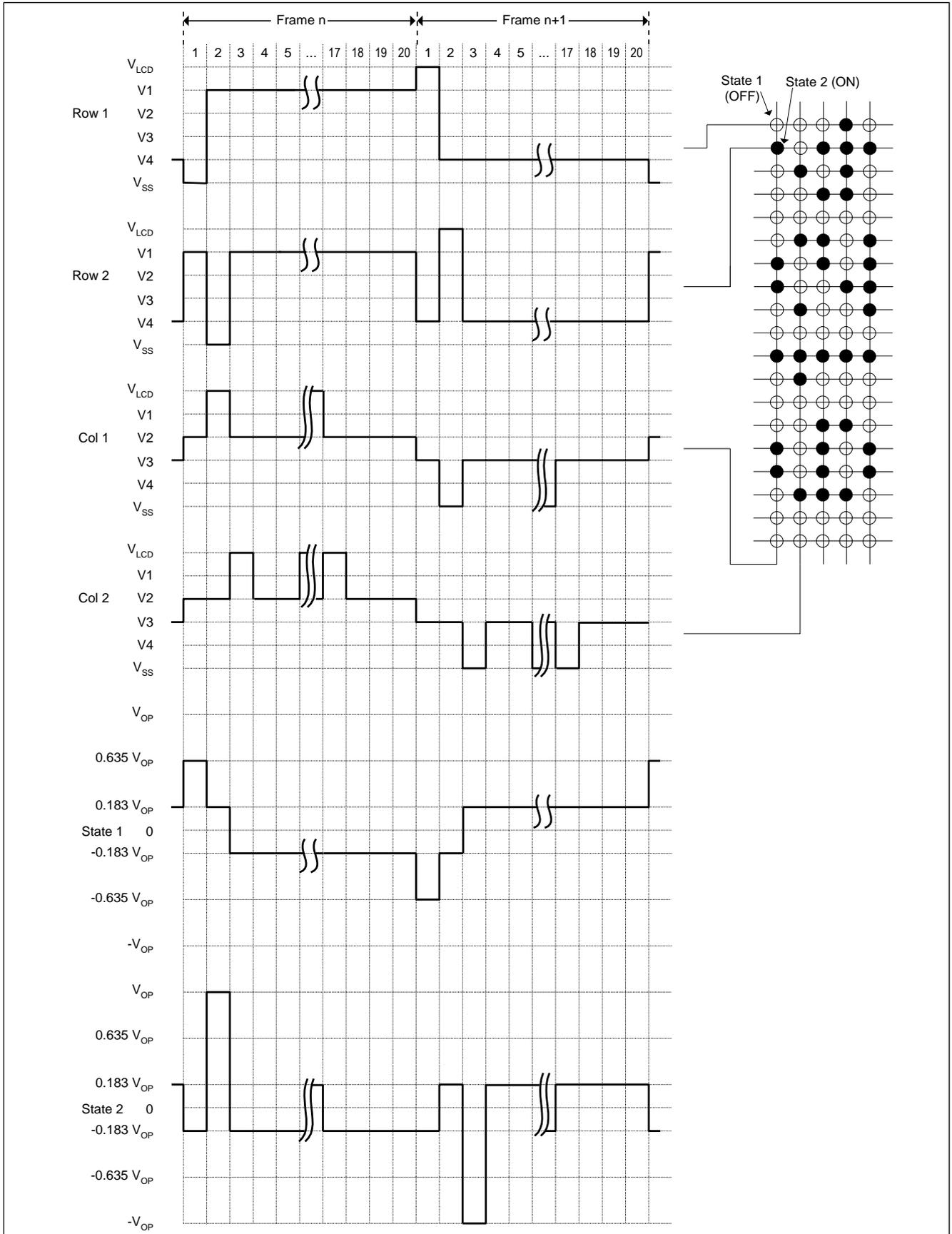


Fig. 15

Row and Column Multiplexing Waveform EM6124 (24)

$$V_{CP} = V_{LCD} - V_{SS}, V_{STATE} = V_{COL} - V_{ROW}$$

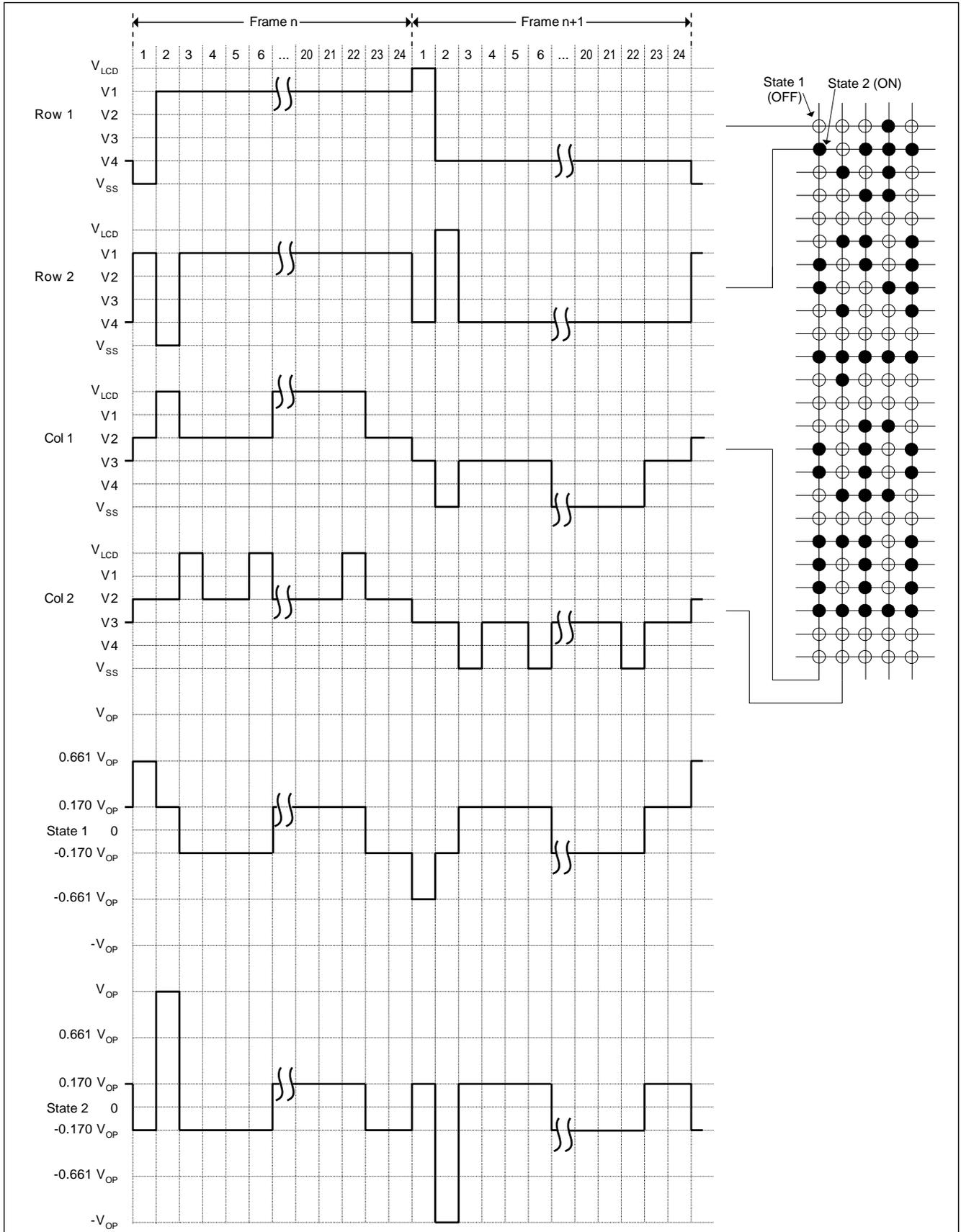


Fig. 16

Functional Description
Supply Voltage V_{DD1} , V_{DD2} , V_{HV} , V_{LCD} , V_{SS}

The voltage between V_{DD1} and V_{SS} is the supply voltage for the logic and the interface. The voltage between V_{DD2} and V_{SS} is the supply voltage for the analogic. V_{DD1} and V_{DD2} must be the same voltage and, in order to guarantee the best functioning, V_{DD1} and V_{DD2} have to be separately connected to the PCB (see Fig. 19). The voltage V_{LCD} is internally generated for the supply voltage of the LCD and is used for the generation of the internal LCD bias level. An external capacitor of 1 μ F must be connected between V_{LCD} and V_{SS} . Table 15 shows the relationship between V_1 , V_2 , V_3 , V_4 for a programmed multiplex rate. Note that $V_{LCD} > V_1 > V_2 > V_3 > V_{SS}$ for the EM6124 8 mux programmed, and for the EM6124 16, 20, 24 mux programmed $V_{LCD} > V_1 > V_2 > V_3 > V_4 > V_{SS}$. The voltage between V_{HV} and V_{SS} is the supply voltage for high voltage part of the EM6124. An external V_{LCD} may also be used by connecting a power supply and programming a lower V_{LCD} voltage during initialization.

Data Input

The data input pin, DI, is used to load serial data into the EM6124. The normal serial data word length is 128 bits. 32 and 8 bits are also available in a special mode (see 1 Bit Interface Description). The command byte is loaded first and then the segment data bits (see Fig. 4).

RES1 Input

Reset is accomplished by applying an external RES1 pulse (active low). When reset occurs within the specified time, all internal register are reset however the content of the RAM is still unchanged. The state after reset is described on page 4.

RES2 Input

Reset is accomplished by applying an external RES2 pulse (active low). When reset occurs within the specified time, the internal counter for serial interface is reset. The counter of the serial interface for data inputs is ready for a new loading of data. This reset 2 does not change the content of the RAM neither the content of the command and the initialization bits. To avoid trouble in case of software interrupt of the MPU during data loading, this function can be used.

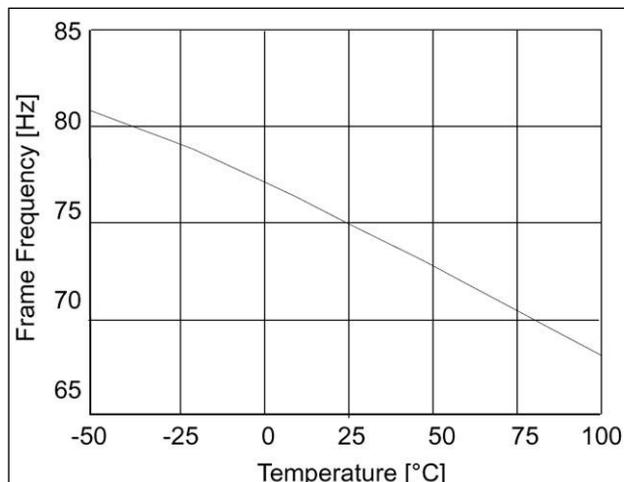
Typical Frame Frequency at $V_{DD} = 3V$


Fig. 17.01

Power-Up

On power up the data in the shift registers, the display RAM, the sequencer driving the 8/16/20/24 rows and the 121 bit display latches are undefined.

CLK Input

The clock input is used to clock the DI serial data into the EM6124.

FR Input / Output

The frame frequency is realized by an internal oscillator with a typical value of 75 Hz. The internal row frequency changes with the number of rows ($F_{row} = 75 \times n$, where $n = 8, 16, 20, 24$). When bit 14 (\overline{Col}) is inactive (active low), the frame frequency is given by the internal oscillator. This frequency can be measured on the I/O FR. When bit 14 (\overline{Col}) is active (active low) or bit 31 (Fr_{ext}) is active (active high), the frame frequency is external then the frequency is given directly by the FR input to the row and column driver (see Fig. 16 and 17 for more details concerning the frame frequency).

\overline{Col}	Fr_{ext}	Pad Frame
0	0	input - ext frame
0	1	input - ext frame
1	0	output - int frame
1	1	input - ext frame

Driver Outputs S1 to S116

There are 121 LCD driver outputs on the EM6124. The output assignments depend on the chosen mux mode ratio (init. bits 8, 9) and the Col function (init. bit 14).

When init. bit 14 (\overline{Col}) is active, all 116 outputs function as column drivers. Table "Output Row Assignments" and Fig. 4 describe exactly the correspondent data to the output of the chip. There is one to one relationship between the display RAM and the LCD driver outputs. Each pixel (segment) driven by the EM6124 on the LCD has a display RAM bit which corresponds to it. Setting the bit turns the pixel "on" and Clearing it turns "off".

For chip-on-glass better performances can be obtained by covering the backside of the chip.

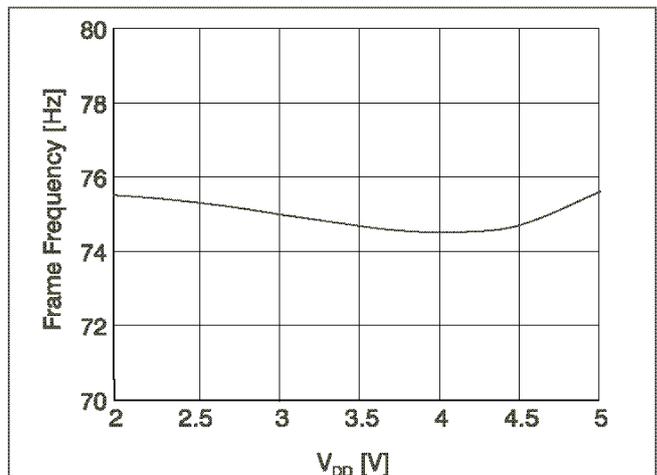
Typical Frame Frequency at $T_A = 25^\circ C$


Fig. 17.02

Functional Description for Versions

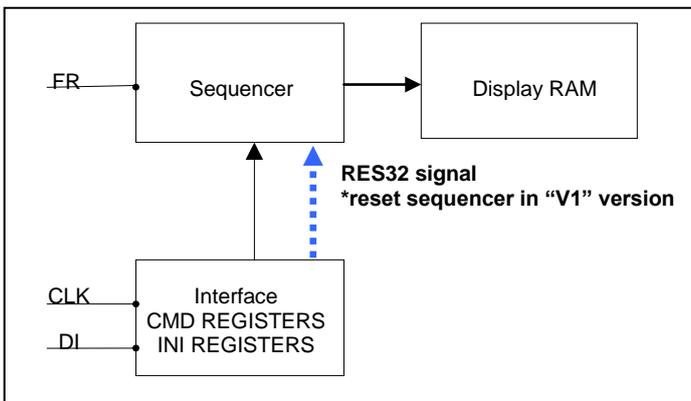
EM6124 is available in two different versions “V1” and “V2”:

- **EM6124V1**
- **EM6124V2**

The difference is the effect of 32 bits initialization procedure. Basically the sequencer block (see block diagram page 9) is used for refresh the rows of the display RAM block, depending of the version (“V1” or “V2”) the sequencer block could be reset or not by the 32 bits initialization procedure.

Functional description EM6124V1

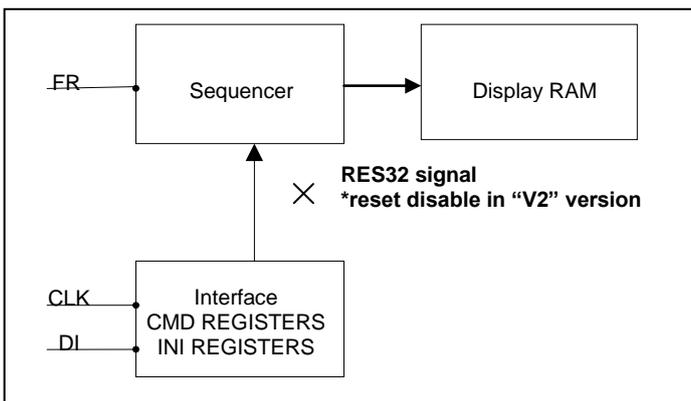
The block sequencer is reset when 32 bits initialization is sent to EM6124V1. Internal signal named “RES32” reset the sequencer, the row1 will be selected during next frame period.



Internal “RES32” signal is used to synchronise the sequencer in cascaded applications.

Functional description EM6124V2

Disable “RES32” in the sequencer block



Internal “RES32” signal is disabled, this version is not recommended for cascaded applications.

Application Example

These tables/figures show how to use the EM6124 with a given initialization. Rows "Data" show the logical value to affect pad DI for each falling edge of pad CLK. A reset cycle pad RES1 at OL is required before sending data.

Command byte								Initialization bits or display data																								
Bit No	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Data	1	1	0	0	0	0	0	0	1	1	0	1	0	0	1	0	0	1	1	1	0	0	0	0	1	0	0	0	0	0	0	0
Description	Bits 0,1 = 1,1: initialization is programmed Bit 2 = 0: no sleep mode Bits 3 to 7: don't care in this case (not 11111)								Bits 8,9,24 = 1,1,1: mux mode 24 + icon; 25 rows driven Bits 10,11 = 0,1: temperature coefficient = $-(0.52 \cdot V_{LCD})$ mV/°C Bits 12,13 = 0,0: no checker or inv. checker functions Bit 14 = 1: row and column driver configuration Bit 15 = 0: row 1 of the RAM displayed on S1, row 2 on S2, ... and row 25 on S25 Bit 16 = 0: first data sent displayed on S26, last one on S121 Bit 17 = 1: 1L in the RAM corresponds to a pixel "ON" Bit 18 to 23 = 1,1,0,0,0,0 : programmed $V_{LCD} = 3.15 + (1 \cdot 32 + 1 \cdot 16 + 0 \cdot 8 + 0 \cdot 4 + 0 \cdot 2 + 0 \cdot 1) \cdot 0.0625 = 6.150V$ Bit 25 = 0: no sleep Bit 26 to 31 = 0,0,0,0,0,0: every test bit must be set to 0																							
	Result																															

Fig. 18.01

Bit No	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	--	125	126	127		
Data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	--	0	0	0		
Description	Bits 0,1,2 = 0,0,0: no set, no blank, no sleep Bits 3 to 7 = 0,0,0,0,0: data sent to row 1 of the RAM								Bits 8 to 103 = 0,0,...,0: first row of the RAM is loaded with 0,0,...,0 Bits 104 to 127 = don't care																							
	Result																															

Fig. 18.02

Table 15
(continued on next pages)

Application Example continued

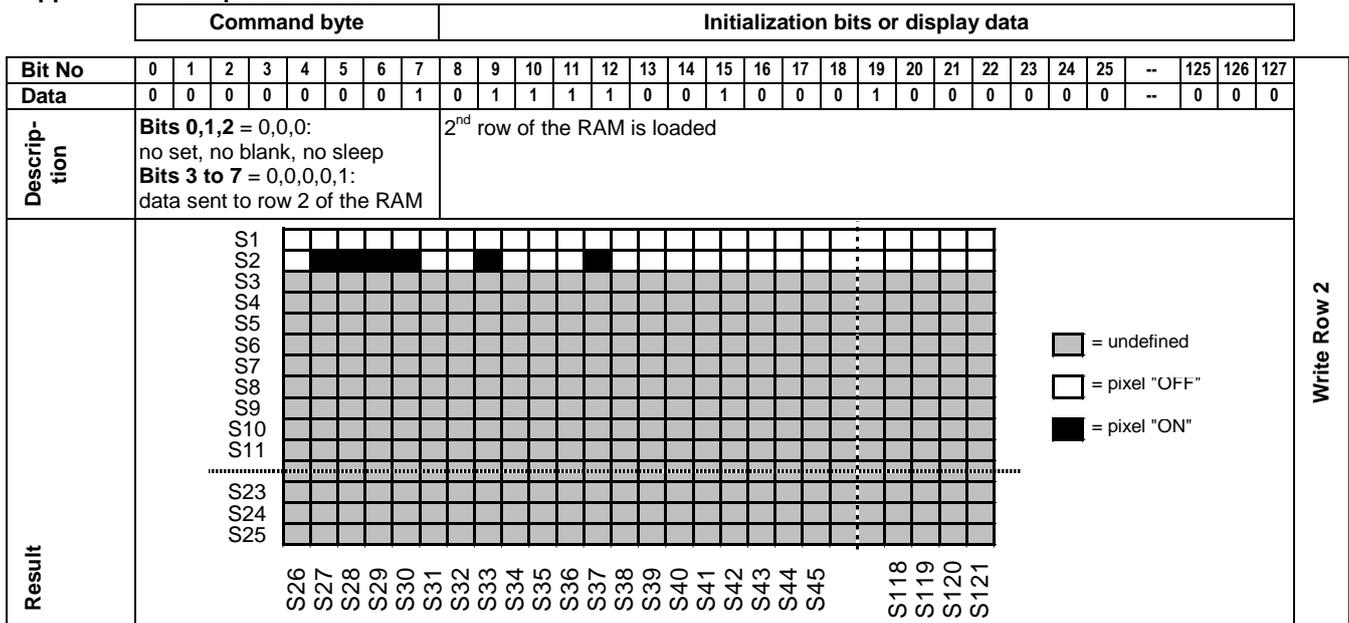


Fig. 18.03

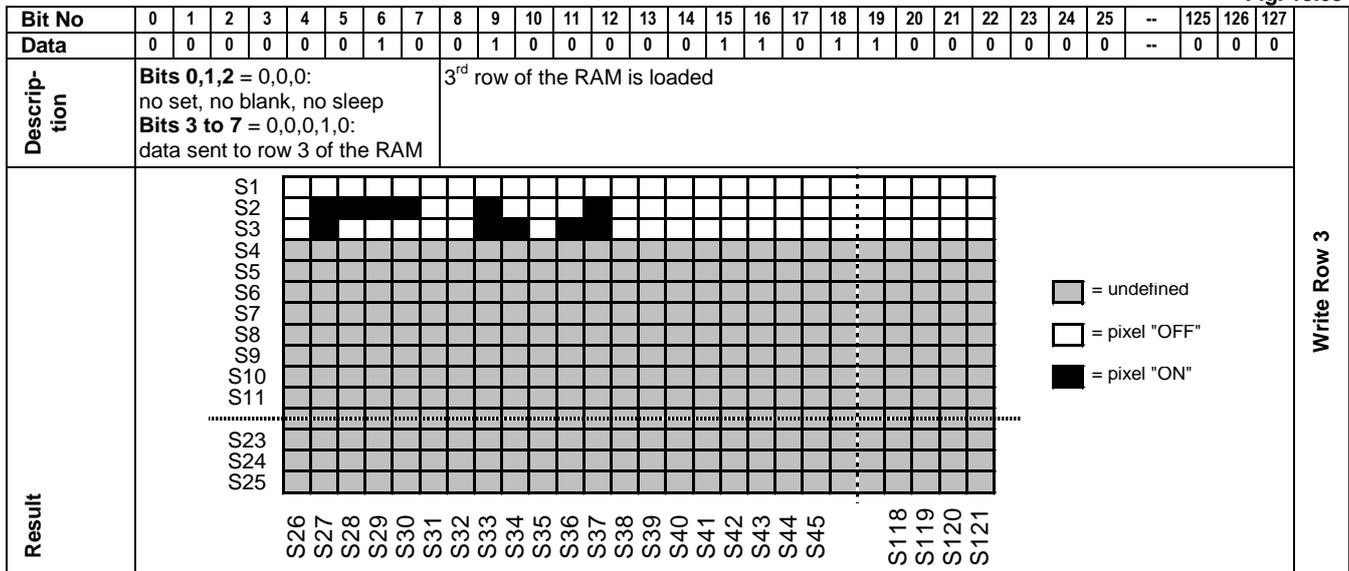


Fig. 18.04

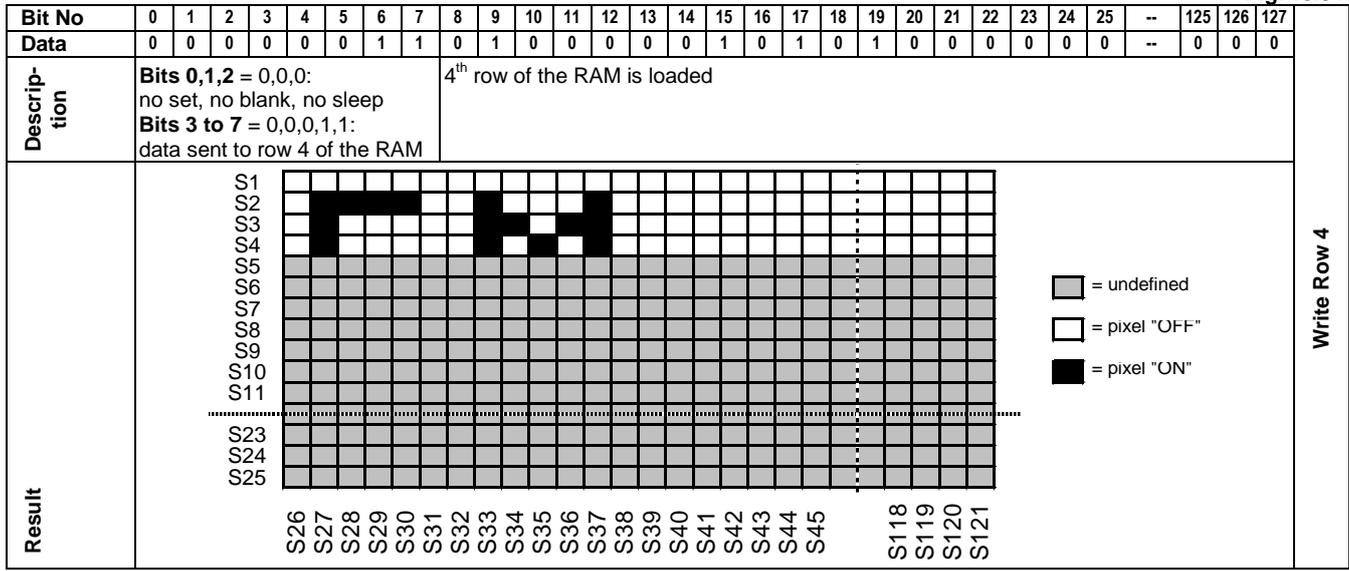


Fig. 18.05

		Command byte							Initialization bits or display data																		
--	--	--------------	--	--	--	--	--	--	-------------------------------------	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--

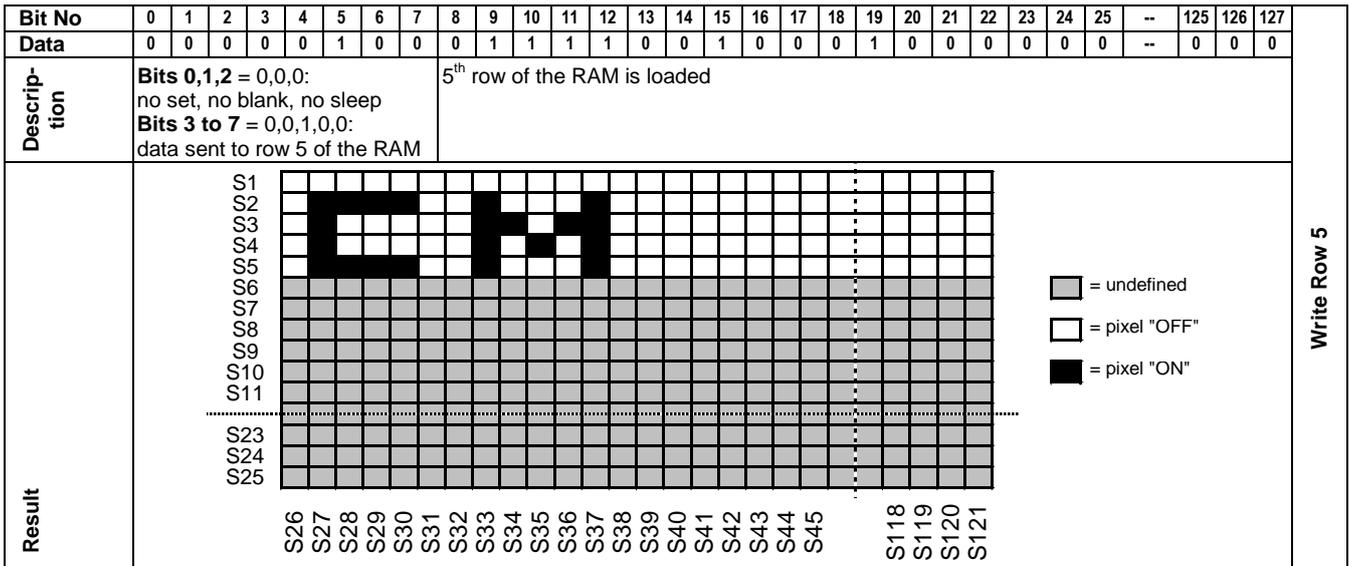


Fig. 18.06

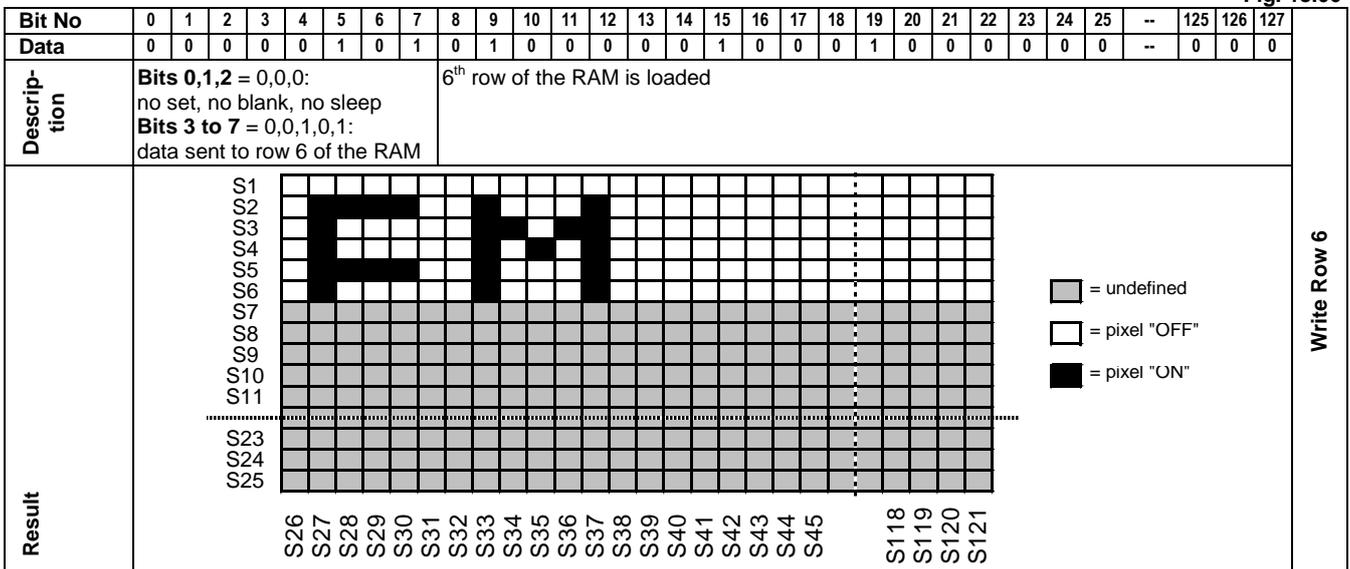


Fig. 18.07

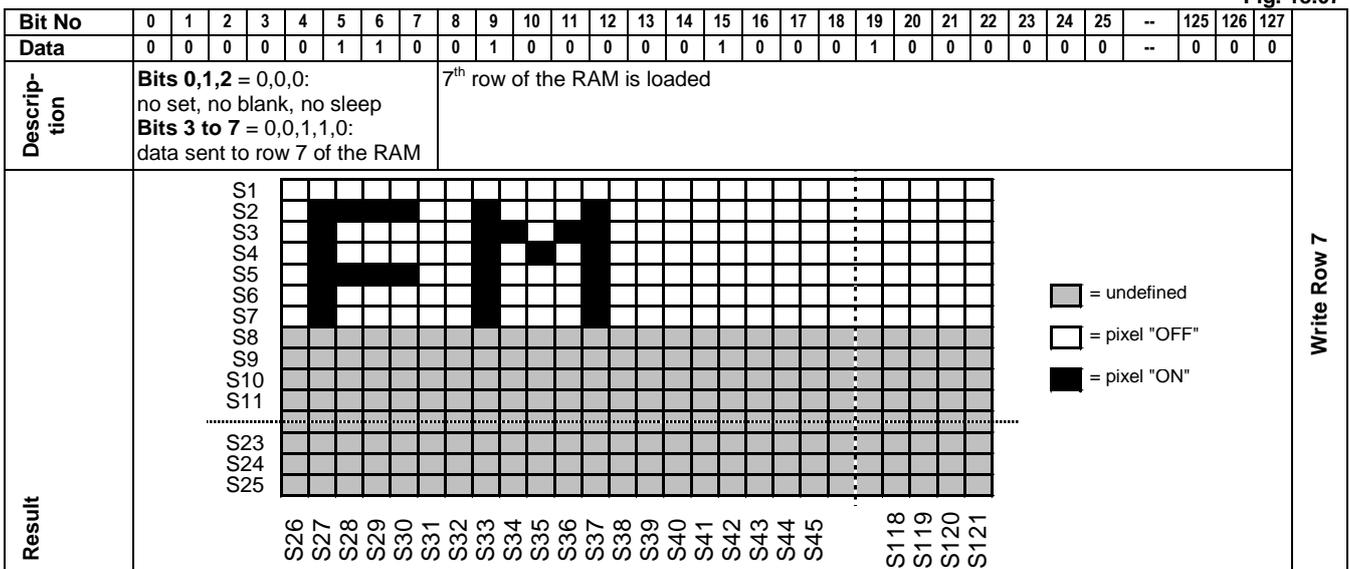


Fig. 18.08

Command byte	Initialization bits or display data
--------------	-------------------------------------

Bit No	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	--	125	126	127
Data	0	0	0	0	0	1	1	1	0	1	1	1	1	0	0	1	0	0	0	1	0	0	0	0	0	0	--	0	0	0

Write Row 5

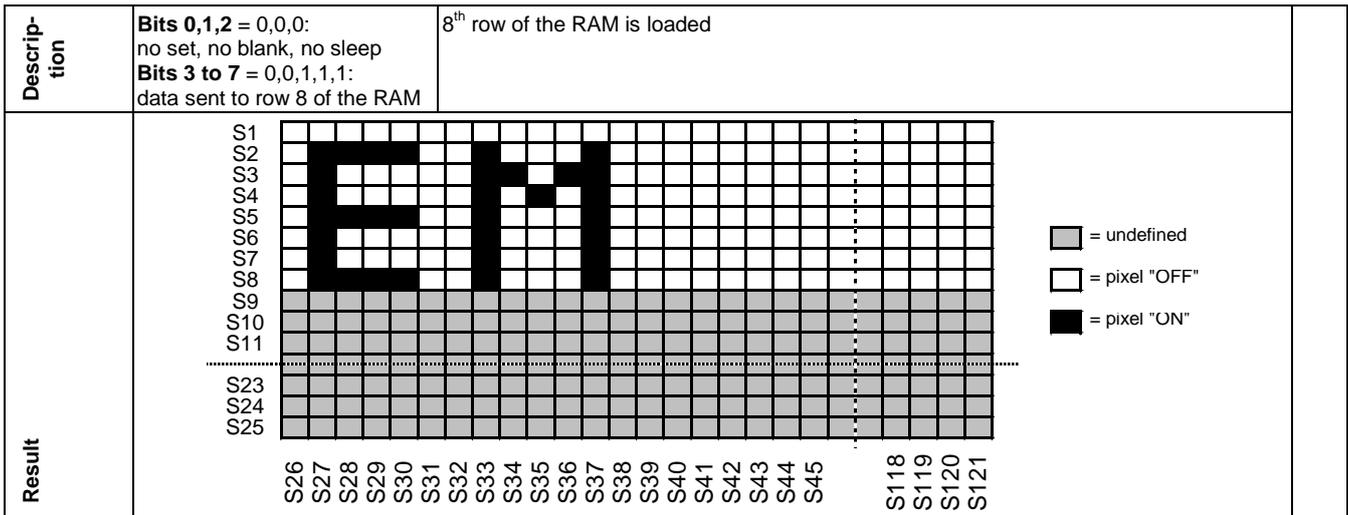


Fig. 18.09

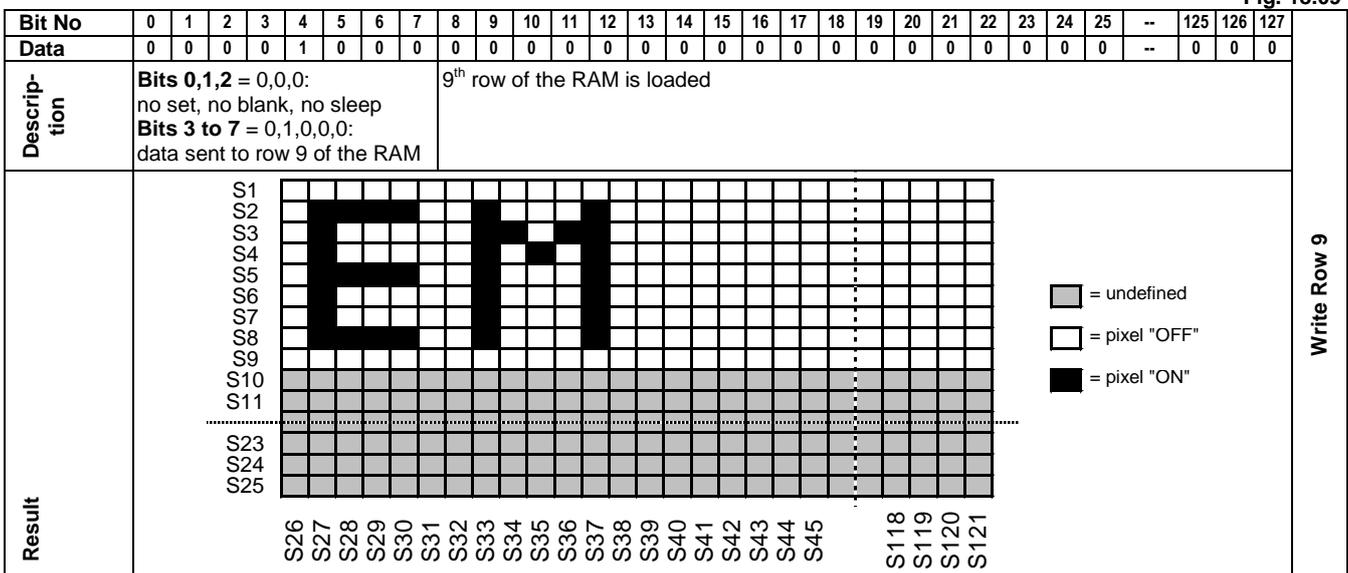


Fig. 18.10

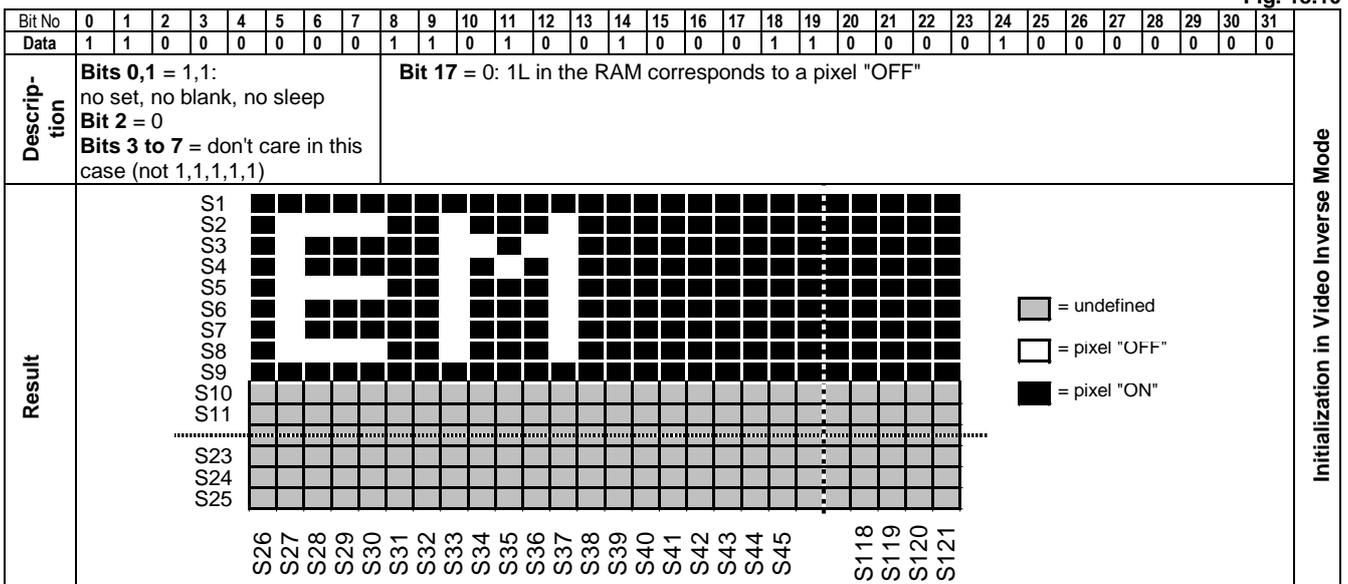


Fig. 18.11

Write Row 9

Initialization in Video Inverse Mode

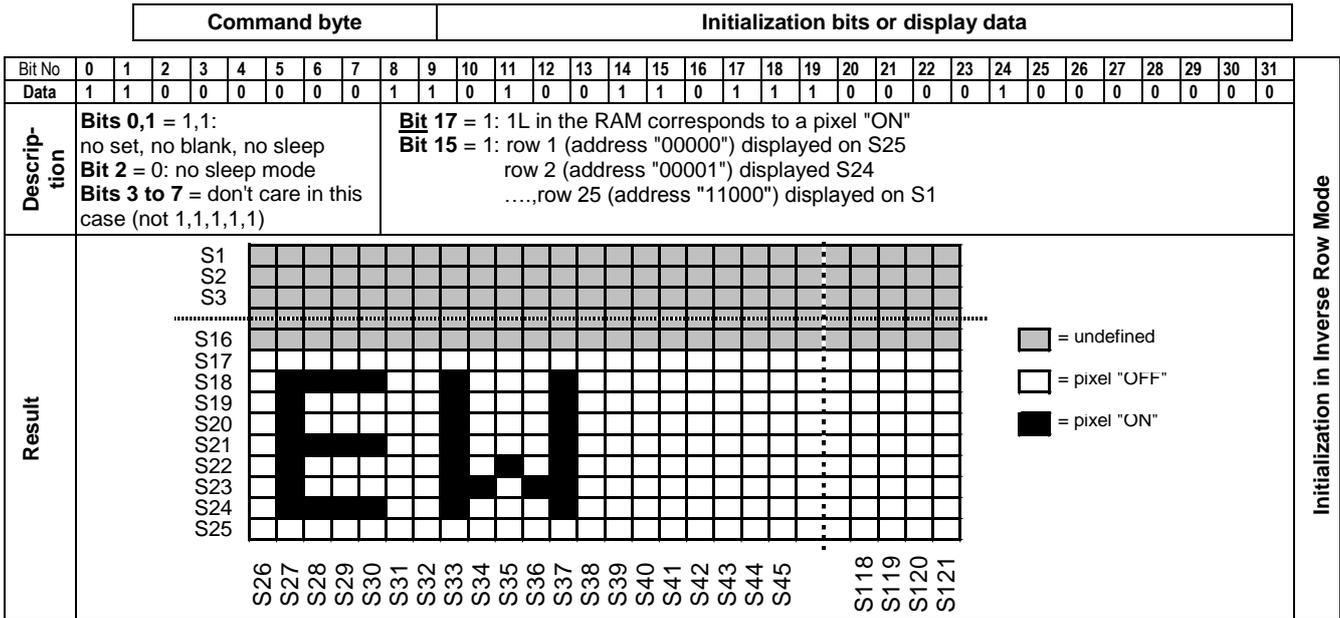


Fig. 18.12

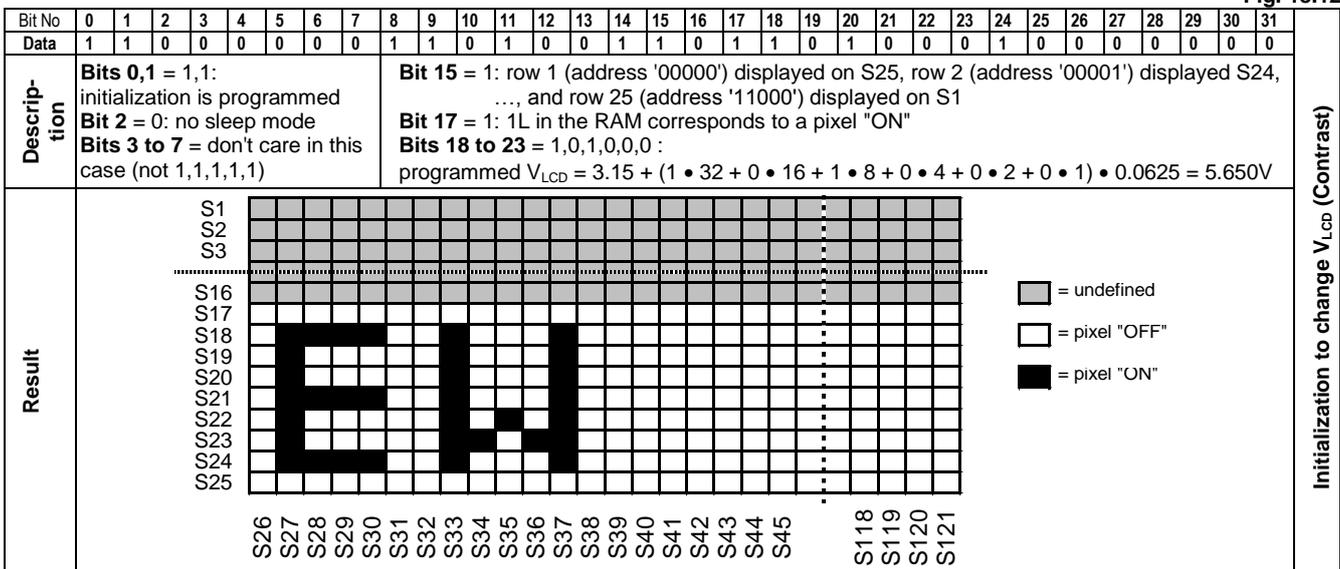


Fig. 18.13

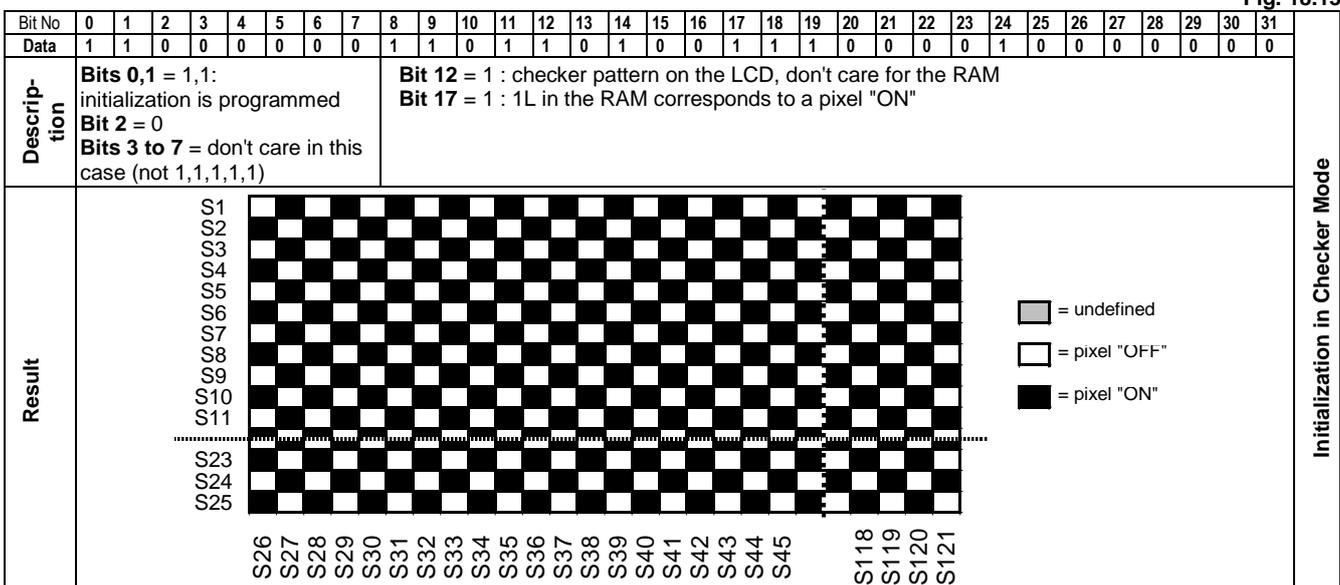


Fig. 18.14

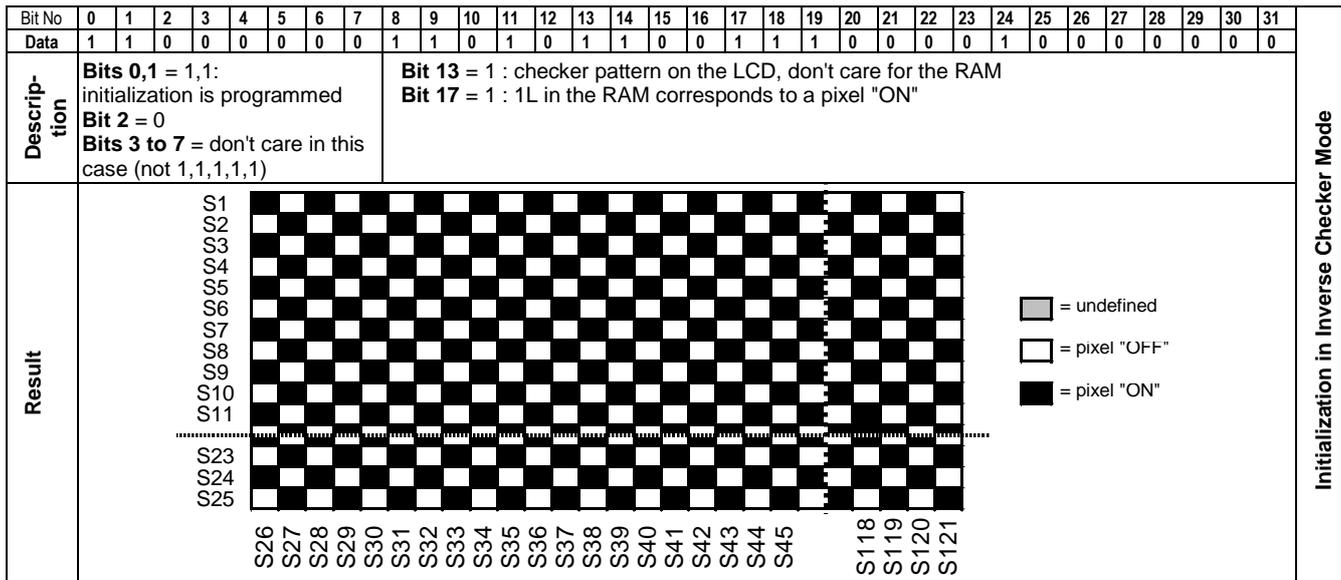


Fig. 18.15

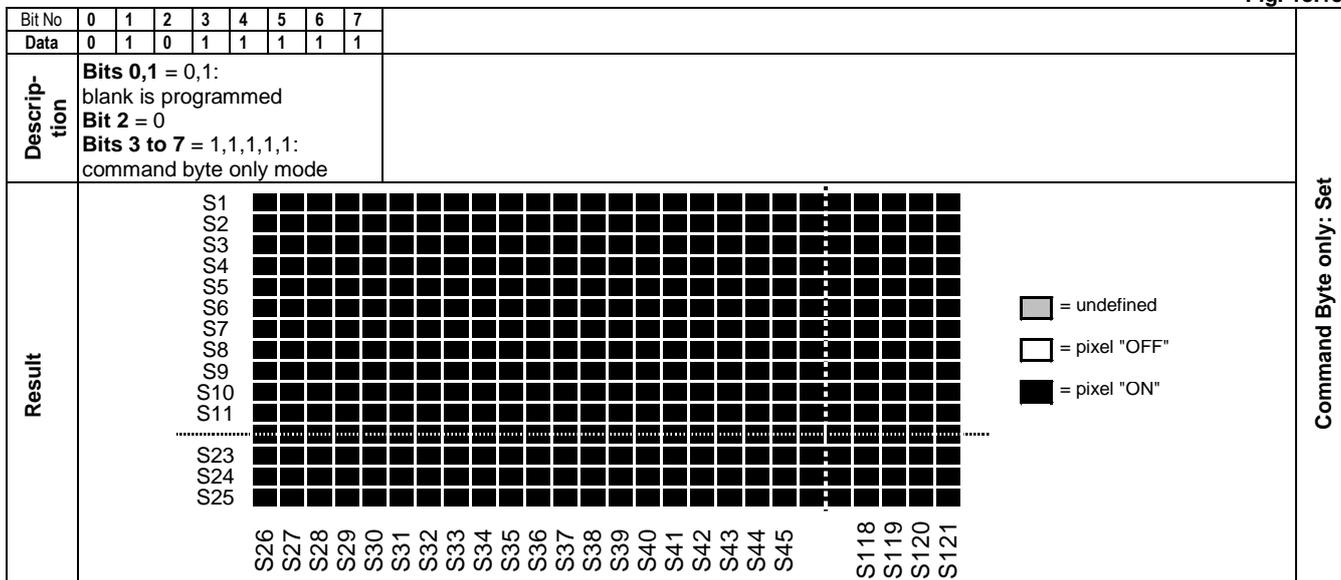


Fig. 18.16

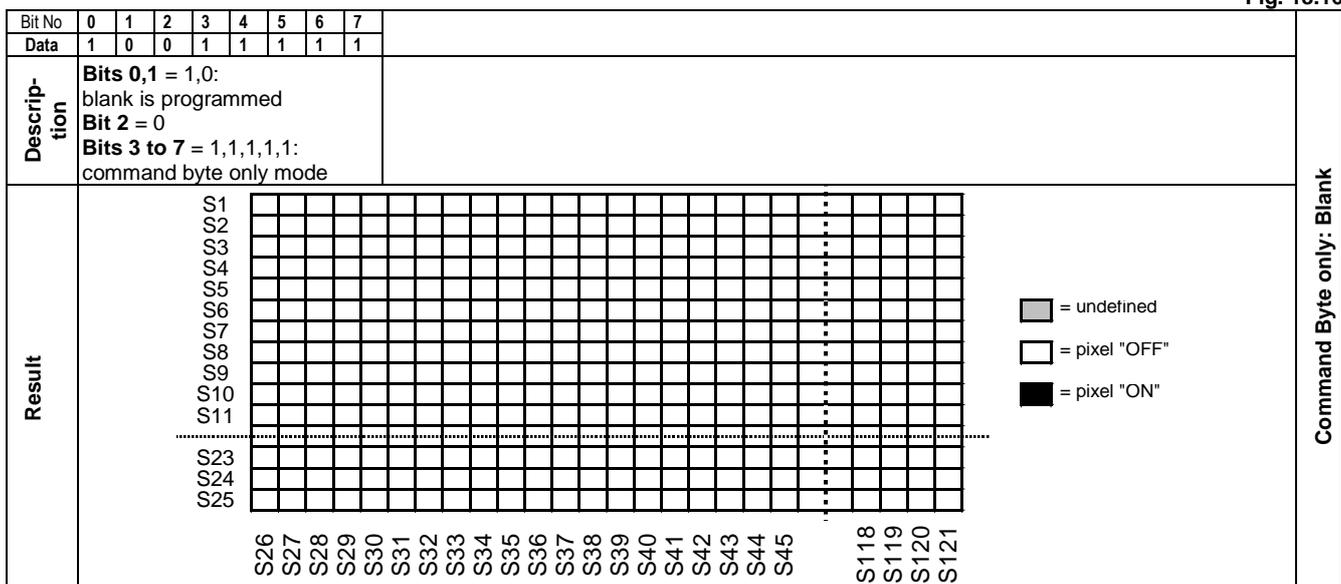


Fig. 18.17

Applications

Two EM6124 work in parallel to drive up to 50 rows x 96 columns or 25 rows x 212 columns as below

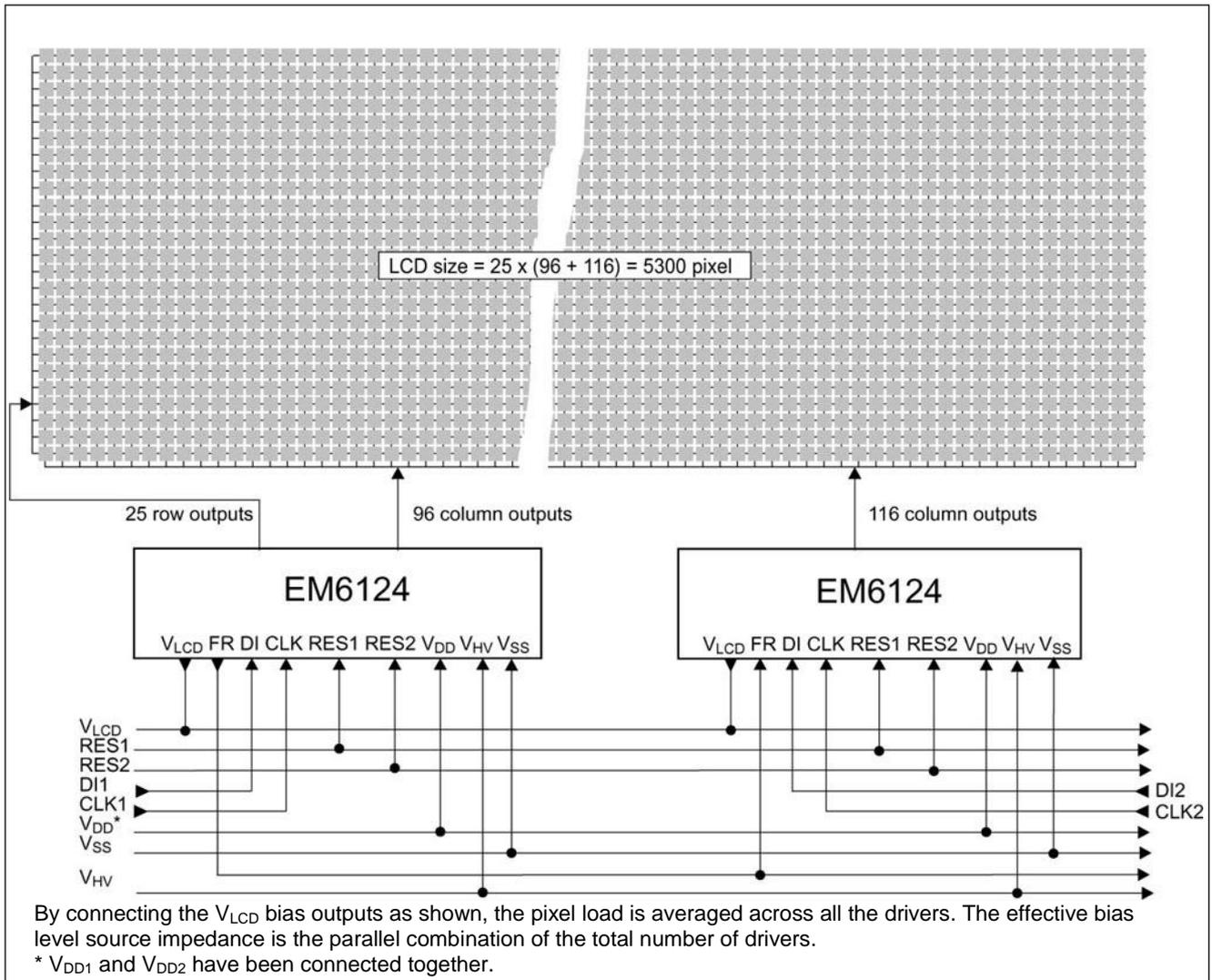


Fig. 19

Contacting Power Supply

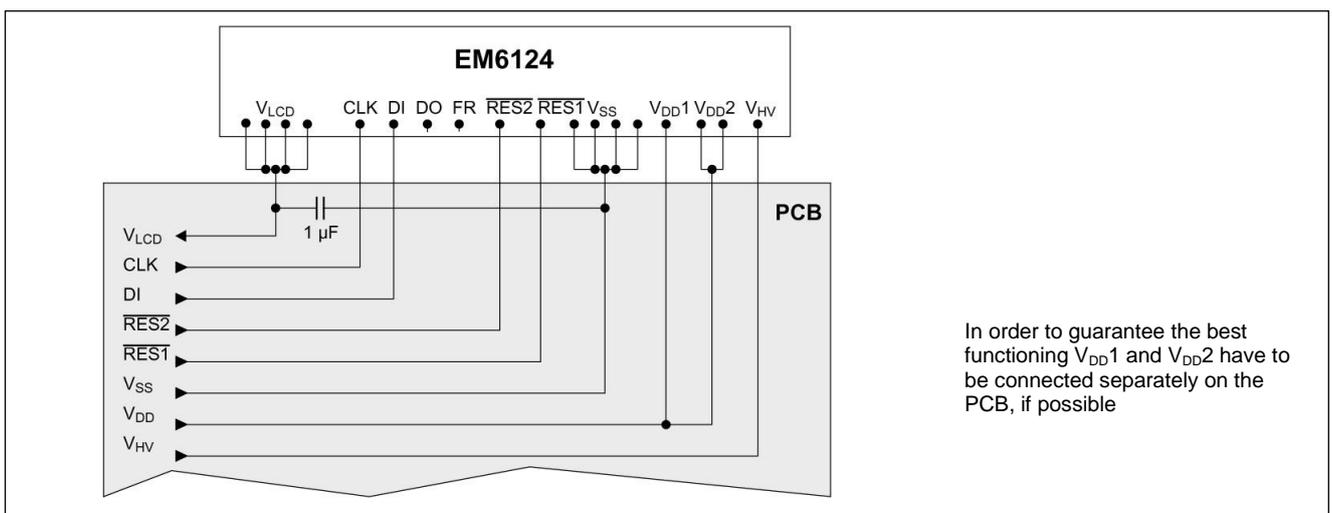


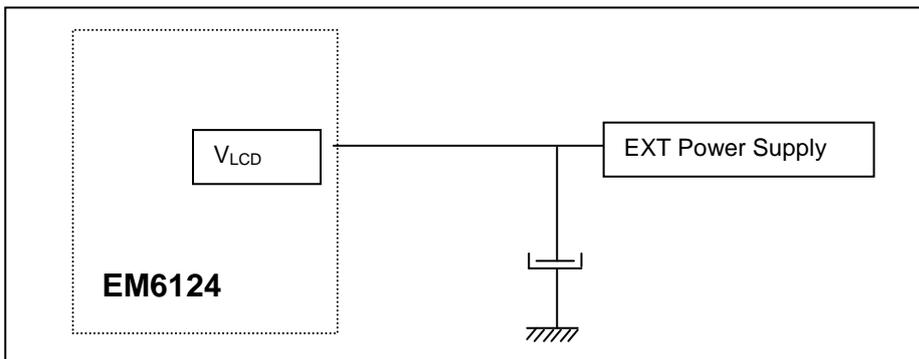
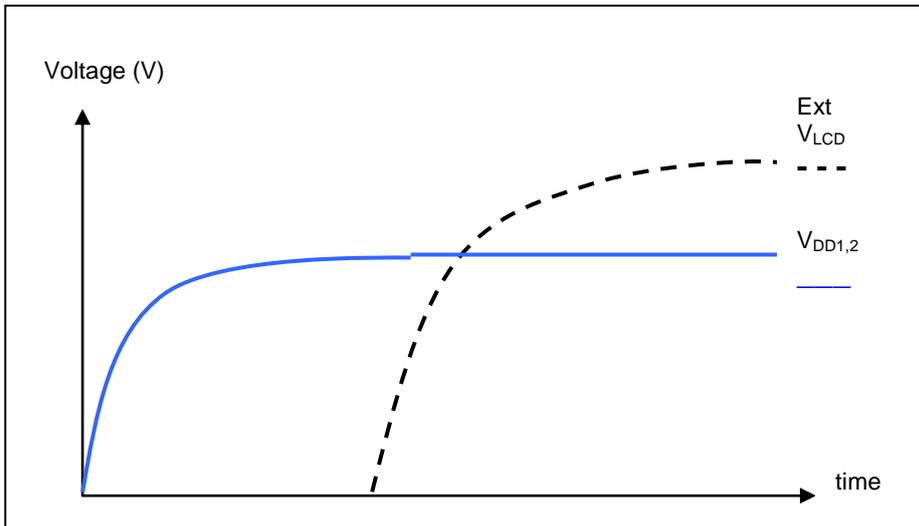
Fig. 20

Applications

Recommended flow to use EM6124 with external VLCD power supply.

Power Supplies:

- VHV pad should be connected to GND.
- Power should be applied first on VDD1,2 then on VLCD (external).

**Initialization sequence method:**

The software should be adapted to avoid high current consumption.

If external VLCD is lower than the internally generated VLCD then EM6124 will understand that the level set by the user is not achieved and it will increase the current to achieve the requested level.

For this reason VLCD step (bit18 to 23) should be set to "000000b" which means 3V then the minimum voltage.

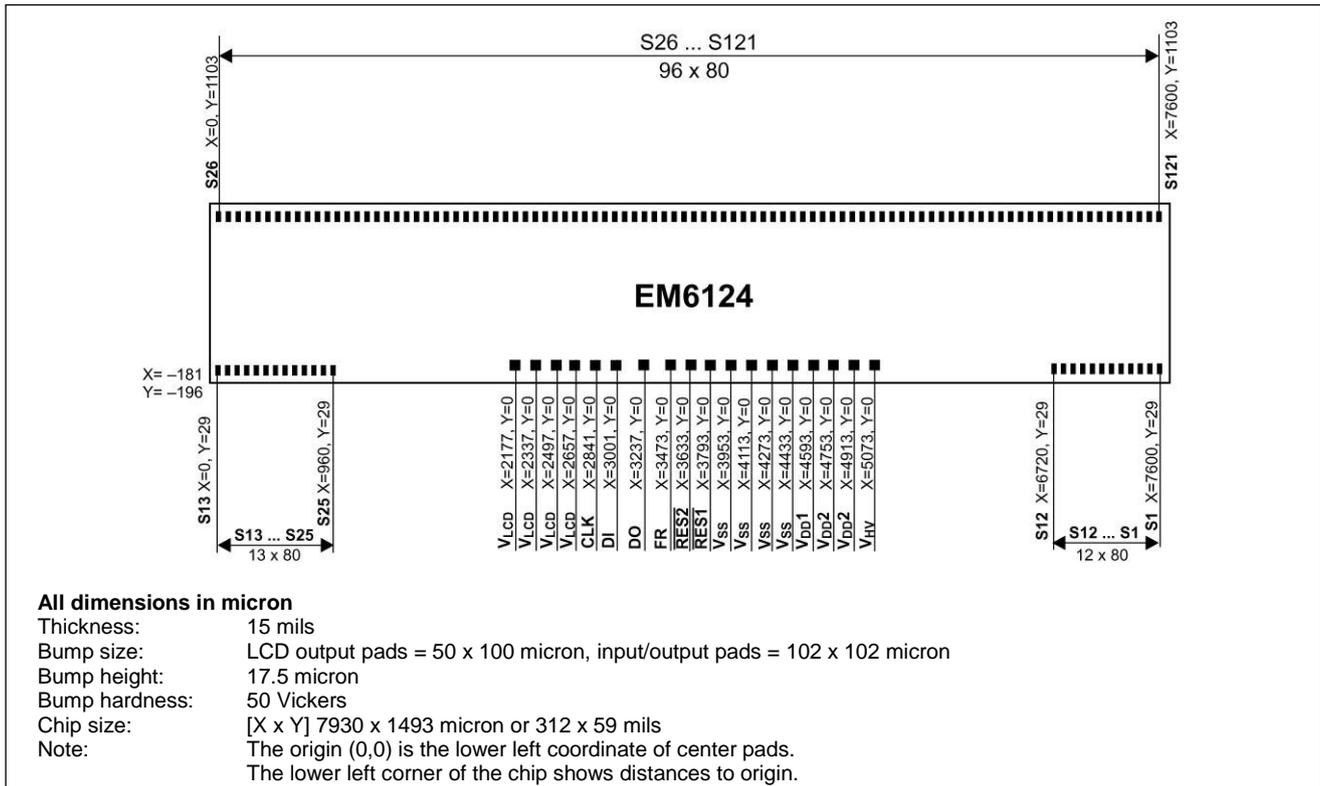
Dimensions of Chip Form and Bumped Die


Fig. 21

Ordering Information

When ordering, please specify the complete Part Number

Part Number	Recommended for cascaded applications (see p.16)	Die Form	Bumping
EM6124V1WP15E	Yes	Die in waffle pack, 15 mils thickness	With gold bumps
EM6124V2WP15E	No	Die in waffle pack, 15 mils thickness	With gold bumps

 For other delivery form in die (with or without bumps), please contact EM Microelectronic-Marine S.A.
 Minimum order quantity might apply.

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