OKI Semiconductor

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MSM511664C/CL

65,536-Word × 16-Bit DYNAMIC RAM : FAST PAGE MODE TYPE (BYTE WRITE)

DESCRIPTION

The MSM511664C/CL is a 65,536-word × 16-bit dynamic RAM fabricated in Oki's silicon-gate CMOS technology. The MSM511664C/CL achieves high integration, high-speed operation, and low-power consumption because Oki manufactures the device in a quadruple-layer polysilicon/single-layer metal CMOS process. The MSM511664C/CL is available in a 40-pin plastic SOJ or 44/40-pin plastic TSOP. The MSM511664CL (the low-power version) is specially designed for lower-power applications.

FEATURES

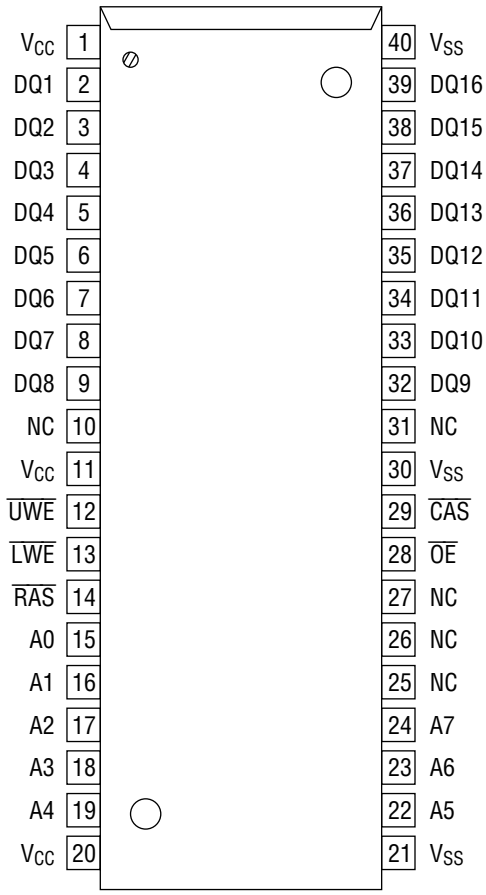
- 65,536-word × 16-bit configuration
- Single 5 V power supply, ±10% tolerance
- Input : TTL compatible, low input capacitance
- Output : TTL compatible, 3-state
- Refresh : 256 cycles/4 ms, 256 cycles/32 ms (L-version)
- Byte write and fast page mode, read modify write capability
- $\overline{CAS}$ before $\overline{RAS}$ refresh, hidden refresh, $\overline{RAS}$-only refresh capability
- Package options:

40-pin 400 mil plastic SOJ	(SOJ40-P-400-1.27)	(Product : MSM511664C/CL-xxJS)
44/40-pin 400 mil plastic TSOP	(TSOPII44/40-P-400-0.80-K)	(Product : MSM511664C/CL-xxTS-K)
		xx indicates speed rank.

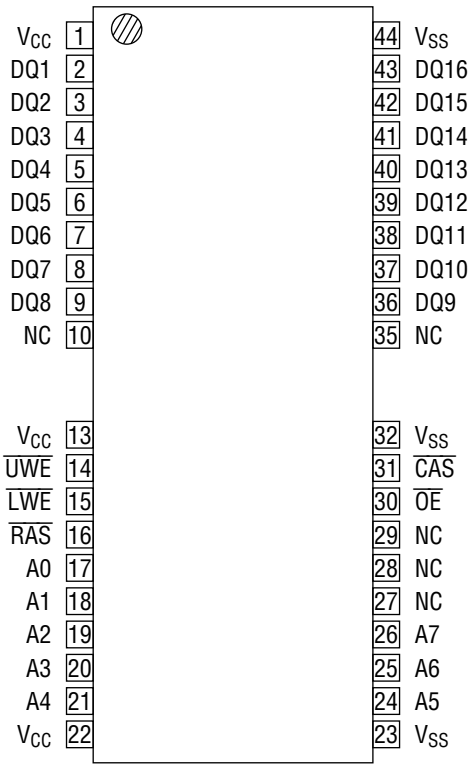
PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}	t_{OEA}		Operating (Max.)	Standby (Max.)
MSM511664C/CL-60	60 ns	30 ns	20 ns	20 ns	110 ns	550 mW	5.5 mW/ 1.1 mW (L-version)
MSM511664C/CL-70	70 ns	40 ns	25 ns	25 ns	120 ns	495 mW	
MSM511664C/CL-80	80 ns	45 ns	30 ns	30 ns	135 ns	440 mW	

PIN CONFIGURATION (TOP VIEW)



40-Pin Plastic SOJ

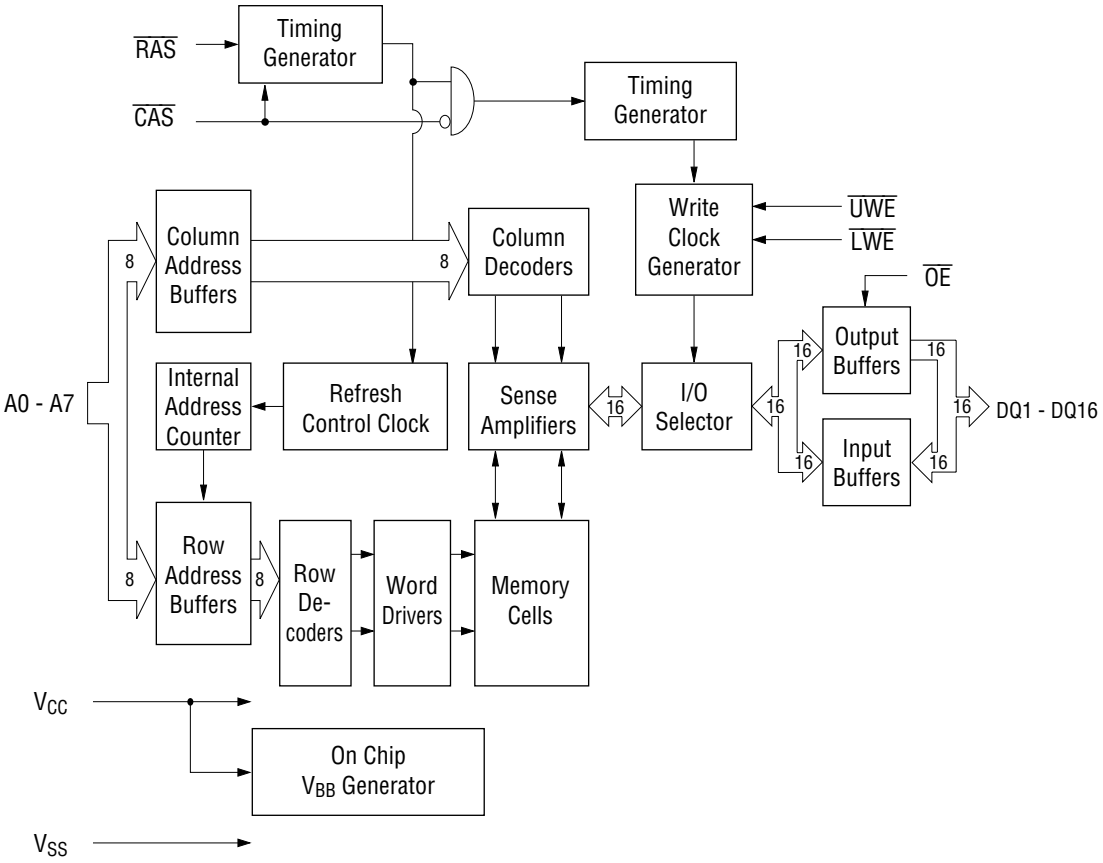


44/40-Pin Plastic TSOP
(K Type)

Pin Name	Function
A0 - A7	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
DQ1 - DQ16	Data Input/Data Output
$\overline{OE}$	Output Enable
$\overline{LWE}$	Lower Byte Write Enable
$\overline{UWE}$	Upper Byte Write Enable
V_{CC}	Power Supply (5 V)
V_{SS}	Ground (0 V)
NC	No Connection

Note : The same power supply voltage must be provided to every V_{CC} pin, and the same GND voltage level must be provided to every V_{SS} pin.

BLOCK DIAGRAM



FUNCTION TABLE

Input Pin					DQ Pin		Function Mode
$\overline{RAS}$	$\overline{CAS}$	$\overline{LWE}$	$\overline{UWE}$	$\overline{OE}$	DQ1 - DQ8	DQ9 - DQ16	
H	*	*	*	*	High-Z	High-Z	Standby
L	H	*	*	*	High-Z	High-Z	Refresh
L	L	H	H	L	D_{OUT}	D_{OUT}	Word Read
L	L	L	H	H	D_{IN}	Don't Care	Lower Byte Write
L	L	H	L	H	Don't Care	D_{IN}	Upper Byte Write
L	L	L	L	H	D_{IN}	D_{IN}	Word Write
L	L	H	H	H	High-Z	High-Z	—

*: "H" or "L"

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	–1.0 to 7.0	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_D*	1	W
Operating Temperature	T_{opr}	0 to 70	°C
Storage Temperature	T_{stg}	–55 to 150	°C

*: Ta = 25°C

Recommended Operating Conditions

(Ta = 0°C to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	6.5	V
Input Low Voltage	V_{IL}	–1.0	—	0.8	V

Capacitance

(V_{CC} = 5 V ±10%, Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A7)	C_{IN1}	—	7	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{UWE}$, $\overline{LWE}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ1 - DQ16)	$C_{I/O}$	—	7	pF

DC Characteristics

(V_{CC} = 5 V ±10%, Ta = 0°C to 70°C)

Parameter	Symbol	Condition	MSM511664 C/CL-60		MSM511664 C/CL-70		MSM511664 C/CL-80		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	V_{OH}	I_{OH} = –2.5 mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	I_{OL} = 2.1 mA	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	I_{LI}	0 V ≤ V_I ≤ 6.5 V; All other pins not under test = 0 V	–10	10	–10	10	–10	10	µA	
Output Leakage Current	I_{LO}	DQ disable 0 V ≤ V_O ≤ 5.5 V	–10	10	–10	10	–10	10	µA	
Average Power Supply Current (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = Min.	—	100	—	90	—	80	mA	1, 2
Power Supply Current (Standby)	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	—	2	—	2	—	2	mA	1
		$\overline{RAS}$, $\overline{CAS}$	—	1	—	1	—	1		
		≥ V_{CC} –0.2 V	—	200	—	200	—	200	µA	1, 5
Average Power Supply Current ($\overline{RAS}$-only Refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = Min.	—	100	—	90	—	80	mA	1, 2
Power Supply Current (Standby)	I_{CC5}	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, DQ = enable	—	5	—	5	—	5	mA	1
Average Power Supply Current ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	I_{CC6}	$\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$	—	100	—	90	—	80	mA	1, 2
Average Power Supply Current (Fast Page Mode)	I_{CC7}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = Min.	—	95	—	85	—	75	mA	1, 3
Average Power Supply Current (Battery Backup)	I_{CC10}	t_{RC} = 125 µs, $\overline{CAS}$ before $\overline{RAS}$, t_{RAS} ≤ 1 µs	—	300	—	300	—	300	µA	1, 4, 5

Notes : 1. I_{CC} Max. is specified as I_{CC} for output open condition.
2. The address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. The address can be changed once or less while $\overline{CAS}$ = V_{IH}.
4. V_{CC} – 0.2 V ≤ V_{IH} ≤ 6.5 V, –1.0 V ≤ V_{IL} ≤ 0.2 V.
5. L-version.

AC Characteristics (1/2)

(V_{CC} = 5 V ±10%, Ta = 0°C to 70°C) Note 1, 2, 3

Parameter	Symbol	MSM511664 C/CL-60		MSM511664 C/CL-70		MSM511664 C/CL-80		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	110	—	120	—	135	—	ns	
Read Modify Write Cycle Time	t_{RWC}	155	—	170	—	185	—	ns	
Fast Page Mode Cycle Time	t_{PC}	40	—	50	—	55	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t_{PRWC}	85	—	95	—	100	—	ns	
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	ns	4, 5, 6
Access Time from $\overline{CAS}$	t_{CAC}	—	20	—	25	—	30	ns	4, 5
Access Time from Column Address	t_{AA}	—	30	—	40	—	45	ns	4, 6
Access Time from $\overline{CAS}$ Precharge	t_{CPA}	—	35	—	45	—	50	ns	4
Access Time from $\overline{OE}$	t_{OEA}	—	20	—	25	—	30	ns	4
Output Low Impedance Time from $\overline{CAS}$	t_{CLZ}	0	—	0	—	0	—	ns	4
$\overline{CAS}$ to Data Output Buffer Turn-off Delay Time	t_{OFF}	0	20	0	20	0	20	ns	7
$\overline{OE}$ to Data Output Buffer Turn-off Delay Time	t_{OEZ}	0	15	0	15	0	15	ns	7
Transition Time	t_T	3	50	3	50	3	50	ns	3
Refresh Period	t_{REF}	—	4	—	4	—	4	ms	
Refresh Period (L-version)	t_{REF}	—	32	—	32	—	32	ms	
$\overline{RAS}$ Precharge Time	t_{RP}	40	—	40	—	45	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	20	—	25	—	30	—	ns	
$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	t_{ROH}	15	—	15	—	15	—	ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	20	10,000	25	10,000	30	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	—	5	—	5	—	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35	—	45	—	50	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	40	20	45	22	50	ns	5
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	30	17	35	ns	6
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	12	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	10	—	10	—	15	—	ns	
Column Address Hold Time from $\overline{RAS}$	t_{AR}	45	—	45	—	55	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	40	—	45	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	ns	8
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	ns	8

AC Characteristics (2/2)

(V_{CC} = 5 V ±10%, Ta = 0°C to 70°C) Note 1, 2, 3

Parameter	Symbol	MSM511664 C/CL-60		MSM511664 C/CL-70		MSM511664 C/CL-80		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	9
Write Command Hold Time	t_{WCH}	10	—	10	—	15	—	ns	
Write Command Hold Time from $\overline{RAS}$	t_{WCR}	40	—	45	—	55	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	15	—	ns	
$\overline{OE}$ Command Hold Time	t_{OEH}	10	—	10	—	10	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	—	20	—	20	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20	—	20	—	20	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	ns	10
Data-in Hold Time	t_{DH}	10	—	10	—	15	—	ns	10
Data-in Hold Time from $\overline{RAS}$	t_{DHR}	40	—	45	—	55	—	ns	
$\overline{OE}$ to Data-in Delay Time	t_{OED}	15	—	15	—	15	—	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	40	—	50	—	55	—	ns	9
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	50	—	60	—	70	—	ns	9
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	80	—	95	—	105	—	ns	9
$\overline{CAS}$ Precharge $\overline{WE}$ Delay Time	t_{CPWD}	55	—	70	—	75	—	ns	9
$\overline{CAS}$ Active Delay Time from $\overline{RAS}$ Precharge	t_{RPC}	0	—	0	—	0	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	5	—	5	—	5	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	10	—	10	—	10	—	ns	

Notes:

1. A start-up delay of 100 µs is required after power-up, followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh or $\overline{CAS}$ before $\overline{RAS}$ refresh) before proper device operation is achieved.

2. The AC characteristics assume t_T = 5 ns.

3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring input timing signals. Transition times (t_T) are measured between V_{IH} and V_{IL}.

4. This parameter is measured with a load circuit equivalent to 1 TTL load and 50 pF.

5. Operation within the t_{RCD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then the access time is controlled by t_{CAC}.

6. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, then the access time is controlled by t_{AA}.

7. t_{OFF} (Max.) and t_{OEZ} (Max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.

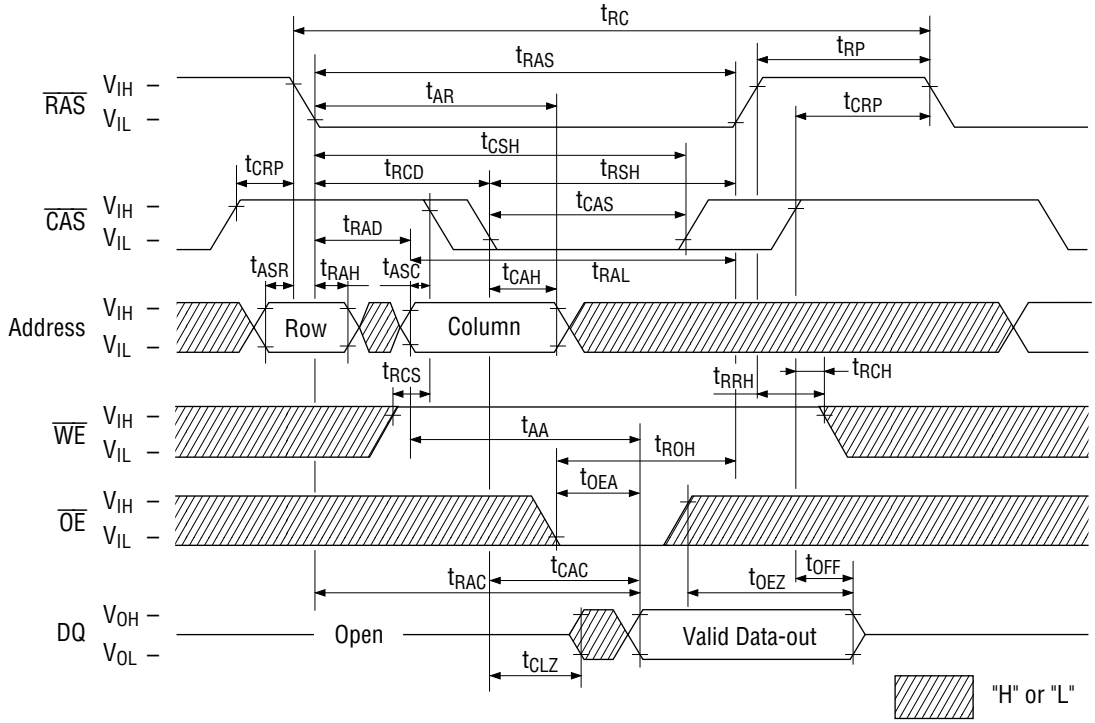
8. t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. t_{WCS}, t_{CWD}, t_{RWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (Min.), then the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (Min.) , $t_{RWD} \geq t_{RWD}$ (Min.), $t_{AWD} \geq t_{AWD}$ (Min.) and $t_{CPWD} \geq t_{CPWD}$ (Min.), then the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, then the condition of the data out (at access time) is indeterminate.

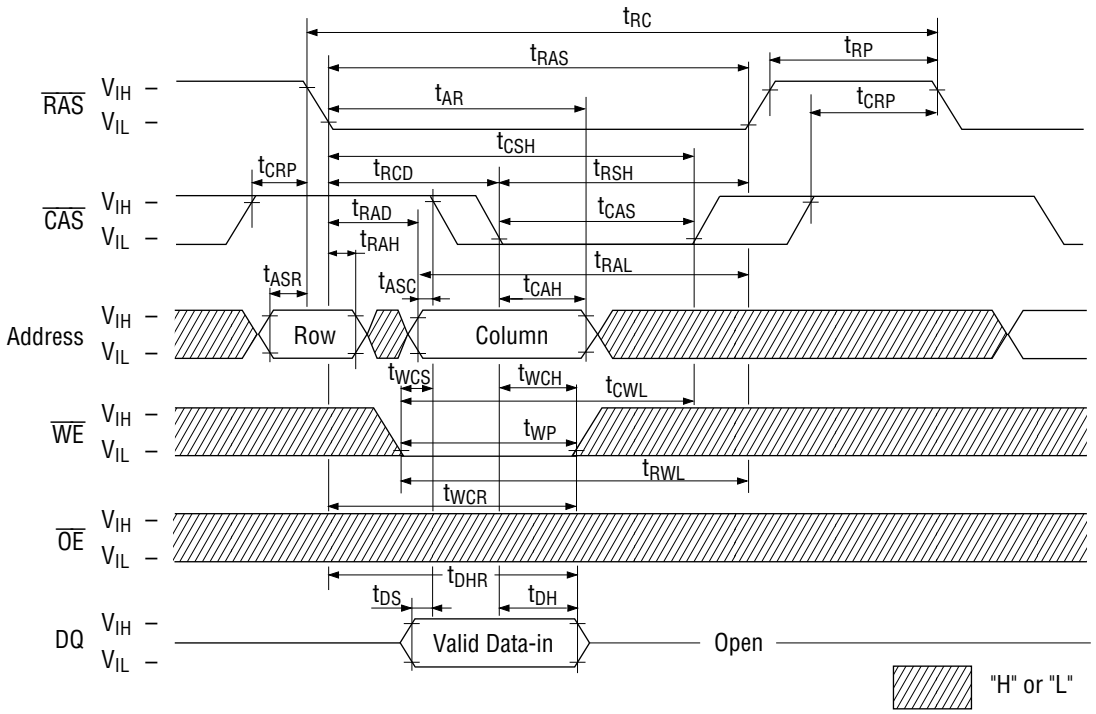
10. These parameters are referenced to the $\overline{CAS}$ leading edge in an early write cycle, and to the $\overline{WE}$ leading edge in an $\overline{OE}$ control write cycle, or a read modify write cycle.

TIMING WAVEFORM

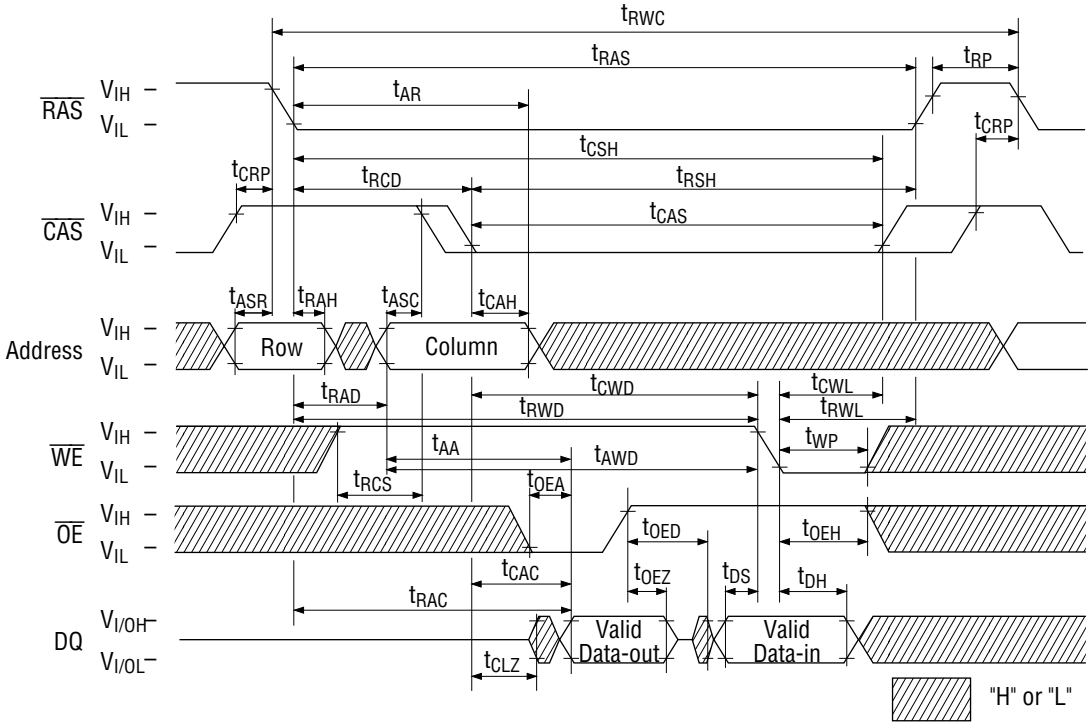
Read Cycle



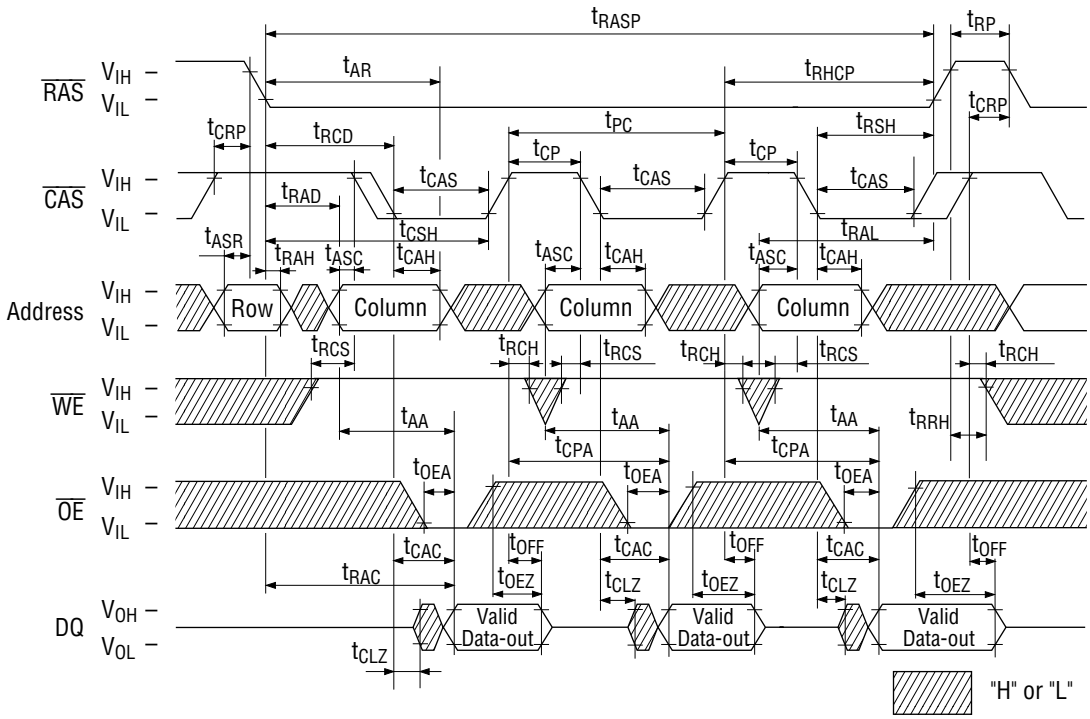
Write Cycle (Early Write)



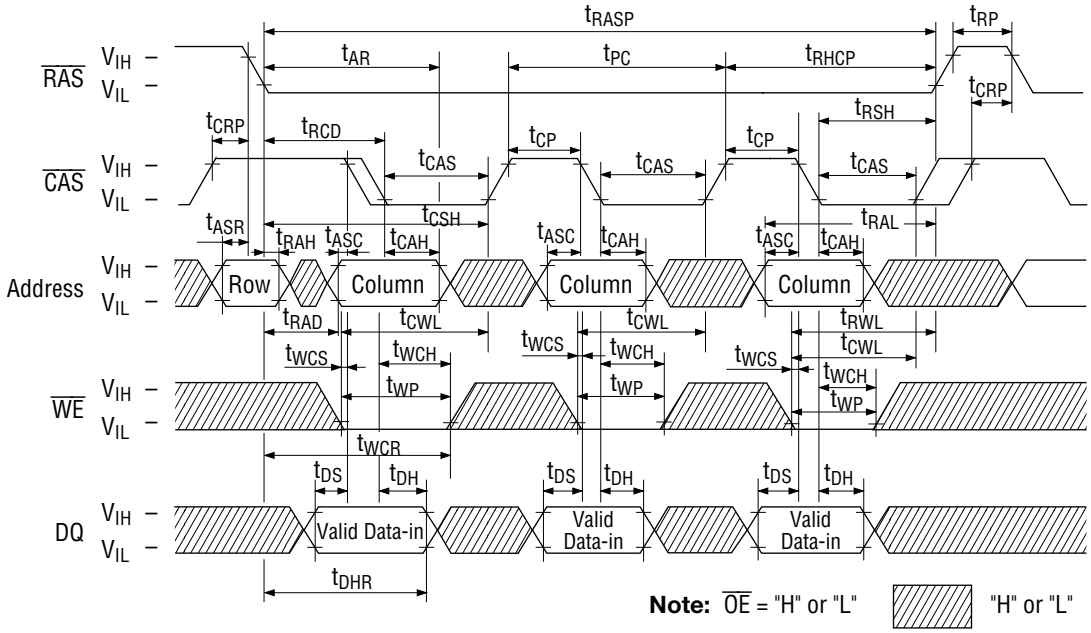
Read Modify Write Cycle



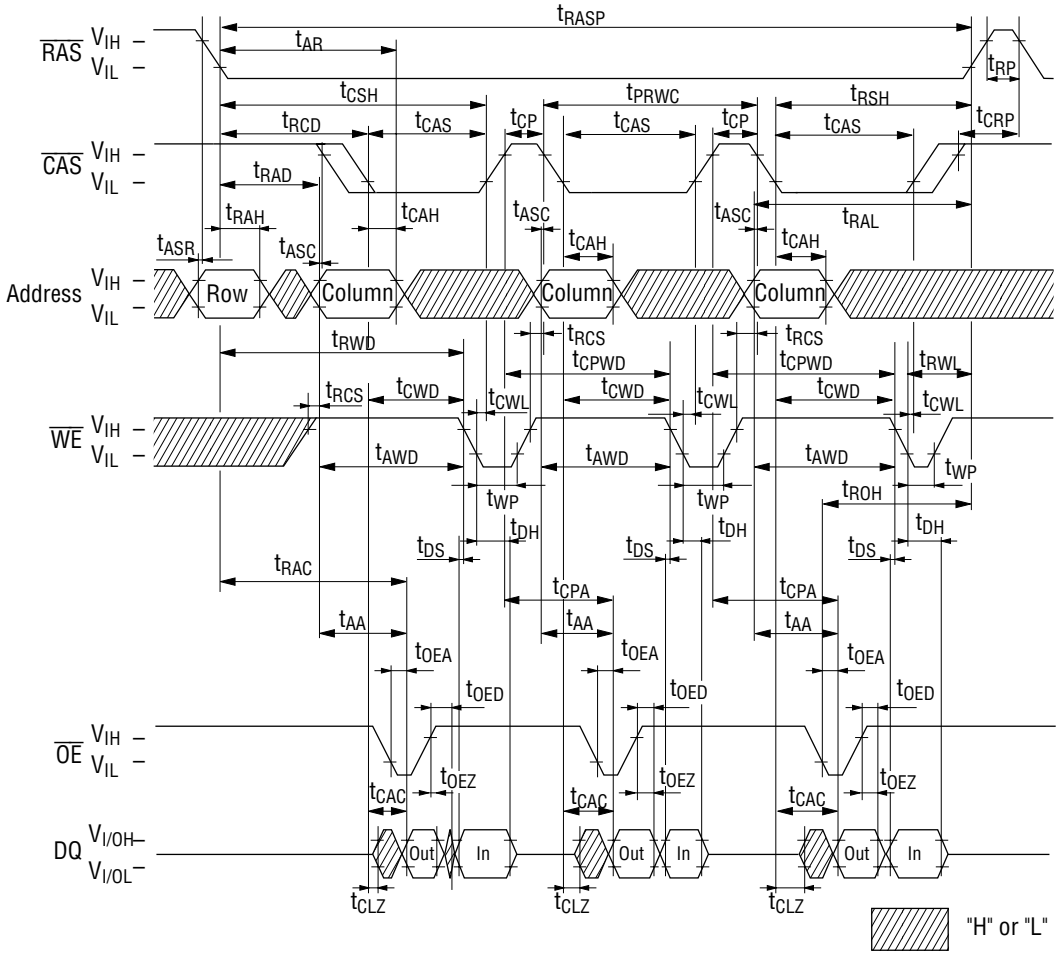
Fast Page Mode Read Cycle



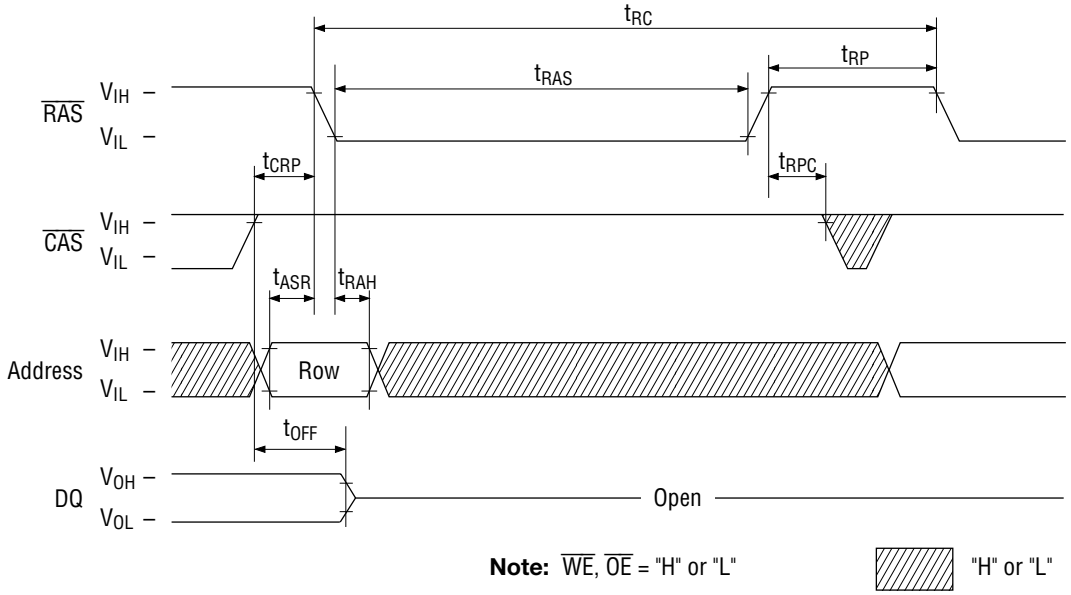
Fast Page Mode Write Cycle (Early Write)



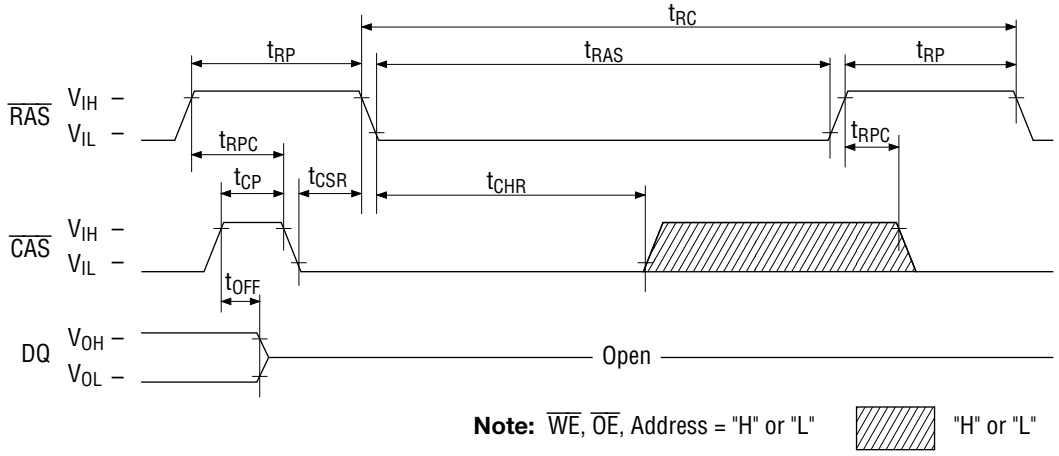
Fast Page Mode Read Modify Write Cycle



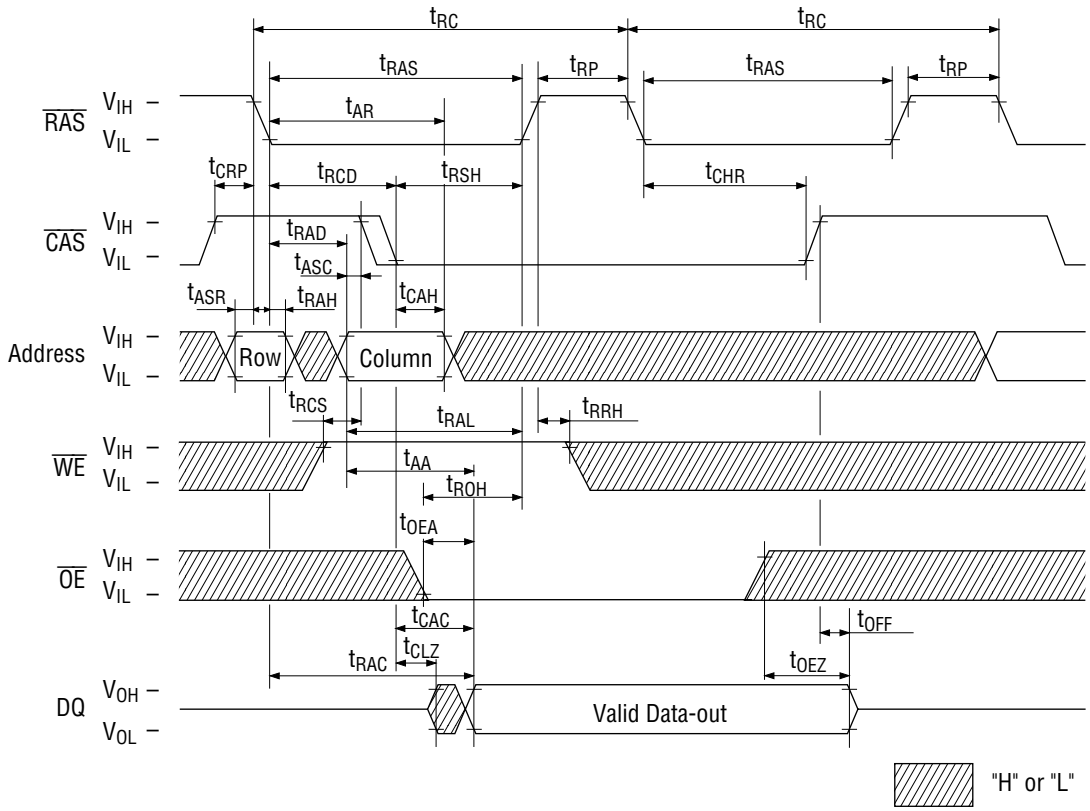
RAS-Only Refresh Cycle



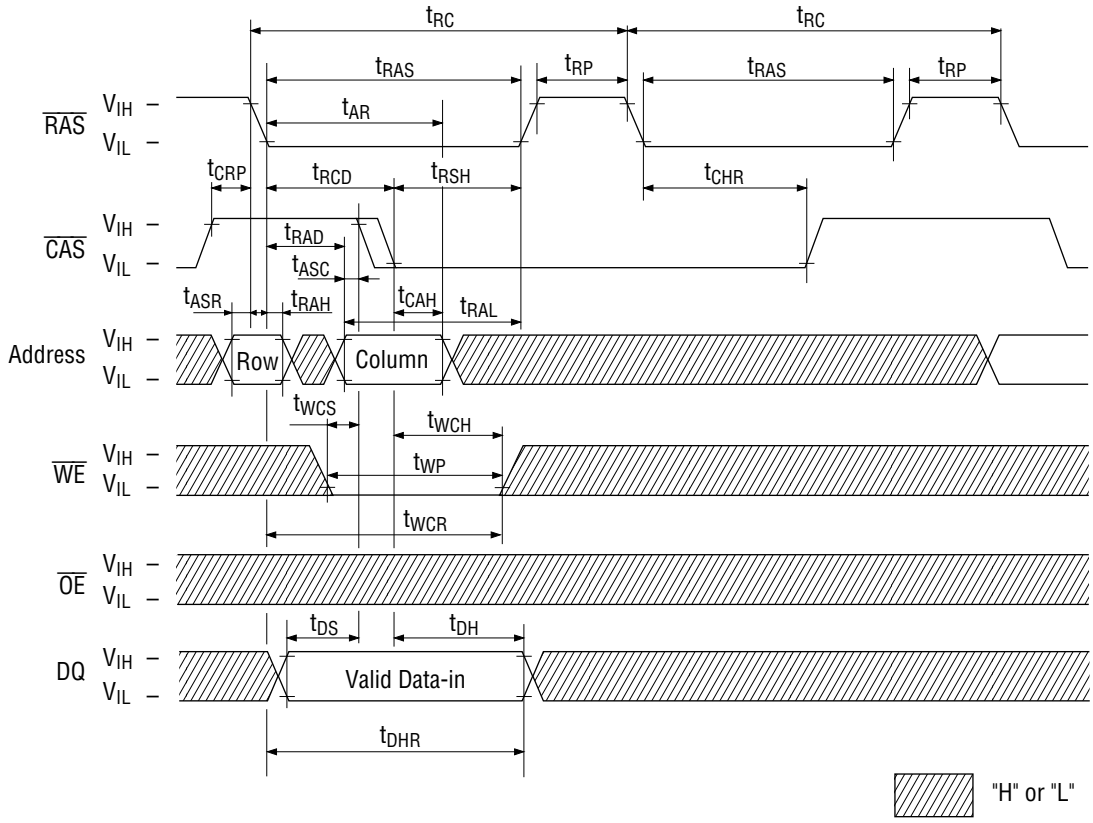
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle



Hidden Refresh Read Cycle



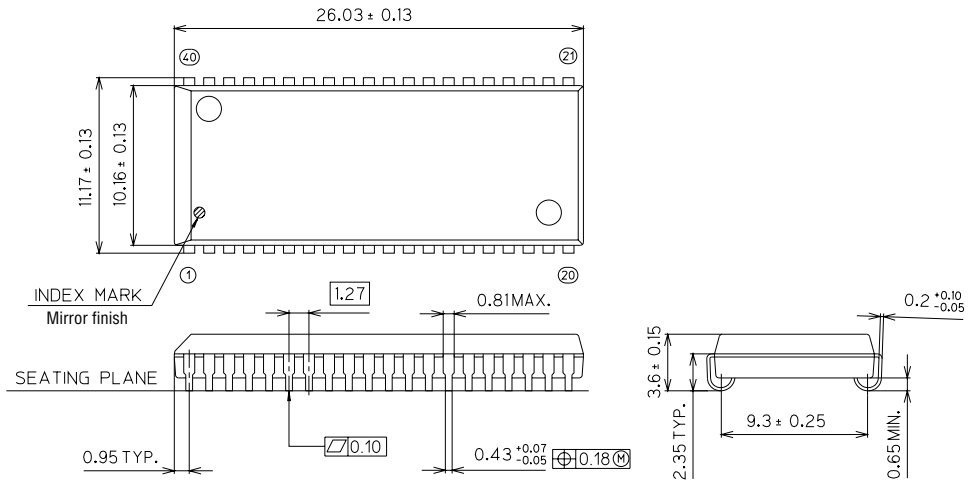
Hidden Refresh Write Cycle



PACKAGE DIMENSIONS

(Unit : mm)

SOJ40-P-400-1.27



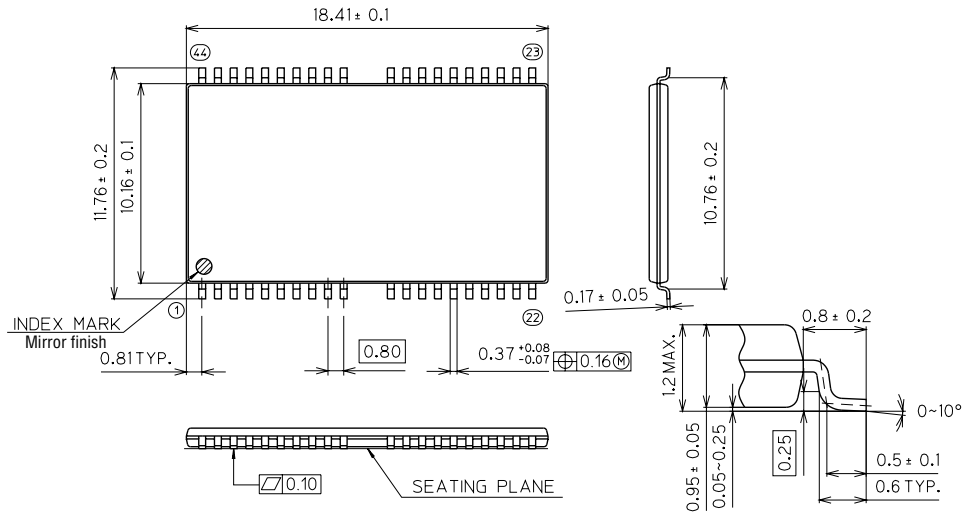
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	1.70 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

TSOPII44/40-P-400-0.80-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.49 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).