INTERNATIONAL CMOS TECHNOLOGY, INC.

T-46-19-07

PEEL™ 20CG10

CMOS Programmable Electrically Erasable Logic Device

Features

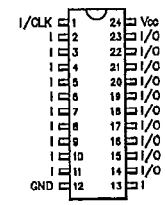
- **Advanced CMOS EEPROM Technology**
- **High Performance, Low Power Consumption**
  - — t_{PD} = 20ns, fmax= 40MHz
  - — I_{CC} = 55mA + 0.5mA/MHz
- **EE Reprogrammability**
  - — Low risk reprogrammable inventory
  - — Superior programming and functional yield
  - — Erases and programs in seconds
- **Development and Programming Support**
  - — Third-party software and programmers
  - — ICT PEEL Development System and Software
- **Architectural Flexibility**
  - — 92 product term X 44 input AND array
  - — Up to 22 inputs and 10 outputs
  - — Independently programmable 12-configuration I/O macrocells
  - — Synchronous preset, asynchronous clear
  - — Independently programmable output enables
- **Application Versatility**
  - — Replaces random SSI/MSI logic
  - — Emulates 24-pin bipolar PAL devices
  - — Convert 24-pin PAL and EPLD designs with ICT software
  - — Superset compatible with the CMOS PALC20G10

General Description

The ICT PEEL20CG10 is a CMOS Programmable Electrically Erasable Logic Device that provides a high-performance, low-power, reprogrammable, and architecturally enhanced alternative to conventional programmable logic devices (PLDs). Designed in advanced CMOS EEPROM technology, the PEEL20CG10 rivals speed parameters of comparable bipolar PLDs while dramatically improving power consumption. EE reprogrammability allows for cost effective plastic packaging, low risk inventory, reduced development and retrofit costs, and enhanced testability to ensure 100% field programmability and function.

The PEEL20CG10's flexible architecture and ICT's JEDEC file translator allows the PEEL20CG10 to replace bipolar 24-pin PAL devices without the need to rework the existing design. Applications for the PEEL20CG10 include: replacement of random SSI/MSI logic circuitry; emulation of 24-pin bipolar PAL devices; and user customized sequential and combinatorial functions such as counters, shift registers, state machines, address decoders, multiplexers, etc. Development and programming support for the PEEL20CG10 is provided by ICT and third-party manufacturers.

Pin Configuration (Figure 1)



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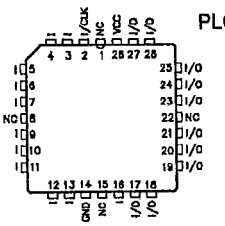
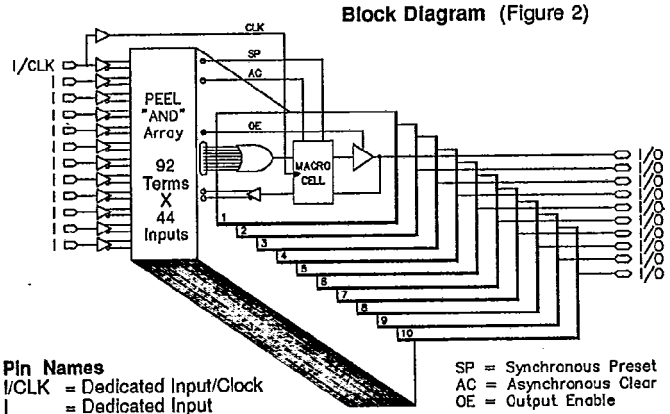


PLCC

Block Diagram (Figure 2)



Pin Names

I/CLK = Dedicated Input/Clock
I = Dedicated Input
I/O = Bidirectional I/O
GND = Ground
Vcc = Power Supply

SP = Synchronous Preset
AC = Asynchronous Clear
OE = Output Enable

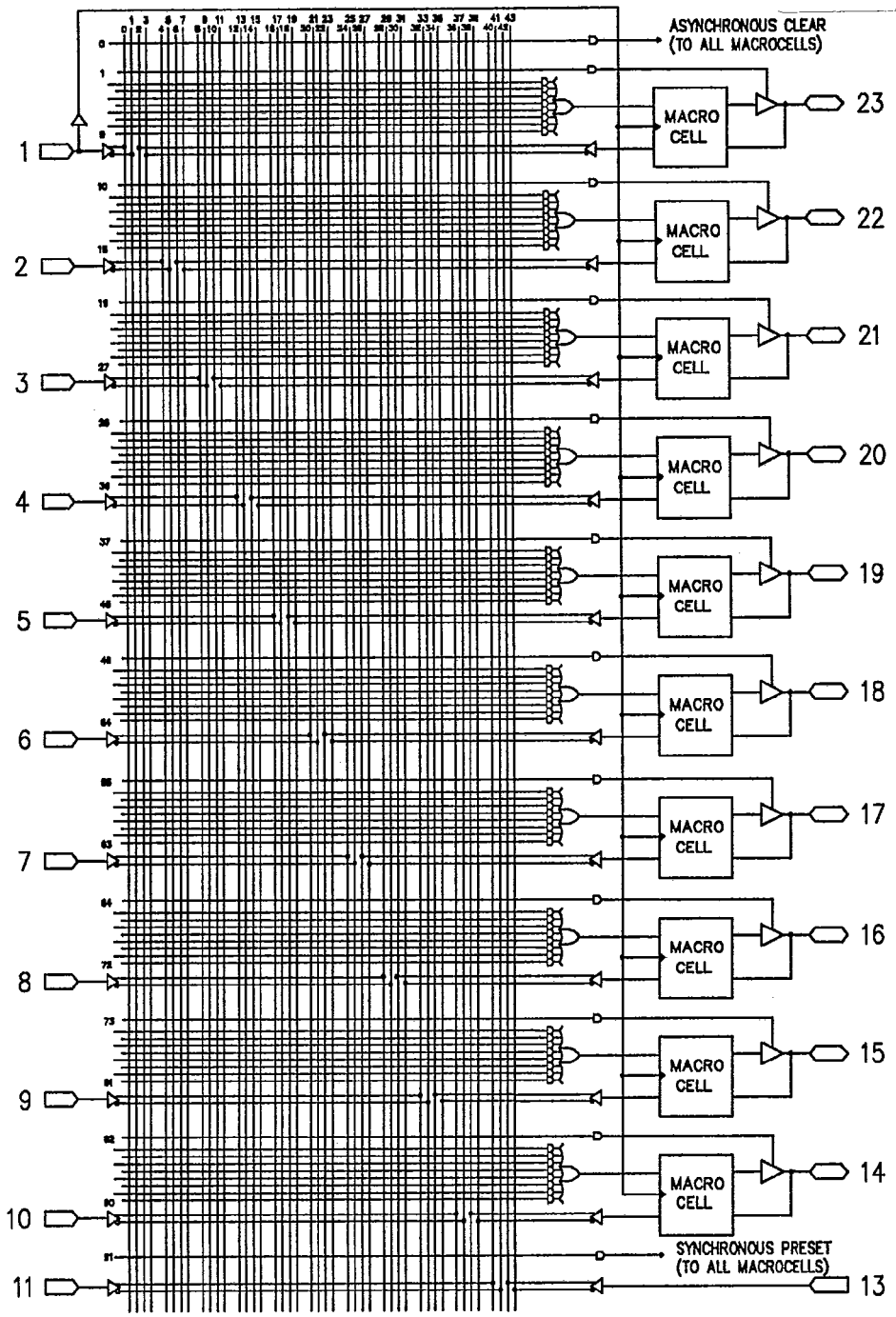


Figure 3. PEEL20CG10 Logic Array Diagram

Function Description

The PEEL20CG10 implements logic functions as sum-of-products expressions in a programmable-AND/fixed-OR logic array. User-defined functions are created by programming the connections of input signals into the array. User-configurable output structures in the form of I/O macrocells further increase logic flexibility.

Architecture Overview

The PEEL20CG10 architecture is illustrated in the block diagram of figure 2. Twelve dedicated inputs and 10 I/Os provide up to 22 inputs and 10 outputs for creation of logic functions. At the core of the device is a programmable electrically-erasable AND array which drives a fixed OR array. With this structure the PEEL20CG10 can implement up to 10 sum-of-products logic expressions.

Associated with each of the 10 OR functions is an I/O macrocell which can be independently programmed to one of 12 different configurations. The programmable macrocells allow each I/O to create sequential or combinatorial logic functions of active-high or active-low polarity, while providing three different feedback paths into the AND array.

AND/OR Logic Array

The programmable AND array of the PEEL20CG10 (shown in figure 3) is formed by input lines intersecting product terms. The input lines and product terms are used as follows:

44 Input Lines:

- 24 input lines carry the true and complement of the signals applied to the 12 input pins
- 20 additional lines carry the true and complement values of feedback or input signals from the 10 I/Os

92 product terms:

- 80 product terms (8 per I/O)
- 10 output enable terms (one for each I/O)
- 1 global synchronous present term
- 1 global asynchronous clear term

At each input-line/product-term intersection there is an EEPROM memory cell which determines whether or not there is a logical connection at that intersection. Each product term is essentially a 44-input AND gate. A product term which is connected to both the true and complement of an input signal will always be FALSE and thus will not effect the OR function that it drives. When all the connections on a product term are opened, a don't care state exists and that term will always be TRUE.

When programming the PEEL20CG10, the device programmer first performs a bulk erase to instantly remove the previous pattern. The erase cycle opens every logical connection in the array. The device is configured to perform the user-defined function by programming selected connections in the AND array. (Note that PEEL device programmers automatically program the connections on unused product terms so that they will have no effect on the output function)

Programmable I/O Macrocell

The unique twelve-configuration output macrocell provides complete control over the architecture of each output. The ability to configure each output independently permits users to tailor the configuration of the PEEL20CG10 to the precise requirements of their designs.

Macrocell Architecture

Each I/O macrocell, as shown in figure 4, consists of a D-type flip-flop and two signal-select multiplexers. The configuration of each macrocell is determined by the four EEPROM bits controlling these multiplexers. These bits determine: output polarity; output type (registered or non-registered); and input/feedback path (bi-directional I/O, combinatorial feedback, or register feedback). Table 1 shows the bit settings for each of the twelve macrocell configurations.

Equivalent circuits for the twelve macrocell configurations are illustrated in figure 5. In addition to emulating the four PAL-type output structures (configurations 3, 4, 9, and 10) the macrocell provides eight configurations that are unavailable in any PAL device.

Output Type

The signal from the OR array can be fed directly to the output pin or latched in the D-type flip-flop (registered function). The D-type flip-flop latches data on the rising edge of the clock and is controlled by the global preset and clear terms. When the synchronous preset term is satisfied, the Q output of the register will be set HIGH at the next rising edge of the clock input. Satisfying the asynchronous clear term will set Q LOW, regardless of the clock state. If both terms are satisfied simultaneously, the clear will override the preset.

Output Polarity
Each macrocell can be configured to implement active-high or active-low logic. Programmable polarity eliminates the need for external inverters.

Output Enable
The output of each I/O macrocell can be enabled or disabled under the control of its associated programmable output enable product term. When the logical conditions programmed on the output enable term are satisfied, the output signal is propagated to the I/O pin. Otherwise, the output buffer is driven into the high-impedance state.

Under the control of the output enable term, the I/O pin can function as a dedicated input, a dedicated output, or a bi-directional I/O. Opening every connection on the output enable term will permanently enable the output buffer and yield a dedicated output. Conversely, if every connection is intact, the enable term will always be logically false and the I/O will function as a dedicated input.

Input/Feedback Select
The PEEL20CG10 macrocell also provides control over the feedback path. The input/feedback signal associated with each I/O macrocell may be obtained from three different locations: from the I/O pin (bi-directional I/O); directly from the Q output of the flip-flop (registered feedback); or directly from the OR gate (combinatorial feedback).

Bi-directional I/O
The input/feedback signal is taken from the I/O pin when using the pin as a dedicated input or as a bi-directional I/O. (Note that it is possible to create a registered output function with bi-directional I/O.)

Combinatorial Feedback
The signal-select multiplexer gives the macrocell the ability to feedback the output directly from the OR gate, regardless of whether the output function is registered or combinatorial. This feature allows the creation of asynchronous latches, even when the output must be disabled. (Refer to configurations 5, 6, 7, and 8 in figure 5.)

Registered Feedback

Feedback also can be taken from the register, regardless of whether the output function is to be combinatorial or registered. When implementing configurations 11 and 12 in figure 5, the register can be used for internal latching of data while leaving the external output free for combinatorial functions.

Design Security
The PEEL20CG10 provides a special EEPROM security bit that prevents unauthorized reading or copying of designs programmed into the device. The security bit is set by the PLD programmer, either at the conclusion of the programming cycle or as a separate step, after the device has been programmed. Once the security bit is set it is impossible to verify (read) or program the PEEL until the entire device has first been erased with the bulk-erase function.

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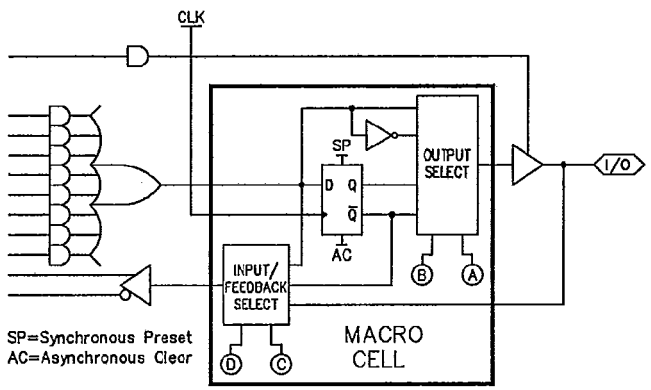

Figure 4. Block Diagram of the PEEL20CG10 I/O Macrocell

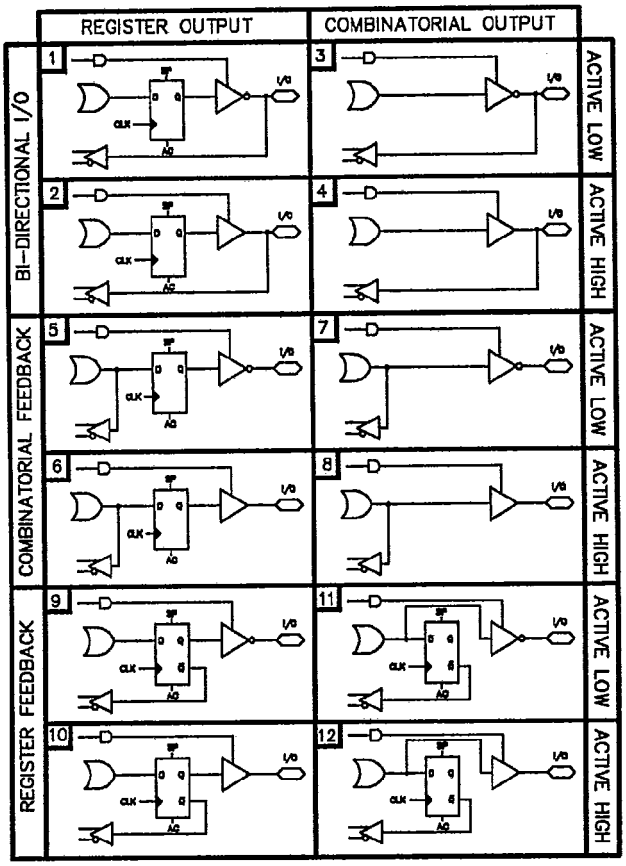

Figure 5. Equivalent Circuits for the Twelve Configurations of the PEEL20CG10 I/O Macrocell.

Configuration #	A B C D	Input/Feedback Select	Output Select	
1	0 0 1 0	Bi-Directional I/O	Register	Active Low
2	1 0 1 0	"	"	Active High
3	0 1 0 0	"	Combinatorial	Active Low
4	1 1 0 0	"	"	Active High
5	0 0 1 1	Combinatorial Feedback	Register	Active Low
6	1 0 1 1	"	"	Active High
7	0 1 1 1	"	Combinatorial	Active Low
8	1 1 1 1	"	"	Active High
9	0 0 0 0	Register Feedback	Regisiter	Active Low
10	1 0 0 0	"	"	Active High
11	0 1 1 0	"	Combinatorial	Active Low
12	1 1 1 0	"	"	Active High

Table 1. PEEL20CG10 Macrocell Configuration Bits

INTERNATIONAL CMOS TECHNOLOGY, INC.

PEEL™20CG10

Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	– 0.5 to + 7.0	V
V_I, V_O	Voltage Applied to Any Pin [3]	Relative to GND [1]	– 0.5 to V_{CC} + 0.6	V
I_O	Output Current	Per pin (I_{OL}, I_{OH})	± 25	mA
T_{ST}	Storage Temperature		– 65 to + 125	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+ 300	°C

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Operating Ranges

Symbol	Alternate Source Symbol*	Parameter	Conditions	Min	Max	Unit
V_{CC}	V_{CC}	Supply Voltage	Commercial [2]	4.75	5.25	V
T_A	T_A	Ambient Temperature	Commercial [2]	0	70	°C
T_R		Clock Rise Time	See note 4		250	nS
T_F		Clock Fall Time	See note 4		250	nS
T_{RVCC}		VCC Rise Time	See note 4		250	mS

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D.C. Electrical Characteristics

Over the operating range

Symbol	Alternate Source Symbol*	Parameter	Conditions	Min	Max	Unit
V_{OH}	V_{OH}	Output HIGH Voltage - TTL	V_{CC} = Min, I_{OH} = –4.0mA	2.4		V
V_{OHC}		Output HIGH Voltage-CMOS	V_{CC} = Min, I_{OH} = –10µA	V_{CC} – 0.1		V
V_{OL}	V_{OL}	Output LOW Voltage - TTL	V_{CC} = Min, I_{OL} = 8mA		0.5	V
V_{OLC}		Output LOW Voltage-CMOS	V_{CC} = Min, I_{OL} = 10µA		0.1	V
V_{IH}	V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.3	V
V_{IL}	V_{IL}	Input LOW Level		– 0.3	0.8	V
I_{IX}	I_{IL},I_{IH},I_{IX}	Input Leakage Current	V_{CC} = Max, GND ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{OZ}	I_{OZ}	Output Leakage Current	I/O = High-Z, GND ≤ V_O ≤ V_{CC}		±10	µA
I_{SC}	I_{SC}	Output Short Circuit Current	V_{CC} = Max, V_O = 0.5V [10]	– 30	– 90	mA
I_{CCAC}	I_{CC}	V_{CC} Active Current CMOS	V_{IN} = V_{CC} or GND [5,11]		55 (*65) + 0.5mA/MHz	mA
I_{CCAT}	I_{CC}	V_{CC} Active Current, TTL	V_{IN} = V_{IL} or V_{IH} [5,11]		65 (*75) + 0.5mA/MHz	mA
C_{IN} [8]	C_{IN}	Input Capacitance	T_A = 25°C, V_{CC} = 5.0V @ f = 1MHz		6	pF
C_{OUT} [8]	C_{OUT}	Output Capacitance			12	pF

* Alternate source symbols are shown to compare PEEL20CG10 specifications to other pin-compatible devices.

* 20CG10-20 only

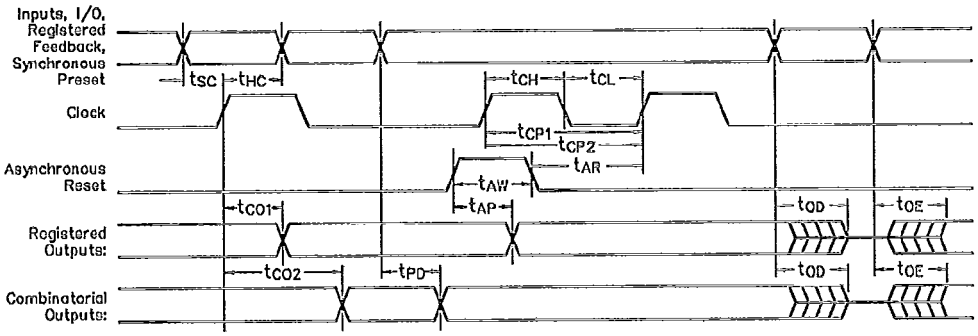
A.C. Electrical Characteristics

Over the Operating Range [9,12]

Symbol	Alternate Source Symbol*	Parameter	20CG10-20		20CG10-25		20CG10-35		Unit
			Min	Max	Min	Max	Min	Max	
t_{PD}	t_{PD}	Input[6] or feedback to non-registered output		20		25		35	ns
t_{OE}	t_{EA}	Input [6] to output enable [7]		20		25		30	ns
t_{OD}	t_{ER}	Input [6] to output disable [7]		20		25		30	ns
t_{CO1}	t_{CO}	Clock to output		15		15		20	ns
t_{CO2}		Clock to combinatorial output delay via internal registered feedback		30		35		45	ns
t_{SC}	t_S	Input [6] or feedback setup to clock	12		15		30		ns
t_{HC}	t_H	Input [6] hold after clock	0		0		0		ns
t_{CL},t_{CH}	t_W	Clock width - clock low time, clock high time [4]	12		13		15		ns
t_{CP1}		Minimum clock period (register feedback to registered output via internal path)	25		27		45		ns
f_{max1}		Maximum clock frequency ($1/t_{CP1}$)	40		37		22.2		MHz
t_{CP2}	t_P	Minimum clock period ($t_{SC} + t_{CO1}$)	27		30		50		ns
f_{max2}	f_{MAX}	Maximum clock frequency ($1/t_{CP2}$)	37		33.3		20		MHz
t_{AW}	t_{AW}	Asynchronous Reset pulse width	20		25		25		ns
t_{AP}	t_{AP}	Input [6] to Asynchronous Reset		25		25		35	ns
t_{AR}	t_{AR}	Asynchronous Reset recovery time		25		25		35	ns
t_{RESET}		Power-on reset time for registers in clear state [4]		5		5		5	µs

* Alternate source symbols are shown to compare the PEEL20CG10 specifications other pin-compatible devices.

Switching Waveforms



1. Minimum DC input is – 0.5V, however inputs may undershoot to – 2.0V for periods less than 20nS.
2. Voltage applied to input or output must not exceed V_{CC} +1.0V.
3. V_I and V_O are not specified for program/verify operation.
4. Test points for Clock and V_{CC} in t_R, t_F, t_{CL}, t_{CH}, and t_{RESET} are referenced at 10% and 90% levels.
5. I/O pins open (no load).
6. "Input" refers to an input pin signal.
7. t_{OE} is measured from input transition to $V_{REF} \pm 0.1V$, t_{OD} is measured from input transition to $V_{OH} - 0.1V$ or $V_{OL} + 0.1V$; $V_{REFF} = V_L$ see test loads at the end of this section.
8. Capacitances are tested on a sample basis.
9. Test conditions assume: signal transition times of 5ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
10. Test one output at a time for a duration of less than 1 sec.
11. ICC for a typical application: This parameter is tested with the device programmed as a 10-bit Counter.
12. PEEL Device test loads are specified at the end of this section.