

Description

The MSM832 is a high speed Static RAM organised as 32K x 8 available with access times of 55, 70, 85 or 100 ns. The device is available in five ceramic package options including the high density VIL™ package. It features completely static operation with a low power standby mode and is 3.0V battery back-up compatible. It is directly TTL compatible and has common data inputs and outputs.

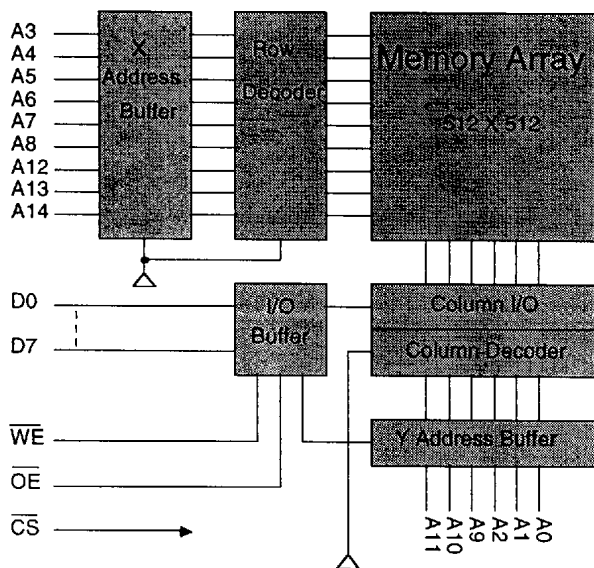
The device may be screened in accordance with MIL-STD-883.

32,768 x 8 CMOS High Speed Static RAM

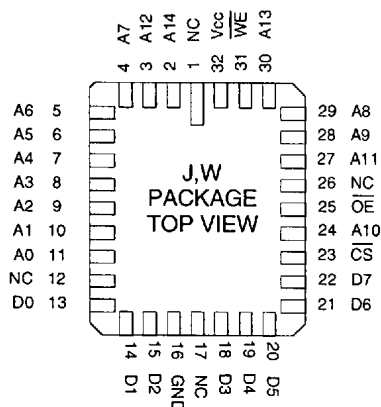
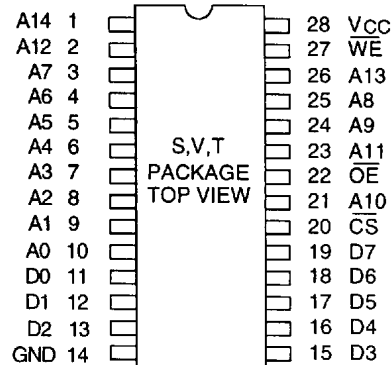
Features

- Access Times of 55/70/85/100 ns.
- Low Power Operation - 85 mW (max) .
- Low Power Standby - 1.1 mW (max) L version.
- Low Voltage Data Retention
- Directly TTL compatible.
- Completely Static Operation.
- JEDEC Standard footprint.

Block Diagram



Pin Definitions



Pin Functions

- A0-A14** Address inputs
- D0-7** Data Input/Output
- CS** Chip Select
- OE** Output Enable
- WE** Write Enable
- V_{CC}** Power(+5V)
- GND** Ground

Package Details

| Pin Count | Description | Package Type |
|-----------|--------------------------------|--------------|
| 28 | 0.6" Dual-in-Line (DIP) | S |
| 28 | 0.3" Dual-in-Line (SKINNY DIP) | T |
| 28 | 0.1" Vertical-in-Line (VIL™) | V |
| 32 | Leadless Chip Carrier (LCC) | W |
| 32 | J-Leaded Chip Carrier (JLCC) | J |

DC OPERATING CONDITIONS**Absolute Maximum Ratings**⁽¹⁾

| | | | |
|--|-----------|-------------|----|
| Voltage on any pin relative to V_{SS} ⁽²⁾ | V_T | -0.5V to +7 | V |
| Power Dissipation | P_T | 1 | W |
| Storage Temperature | T_{STG} | -65 to +150 | °C |

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) Pulse width:- 3.0V for less than 50ns.

Recommended Operating Conditions

| Parameter | Symbol | min | typ | max | |
|-----------------------|----------|------|-----|--------------|--------------------|
| Supply Voltage | V_{CC} | 4.5 | 5.0 | 5.5 | V |
| Input High Voltage | V_{IH} | 2.2 | - | $V_{CC}+0.5$ | V |
| Input Low Voltage | V_{IL} | -0.5 | - | 0.8 | V |
| Operating Temperature | T_A | 0 | - | 70 | °C |
| | T_{AL} | -40 | - | 85 | °C (Suffix I) |
| | T_{AM} | -55 | - | 125 | °C (Suffix M, MB) |

DC Electrical Characteristics ($V_{CC} = 5.0V \pm 10\%$, $T_A = -55^\circ C$ to $+125^\circ C$)

| Parameter | Symbol | Test Condition | min | typ | max | Unit |
|--------------------------|-----------|---|-----|-----|-----|---------|
| Input Leakage Current | I_{LI} | $V_{IN}=0V$ to V_{CC} | - | - | 2 | μA |
| Output Leakage Current | I_{LO} | $\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$, $V_{IO}=GND$ to V_{CC} | - | - | 2 | μA |
| Operating Supply Current | I_{CC1} | $\overline{CS}=V_{IL}$, $I_{IO}=0mA$, I/P's Static | - | - | 15 | mA |
| Average Supply Current | I_{CC2} | $\overline{CS}=V_{IL}$, $I_{IO}=0mA$, Min. Cycle, Duty=100% | - | - | 70 | mA |
| Standby Supply Current | I_{SB1} | $\overline{CS}=V_{IH}$, I/P's static | - | - | 3 | mA |
| -L Version | I_{SB2} | $\overline{CS} \geq V_{CC}-0.2V$, $0.2V \geq V_{IN} \geq V_{CC}-0.2V$ | - | - | 200 | μA |
| Output Voltage | V_{OL} | $I_{OL}=2.1mA$ | - | - | 0.4 | V |
| | V_{OH} | $I_{OH}=-1.0mA$ | 2.4 | - | - | V |

Typical values are at $V_{CC}=5.0V$, $T_A=25^\circ C$ and specified loading.

Capacitance ($V_{CC}=5V \pm 10\%$, $T_A=25^\circ C$)

| Parameter | Symbol | Test Condition | typ | max | Unit |
|--------------------|----------|----------------|-----|-----|------|
| Input Capacitance: | C_{IN} | $V_{IN}=0V$ | - | 8 | pF |
| I/O Capacitance: | C_{IO} | $V_{IO}=0V$ | - | 10 | pF |

Note: This parameter is sampled and not 100% tested.

Operating Modes

The table below shows the logic inputs required to control the operating modes the MSM832.

| Mode | \overline{CS} | \overline{OE} | \overline{WE} | V_{CC} Current | I/O Pin | Reference Cycle |
|---------------|-----------------|-----------------|-----------------|--------------------|-----------|-----------------|
| Not Selected | 1 | X | X | I_{SB1}, I_{SB2} | High Z | Power Down |
| OutputDisable | 0 | 1 | 1 | I_{CC1}, I_{CC2} | High Z | |
| Read | 0 | 0 | 1 | I_{CC1}, I_{CC2} | D_{OUT} | Read Cycle |
| Write | 0 | X | 0 | I_{CC1}, I_{CC2} | D_{IN} | Write Cycle |

1 = V_{IH} ,

0 = V_{IL} ,

X = Don't Care

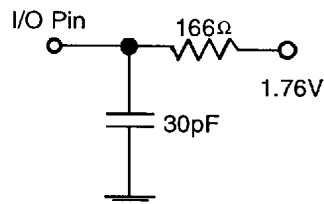
Low V_{CC} Data Retention Characteristics - L Version Only ($T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$)

| Parameter | Symbol | Test Condition | min | typ | max | Unit |
|--------------------------------------|-------------|--|----------------|-----|-----|---------------|
| V_{CC} for Data Retention | V_{DR} | $\overline{CS} \geq V_{CC} - 0.2\text{V}, V_{IN} \geq 0\text{V}$ | 2.0 | - | - | V |
| Data Retention Current | I_{CCDR1} | $V_{CC} = 3.0\text{V}, \overline{CS} \geq V_{CC} - 0.2\text{V}, V_{IN} \geq 0$ | - | - | 170 | μA |
| Chip Deselect to Data Retention Time | t_{CDR} | See Retention Waveform | 0 | - | - | ns |
| Operation Recovery Time | t_R | See Retention Waveform | $t_{RC}^{(1)}$ | - | - | ns |

Notes (1) t_{RC} = Read Cycle Time

AC Test Conditions

- * Input pulse levels: 0V to 3.0V
- * Input rise and fall times: 5ns
- * Input and Output timing reference levels: 1.5V
- * Output load: See Diagram
- * $V_{CC} = 5\text{V} \pm 10\%$



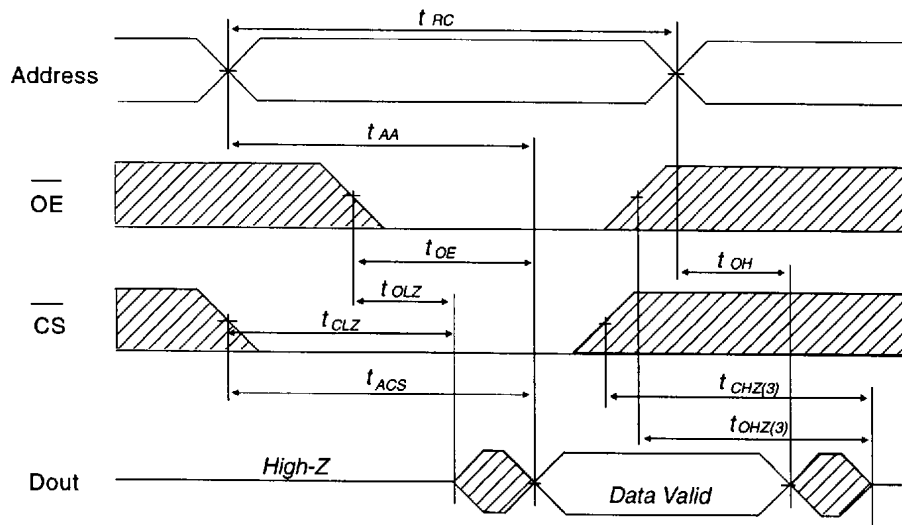
AC OPERATING CONDITIONS**Read Cycle**

| Parameter | Symbol | 55 | | 70 | | 85 | | 10 | | Unit |
|---|-----------|-----|-----|-----|-----|-----|-----|-----|-----|------|
| | | min | max | min | max | min | max | min | max | |
| Read Cycle Time | t_{RC} | 55 | - | 70 | - | 85 | - | 100 | - | ns |
| Address Access Time | t_{AA} | - | 55 | - | 70 | - | 85 | - | 100 | ns |
| Chip Select Access Time | t_{ACS} | - | 55 | - | 70 | - | 85 | - | 100 | ns |
| Output Enable to Output Valid | t_{OE} | - | 35 | - | 40 | - | 45 | - | 50 | ns |
| Output Hold from Address Change | t_{OH} | 5 | - | 5 | - | 5 | - | 10 | - | ns |
| Chip Selection to Output in Low Z | t_{CLZ} | 5 | - | 5 | - | 10 | - | 10 | - | ns |
| Output Enable to Output in Low Z | t_{OLZ} | 0 | - | 0 | - | 5 | - | 5 | - | ns |
| Chip Deselection to Output in High Z ⁽³⁾ | t_{CHZ} | 0 | 25 | 0 | 25 | 0 | 30 | 0 | 35 | ns |
| Output Disable to Output in High Z ⁽³⁾ | t_{OHZ} | 0 | 25 | 0 | 25 | 0 | 30 | 0 | 35 | ns |

Write Cycle

| Parameter | Symbol | 55 | | 70 | | 85 | | 10 | | Unit |
|------------------------------------|-----------|-----|-----|-----|-----|-----|-----|-----|-----|------|
| | | min | max | min | max | min | max | min | max | |
| Write Cycle Time | t_{WC} | 55 | - | 70 | - | 85 | - | 100 | - | ns |
| Chip Selection to End of Write | t_{CW} | 50 | - | 65 | - | 75 | - | 80 | - | ns |
| Address Valid to End of Write | t_{AW} | 50 | - | 65 | - | 75 | - | 80 | - | ns |
| Address Setup Time | t_{AS} | 0 | - | 0 | - | 0 | - | 0 | - | ns |
| Write Pulse Width | t_{WP} | 45 | - | 60 | - | 60 | - | 60 | - | ns |
| Write Recovery Time | t_{WR} | 0 | - | 0 | - | 0 | - | 0 | - | ns |
| Write to Output in High Z | t_{WHZ} | 0 | 30 | 0 | 30 | 0 | 30 | 0 | 35 | ns |
| Data to Write Time Overlap | t_{DW} | 35 | - | 40 | - | 40 | - | 40 | - | ns |
| Data Hold from Write Time | t_{DH} | 0 | - | 0 | - | 0 | - | 0 | - | ns |
| Output Disable to Output in High Z | t_{OHZ} | 0 | 25 | 0 | 25 | 0 | 30 | 0 | 35 | ns |
| Output Active from End of Write | t_{OW} | 5 | - | 5 | - | 5 | - | 5 | - | ns |

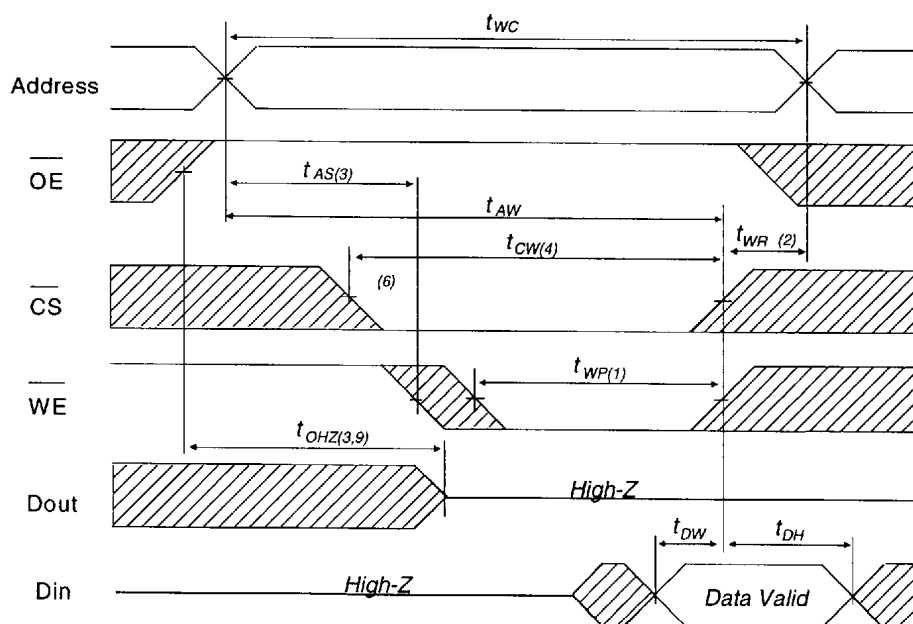
Read Cycle Timing Waveform (1,2)



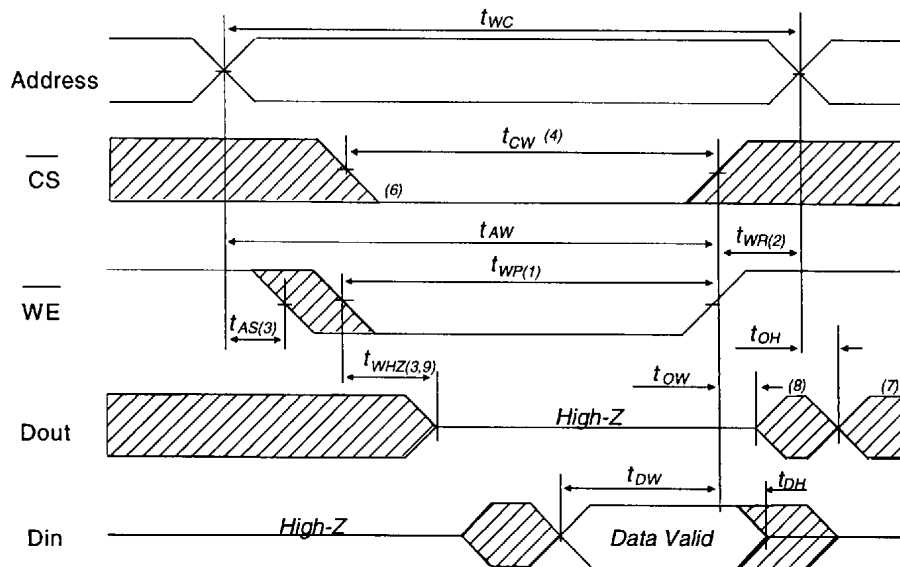
Notes:

- (1) During the Read Cycle, \overline{WE} is high.
- (2) Address valid prior to or coincident with \overline{CS} transition Low.
- (3) t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.

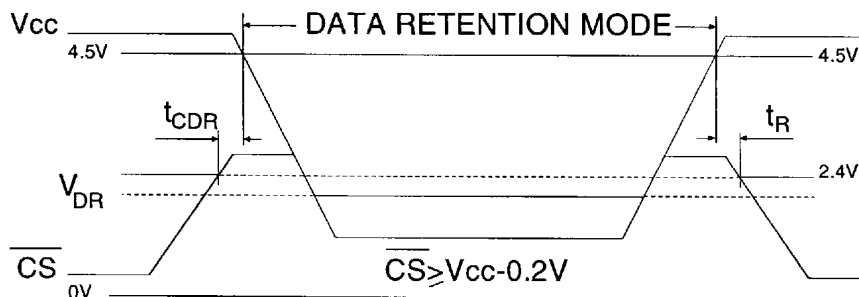
Write Cycle No.1 Timing Waveform



Write Cycle No.2 Timing Waveform ⁽⁵⁾



Data Retention Waveform

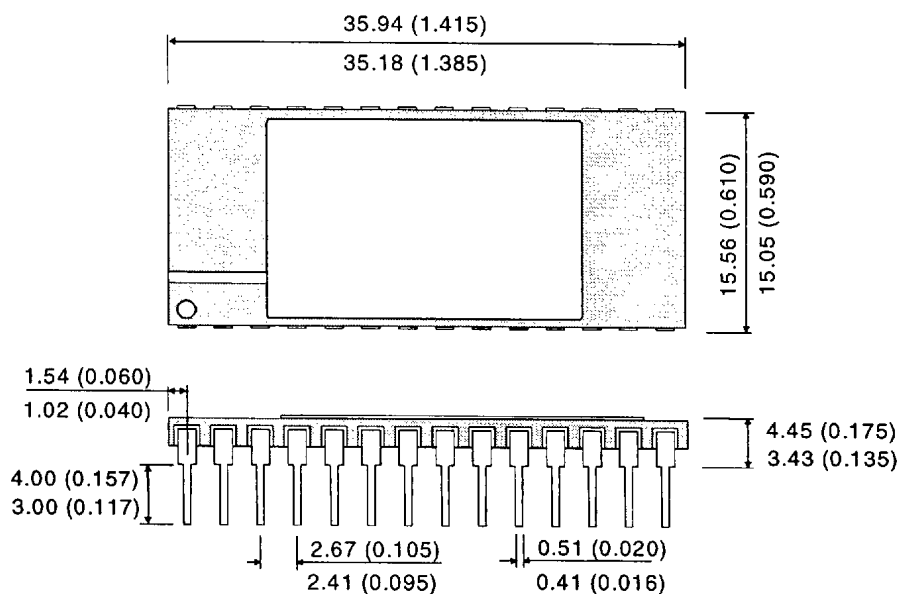


AC Characteristics Notes

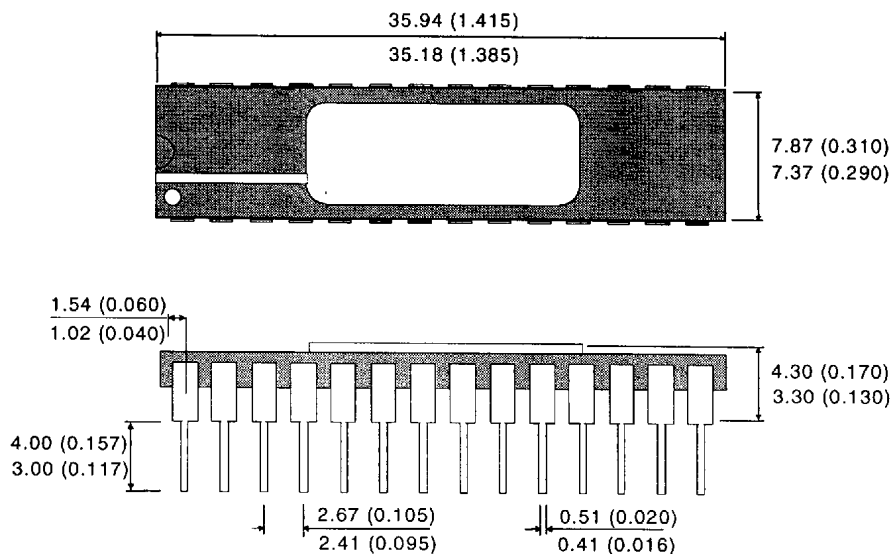
- (1) A write occurs during the overlap (t_{WP}) of a low \overline{CS} and a low \overline{WE} .
- (2) t_{WR} is measured from the earlier of \overline{CS} or \overline{WE} going high to the end of write cycle.
- (3) During this period, I/O pins are in the output state. Input signals out of phase must not be applied.
- (4) If the \overline{CS} low transition occurs simultaneously with the \overline{WE} low transition or after the \overline{WE} low transition, outputs remain in a high impedance state.
- (5) \overline{OE} is continuously low. ($\overline{OE} = V_{IL}$)
- (6) D_{OUT} is in the same phase as written data of this write cycle.
- (7) D_{OUT} is the read data of next address.
- (8) If \overline{CS} is low during this period, I/O pins are in the output state. Input signals out of phase must not be applied.
- (9) t_{WHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to

PACKAGE DETAILS Dimensions in mm (inches)

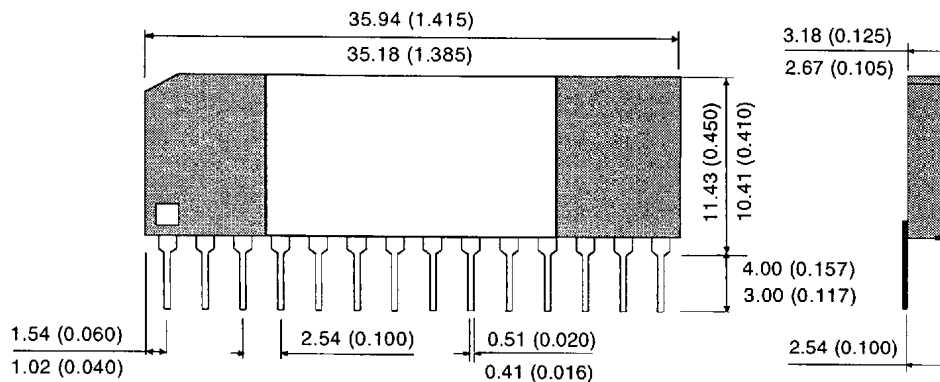
28 pin 0.6" Dual-In-Line (DIL) - 'S' Package



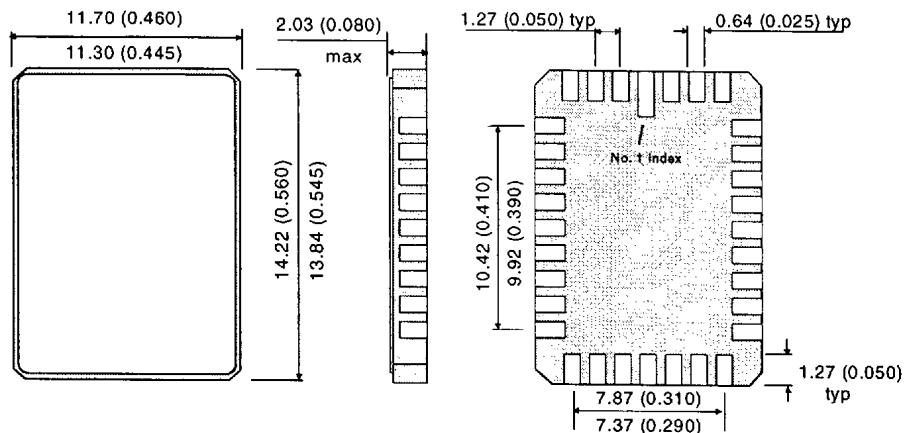
28 pin 0.3" Dual-In-Line (DIL) - 'T' Package



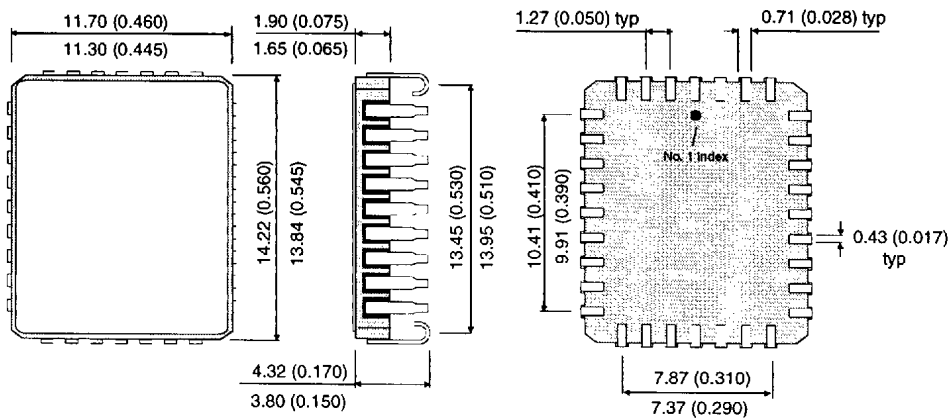
28 pin 0.1" Vertical-In-Line (VIL) - 'V' Package



32 pad Leadless Chip Carrier (LCC) - 'W' Package



32 pin J-Leaded Chip Carrier (JLCC) - 'J' Package



SCREENING

Military Screening Procedure

Component Screening Flow for high reliability parts in accordance with Mil-883 method 5004 is shown below:

| MB COMPONENT SCREENING FLOW | | |
|--|--|--------------|
| SCREEN | TEST METHOD | LEVEL |
| Visual and Mechanical | | |
| Internal visual | 2010 Condition B or manufacturers equivalent | 100% |
| Temperature cycle | 1010 Condition C (10 Cycles, -65°C to +150°C) | 100% |
| Constant acceleration | 2001 Condition E (Y, only) (30,000g) | 100% |
| Pre-Burn-in electrical | Per applicable device specifications at $T_A=+25^\circ\text{C}$ | 100% |
| Burn-in | Method 1015, Condition D, $T_A=+125^\circ\text{C}$, 160hrs min | 100% |
| Final Electrical Tests | Per applicable Device Specification | |
| Static (dc) | a) @ $T_A=+25^\circ\text{C}$ and power supply extremes b) @ temperature and power supply extremes | 100% 100% |
| Functional | a) @ $T_A=+25^\circ\text{C}$ and power supply extremes b) @ temperature and power supply extremes | 100% 100% |
| Switching (ac) | a) @ $T_A=+25^\circ\text{C}$ and power supply extremes b) @ temperature and power supply extremes | 100% 100% |
| Percent Defective allowable (PDA) | Calculated at post-burn-in at $T_A=+25^\circ\text{C}$ | 5% |
| Hermeticity | 1014 | |
| Fine | Condition A | 100% |
| Gross | Condition C | 100% |
| External Visual | 2009 Per vendor or customer specification | 100% |

ORDERING INFORMATION**MSM832SLMB-70**

| | |
|-----------------------|---|
| Speed | 55 = 55 ns 70 = 70 ns 85 = 85 ns 10 = 100 ns |
| Temp. range/screening | Blank = Commercial I = Industrial M = Military MB = May be screened in accordance with MIL-STD-883 |
| Standard/Low Power | Blank = Standard Power L = Low Power |
| Package | S = 28 pin 0.6" DIL T = 28 pin 0.3" DIL V = 28 pin 0.1" VIL W = 32 pad LCC J = 32 pin JLCC |
| Memory Organisation | 832 = 32K x 8 SRAM |