MOTOROLA

MCM5101
MCM51L01

256 × 4 BIT STATIC RAM

The MCM5101 family of CMOS RAMs offers ultra low power and fully static operation with a single 5-volt supply. The CMOS 1024-bit devices are organized in 256 words by 4 bits. Separate data inputs and data outputs permit maximum flexibility in bus-oriented systems. Data retention at a power supply as low as 2.0 volts over temperature readily allows design into applications using battery backup for nonvolatility. The MCM5101 is fully static and does not require clocking in standby mode.

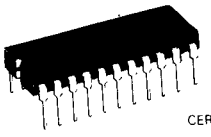
The MCM5101 is fabricated using the Motorola advanced ion-implanted, silicon-gate technology for high performance and high reliability.

- Low Standby Power
- Fast Access Time
- Single +5.0 Volt Supply
- Fully TTL Compatible — All Inputs and Outputs
- Three-State Output
- Fully Static Operation
- Data Retention to 2.0 Volts
- Direct Replacement for:
  - Intel 5101 Series
  - AMI S5101 Series
  - Hitachi HM435101 Series
- Pin Replacement for Harris HM6501 Series

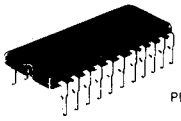
CMOS

(COMPLEMENTARY MOS)

1024-BIT STATIC RANDOM ACCESS MEMORY



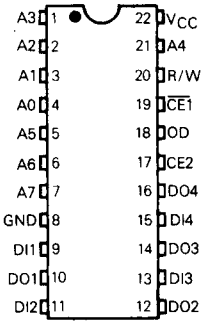
C SUFFIX
CERDIP PACKAGE
CASE 736



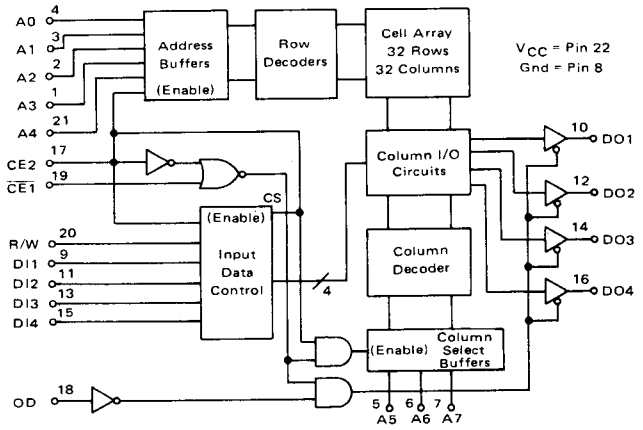
P SUFFIX
PLASTIC PACKAGE
CASE 708

Type Number	Typical Current @2 V (μA)	Typical Current @ 5 V (μA)	Max Access (ns)
MCM51L01C45, P45	0.14	0.2	450
MCM51L01C65, P65	0.14	0.2	650
MCM5101C65, P65	0.70	1.0	650
MCM5101C80, P80	–	10	800

PIN ASSIGNMENT



BLOCK DIAGRAM



TRUTH TABLE

$\overline{CE1}$	CE2	OD	R/W	D_{in}	Output	Mode
H	X	X	X	X	High-Z	Not Selected
X	L	X	X	X	High-Z	Not Selected
X	X	H	H	X	High-Z	Output Disabled
L	H	H	L	X	High-Z	Write
L	H	L	L	X	D_{in}	Write
L	H	L	H	X	D_{out}	Read

DS9628/9-80

MAXIMUM RATINGS (Voltages referenced to V_{SS} Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage on Any Pin	V_{in}	−0.3 to V_{CC}+0.3	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC} V_{SS}	4.75 0	5.0 0	5.25 0	V
Logic 1 Voltage, All Inputs	V_{IH}	2.2	–	V_{CC}+0.3	V
Logic 0 Voltage, All Inputs	V_{IL}	−0.3	–	0.65	V

DC CHRACTERISTICS

Characteristic	Symbol	MCM51L01-45 MCM51L01-65			MCM5101-65			MCM5101-80			Unit
		Min	Typ(1)	Max	Min	Typ(1)	Max	Min	Typ(1)	Max	
Input Current	I_{in}(2)	–	5.0	–	–	5.0	–	–	5.0	–	nA
Input High Voltage	V_{IH}	2.2	–	V_{CC}+0.3	2.2	–	V_{CC}+0.3	2.2	–	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.3	–	0.65	−0.3	–	0.65	−0.3	–	0.65	V
Output High Voltage (I_{OH} = −1.0 mA)	V_{OH}	2.4	–	–	2.4	–	–	2.4	–	–	V
Output Low Voltage (I_{OL} = 2.0 mA)	V_{OL}	–	–	0.4	–	–	0.4	–	–	0.4	V
Output Leakage Current ($\overline{CE1}$ = 2.2 V, V_{OL} = 0 V to V_{CC})	I_{LO}(2)	–	–	±1.0	–	–	±1.0	–	–	±2.0	μA
Operating Current (V_{in} = V_{CC}, except $\overline{CE1}$ ≤ 0.65 V, outputs open)	I_{CC1}	–	9.0	22	–	9.0	22	–	11	25	mA
Operating Current (V_{in} = 2.2 V, Except $\overline{CE1}$ ≤ 0.65 V, outputs open)	I_{CC2}	–	13	27	–	13	27	–	15	30	mA
Standby Current ($\overline{CE2}$ ≤ 0.2 V, V_{in} = 0 V or V_{CC})	I_{CCL}(2)(4)	–	–	10	–	–	200	–	–	500	μA

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V periodically sampled rather than 100% tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (V_{in} = 0 V)	C_{in}	4.0	8.0	pF
Output Capacitance (V_{out} = 0 V)	C_{out}	8.0	12.0	pF

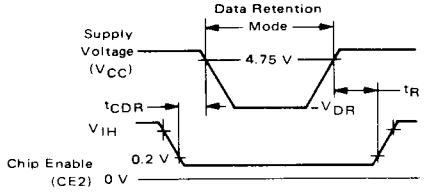
LOW V_{CC} DATA RETENTION CHARACTERISTICS (Excluding MCM5101-80)

Parameter	Test Conditions		Symbol	Min	Typ(1)	Max	Unit
V_{CC} for Data Retention			V_{DR}	2.0	–	–	V
MCM51L01-45, -65 Data Retention Current	$\overline{CE2}$ ≤ 0.2 V	V_{DR} = 2.0 V	I_{CCDR1}	–	0.14	10	μA
MCM5101-65 Data Retention Current		V_{DR} = 2.0 V	I_{CCDR2}	–	0.70	200	μA
Chip Deselect to Data Retention Time			t_{CDR}	0	–	–	ns
Operation Recover Time			t_R	t_{RC}(3)	–	–	ns

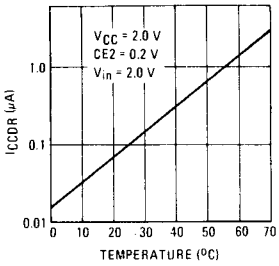
Notes:
1. Typical values are T_A = 25°C and nominal supply voltage
2. Current through all inputs and outputs included in I_{CCL} measurement
3. t_{RC} = Read Cycle Time
4. Low current state is for $\overline{CE2}$ = 0 only

SRAM

LOW V_{CC} DATA RETENTION WAVEFORM



TYPICAL I_{CCDR} vs TEMPERATURE



AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted)

Input Pulse Levels..... + 0.65 V to 2.2 V
Input Rise and Fall Times.....20 ns

Output Load..... 1 TTL Gate and C_L = 100 pF
Timing Measurement Reference Level.....1.5 V

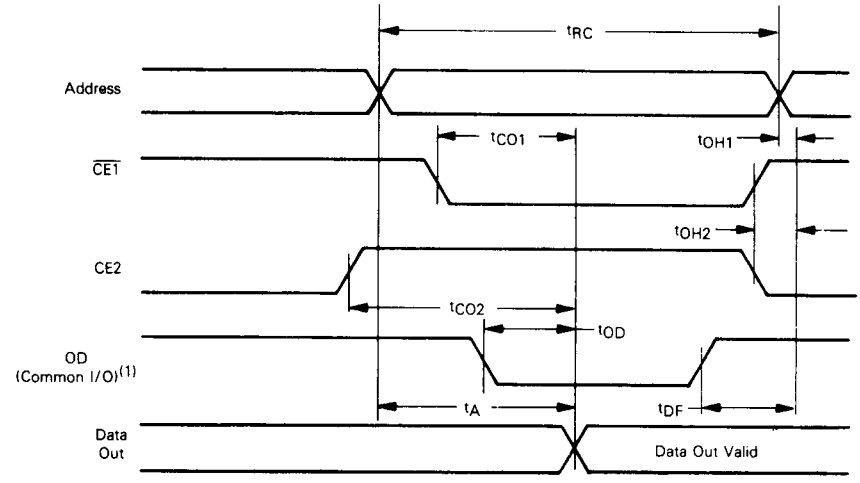
READ CYCLE

Parameter	Symbol	MCM51L01-45		MCM51L01-65 MCM5101-65		MCM5101-80		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle	t_{RC}	450	–	650	–	800	–	ns
Access Time	t_A	–	450	–	650	–	800	ns
Chip Enable ($\overline{CE1}$) to Output	t_{CO1}	–	400	–	600	–	800	ns
Chip Enable (CE2) to Output	t_{CO2}	–	500	–	700	–	850	ns
Output Disable to Output	t_{OD}	–	250	–	350	–	450	ns
Data Output to High-Z State	t_{DF}	0	130	0	150	0	200	ns
Previous Read Data Valid with Respect to Address Change	t_{OH1}	0	–	0	–	0	–	ns
Previous Read Data Valid with Respect to Chip Enable	t_{OH2}	0	–	0	–	0	–	ns

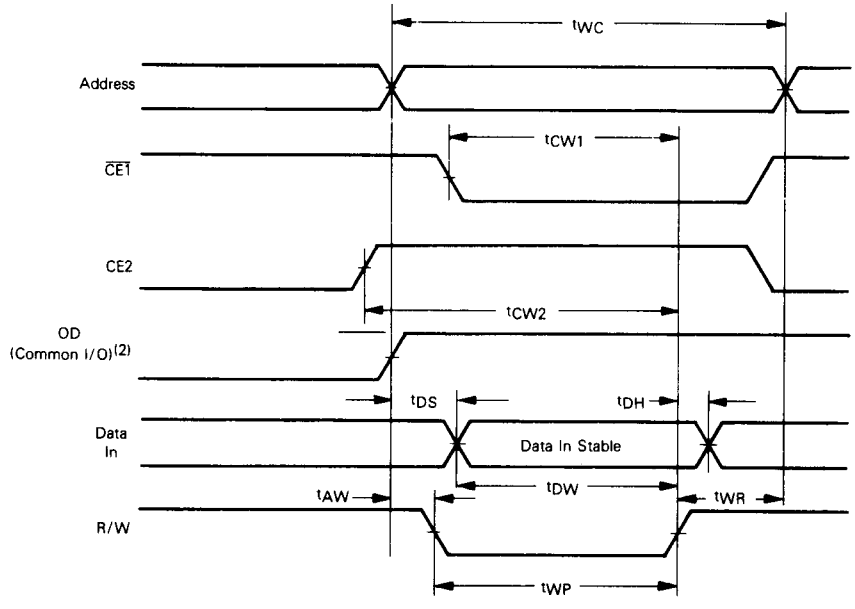
WRITE CYCLE

Parameter	Symbol	MCM51L01-45		MCM51L01-65 MCM5101-65		MCM5101-80		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle	t_{WC}	450	–	650	–	800	–	ns
Write Delay	t_{AW}	130	–	150	–	200	–	ns
Chip Enable ($\overline{CE1}$) to Write	t_{CW1}	350	–	550	–	650	–	ns
Chip Enable (CE2) to Write	t_{CW2}	350	–	550	–	650	–	ns
Data Setup	t_{DW}	250	–	400	–	450	–	ns
Data Hold	t_{DH}	50	–	100	–	100	–	ns
Write Pulse	t_{WP}	250	–	400	–	450	–	ns
Write Recovery	t_{WR}	50	–	50	–	100	–	ns
Output Disable Setup	t_{DS}	130	–	150	–	200	–	ns

READ CYCLE TIMING



WRITE CYCLE TIMING



Notes:
1. OD may be tied low for separate I/O operation
2. During the write cycle, OD is "high" for common I/O and "don't care" for separate I/O operation