



## MM5559 serial-to-parallel converter

### general description

The MM5559 serial-to-parallel converter provides 33 bits of conversion in a single package. A serial output facilitates cascading these devices to provide larger conversions.

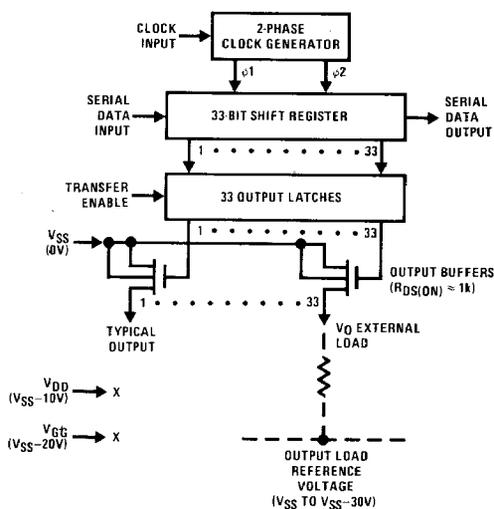
### features

- 33 Parallel outputs
- Serial output
- DC-to-250 kHz operation

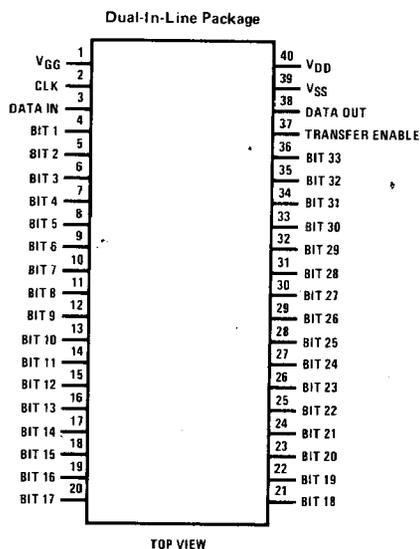
### applications

- Matrix displays and printers
- Musical instrument keyboard/tone generator interface controllers

### logic and connection diagrams



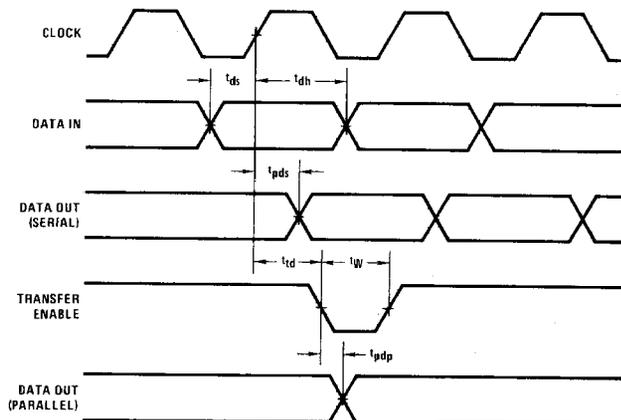
33-Bit Serial-to-Parallel Converter



TOP VIEW

Order Number MM5559N  
See Package 24

### timing diagram



**absolute maximum ratings**

Voltage At Any Pin

 $V_{SS} + 0.3$  to  $V_{SS} - 25V$ 

Storage Temperature

 $-55^{\circ}C$  to  $+100^{\circ}C$ 

Voltage At Any Output Pin

 $V_{SS} + 0.3$  to  $V_{SS} - 33V$ 

Lead Temperature (Soldering, 10 seconds)

 $300^{\circ}C$ 

Operating Temperature

 $0^{\circ}C$  to  $+70^{\circ}C$ **dc electrical characteristics**

$T_A$  within operating range,  $V_{SS} = 0V$ ,  $V_{DD} = -10V$ ,  $\pm 10\%$ ,  $V_{GG} = -20V \pm 10\%$ , output load reference voltage =  $0V$  to  $-30V$  (via external load resistor)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Voltages					
Logic High Level		$V_{SS}-2.2$		$V_{SS}$	V
Logic Low Level		$V_{SS}-11$		$V_{SS}-7$	V
Clock and Transfer Enable Input Voltages					
Logic High Level		$V_{SS}-1.0$		$V_{SS}$	V
Logic Low Level		$V_{SS}-11$		$V_{SS}-8.6$	V
Input Capacitance				7	pF
Input Leakage Current	$T_A = 25^{\circ}C$ , $V_{IN} = V_{SS}-11$			10	$\mu A$
Clock Input Frequency	Duty Cycle = 50%	0		250	kHz
Rise and Fall Times	$V_{SS}-2.2$ through $V_{SS}-8.6$			0.2	$\mu s$
Transfer Enable Input					
Pulse Width	Time at $V_{SS}-8.6$	1.6			$\mu s$
Rise and Fall Times				0.2	$\mu s$
Parallel Outputs					
Output Voltage	$I_O = 2$ mA	$V_{SS}-2$			V
Leakage Current	$T_A = 25^{\circ}C$ , $V_O = V_{SS}-30$ .			10	$\mu A$
Serial Output Voltages					
Logical High Level	Loaded $56$ k $\Omega$ to $V_{DD}$	$V_{SS}-2$		$V_{SS}$	V
Logical Low Level	Loaded $560$ k $\Omega$ to $V_{SS}$	$V_{DD}$		$V_{SS}-8$	V
Power Supply Currents					
Drain Supply, $I_{DD}$				10	mA
Gate Supply, $I_{GG}$	(Note 1)		7.5	20	mA

**Note 1:** The magnitude of  $I_{GG}$  is modulated by the parallel output data; the current is inversely proportional to the number of outputs that are high (sourcing current). The typical value of 7.5 mA is representative of an alternating 1's and 0's output pattern.

**ac electrical characteristics**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$t_{ds}$ Data Setup Time	Referenced from $V_{SS}-7$ on Data In to $V_{SS}-8.6$ on Clock In	0.4			$\mu s$
$t_{dh}$ Data Hold Time		0.2			$\mu s$
$t_{td}$ Transfer Delay	Referenced from $V_{SS}-8.6$	0.6			$\mu s$
$t_W$ Transfer Strobe Width		1.6			$\mu s$
Propagation Delay					
$t_{pds}$ Serial	High-to-Low ( $V_{SS}$ to $V_{DD}$ )	3.0			$\mu s$
	Low-to-High	1.2			$\mu s$
$t_{pdp}$ Parallel	Low-to-High with $10$ k $\Omega$ Load	1.2			$\mu s$