

OKI semiconductor

MSM51257AL

32,768-Word x 8-Bit CMOS STATIC RAM

GENERAL DESCRIPTION

The MSM51257AL is a 32768-word by 8-bit CMOS RAM static RAM featuring a 5V power supply operation and direct TTL input/output compatibility. Since the circuitry is completely static, external clock and refreshing operations are unnecessary, making this device very easy to use. The MSM51257AL is also a CMOS silicon gate device that requires very low power during standby (standby current of 100 μ A) when there is no chip selection.

The pins $\overline{CS}$ and $\overline{OE}$ are provided as control signals that permit the outputs to be tri-stated, allowing easy memory expansion on a system bus.

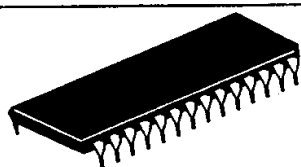
FEATURES

- Single 5V Supply
- 0°C ~ 70°C
- Low Power Dissipation
 - Standby: 0.55 mW MAX
 - Operation: 385 mW MAX (-10, -12)
 - 440 mW MAX (-70, -85)
- High Speed (Equal Access and Cycle Time)
 - 70-120 ns MAX
- Direct TTL Compatible (Input and Output)
- 3-State Output
- 28-pin DIP PKG
- 28-pin FLAT PKG

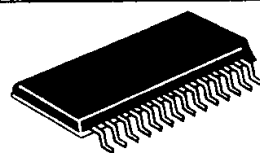
PIN CONFIGURATION (TOP VIEW)

MSM51257ALRS

MSM51257ALGS



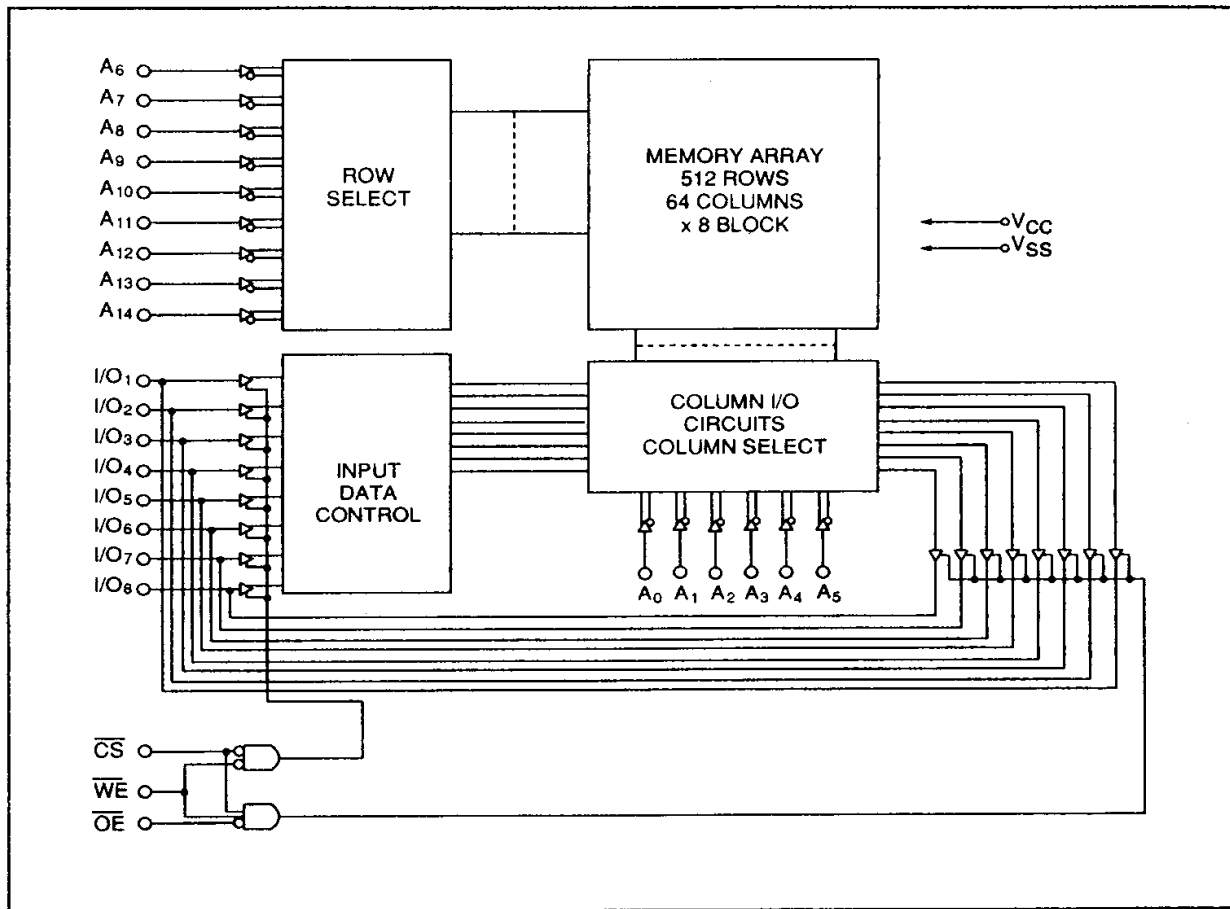
A14	1	28	VCC
A12	2	27	$\overline{WE}$
A7	3	26	A13
A6	4	25	A8
A5	5	24	A9
A4	6	23	A11
A3	7	22	$\overline{OE}$
A2	8	21	A10
A1	9	20	$\overline{CS}$
A0	10	19	I/O8
I/O1	11	18	I/O7
I/O2	12	17	I/O6
I/O3	13	16	I/O5
VSS	14	15	I/O4



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A3	7	22	$\overline{OE}$
A2	8	21	A10
A1	9	20	$\overline{CS}$
A0	10	19	I/O8
I/O1	11	18	I/O7
I/O2	12	17	I/O6
I/O3	13	16	I/O5
VSS	14	15	I/O4

Pin Names	Function
A ₀ ~ A ₁₄	Address inputs
I/O ₁ ~ I/O ₈	Data input/output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
Vcc, Vss	Supply voltage

FUNCTIONAL BLOCK DIAGRAM



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TRUTH TABLE

Mode	Pins	$\overline{\text{CS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Output
Standby		H	X	X	High Z
Read		L	H	H	High Z
		L	H	L	D _{OUT}
Write		L	L	X	D _{IN}

X: H or L

ELECTRICAL CHARACTERISTICS ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Conditions	Value	Unit
Supply Voltage	V _{CC}	Referenced to GND	-0.3~7.0	V
Input Voltage	V _{IN}		-0.3~V _{CC} +0.3	V
Operating Temperature	T _{opr}	—————	0~70	°C
Storage Temperature	T _{stg}	—————	-55~150	°C
Power Dissipation	P _D	T _a = 25°C	1.0	W

* Pulse width < 30 ns: -3.0V MIN

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Supply Voltage	V_{CC}	$5V \pm 10\%$	4.5	5	5.5	V
	V_{SS}	—	—	0	—	V
Data Retention Voltage	V_{CCH}	—	2	5	5.5	V
Input Voltage	V_{IH}	$5V \pm 10\%$	2.2	—	$V_{CC}+0.3$	V
	V_{IL}		-0.3*	—	0.8	V
Output Voltage	C_L	—	—	—	100	pF
	TTL		—	—	1	—

* Pulse width < 30 ns: -3.0V MIN

DC CHARACTERISTICS

($V_{CC} = 5V \pm 10\%$, $T_a = 0 \sim 70^\circ C$)

Parameter	Symbol	Conditions	MSM51257AL			Unit	Notes
			Min.	Typ.	Max.		
Input Leakage Current	I_{LI}	$V_{IN} = 0 \sim V_{CC}$	-1	—	1	μA	
Output Leakage Current	I_{LO}	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ $V_{IO} = 0 \sim V_{CC}$	-1	—	1	μA	
Output Voltage	V_{OH}	$I_{OH} = -1mA$	2.4	—	—	V	
	V_{OL}	$I_{OL} = 2.1mA$	—	—	0.4	V	
Standby Supply Current	I_{CCS}	$\overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} = 0 \sim V_{CC}$	—	2	100*	μA	
	I_{CCS1}	$\overline{CS} = V_{IH}$	—	—	3	mA	
Operating Supply Current	I_{CCA}	Min cycle, $I_{OUT} = 0mA$	—	—	①	mA	

* $T_a = 0$ to $40^\circ C$: 30 μA MAX

① 51257AL-70/85 80 mA 51257AL-10/12 70 mA

AC CHARACTERISTICS

Test Condition

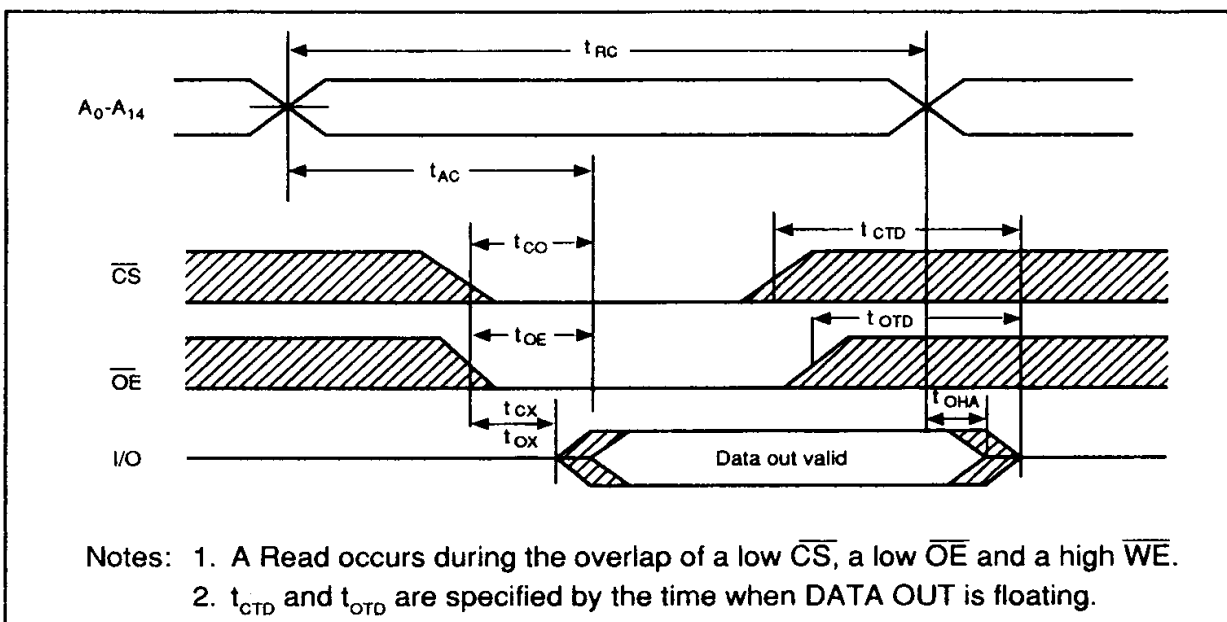
Parameter	Conditions
Input Pulse Level	$V_{IH} = 2.4V$, $V_{IL} = 0.6V$
Input Rise and Fall Times	5 ns
Input and Output	1.5V
Output Load	$C_L = 100pF$, 1TTL Gate

READ CYCLE

($V_{CC} = 5V \pm 10\%$, $T_a = 0 \sim +70^\circ C$)

Parameter	Symbol	MSM51257AL-70		MSM51257AL-85		MSM51257AL-10		MSM51257AL-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	70	—	85	—	100	—	120	—	ns
Address Access Time	t_{AC}	—	70	—	85	—	100	—	120	ns
Chip Enable Access Time	t_{CO}	—	70	—	85	—	100	—	120	ns
Output Enable to Output Valid	t_{OE}	—	40	—	45	—	50	—	60	ns
Chip Selection to Output Active	t_{CX}	10	—	10	—	10	—	10	—	ns
Output Hold Time from Address Change	t_{OHA}	5	—	5	—	10	—	10	—	ns
Output 3-State from Output Disable	t_{OTD}	—	30	—	30	—	35	—	35	ns
Output 3-State from Chip Deselection	t_{CTD}	—	30	—	30	—	35	—	35	ns
Output Enable to Output Active	t_{OX}	5	—	5	—	5	—	5	—	ns

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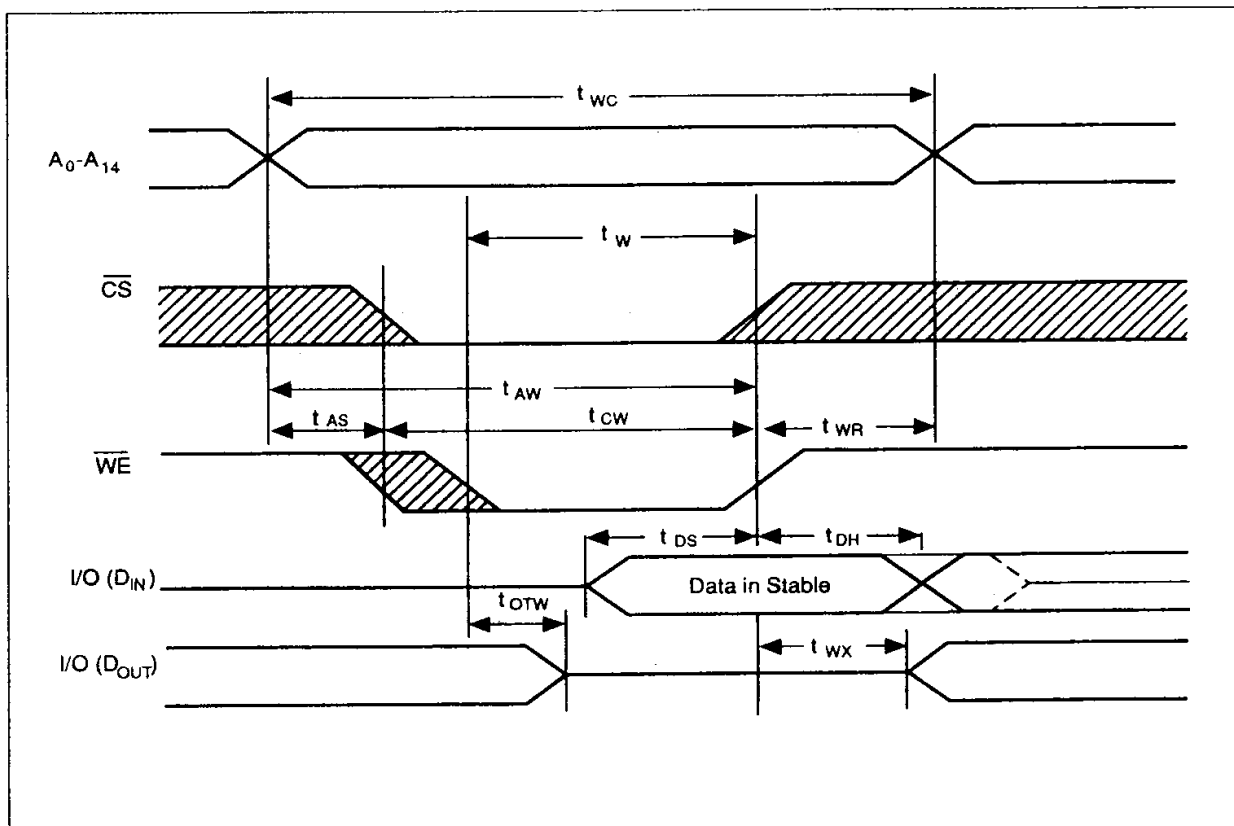


WRITE CYCLE

(V_{CC} = 5 V ±10%, T_a = 0 ~ +70°C)

Parameter	Symbol	MSM51257AL-70		MSM51257AL-85		MSM51257AL-10		MSM51257AL-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t _{WC}	70	—	85	—	100	—	120	—	ns
Address to Write Setup Time	t _{AS}	0	—	0	—	0	—	0	—	ns
Write Time	t _W	55	—	70	—	75	—	90	—	ns
Write Recovery Time	t _{WR}	5	—	5	—	5	—	5	—	ns
Data Setup Time	t _{DS}	35	—	40	—	40	—	50	—	ns
Data Hold from Write Time	t _{DH}	0	—	0	—	0	—	0	—	ns
Output 3-State from Write	t _{OTW}	0	30	0	30	0	35	0	35	ns
Chip Selection to End of Write	t _{CW}	65	—	75	—	90	—	100	—	ns
Address Valid to End of Write	t _{AW}	65	—	75	—	90	—	100	—	ns
Output Active from End of Write	t _{WX}	5	—	5	—	5	—	5	—	ns

- Notes
1. A Write Cycle occurs during the overlap of a low $\overline{CS}$, and a low $\overline{WE}$.
 2. $\overline{OE}$ can be both high and low in a Write Cycle.
 3. t_{AS} is specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs last.
 4. t_W is an overlap time of a low $\overline{CS}$, and a low $\overline{WE}$.
 5. t_{WR}, t_{DS}, and t_{DH} are specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs first.
 6. t_{OTW} is specified by the time when DATA OUT is floating, not defined by output level.
 7. When I/O pins are Data output mode, don't force inverse signals to those pins.



LOW V_{CC} DATA RETENTION CHARACTERISTICS

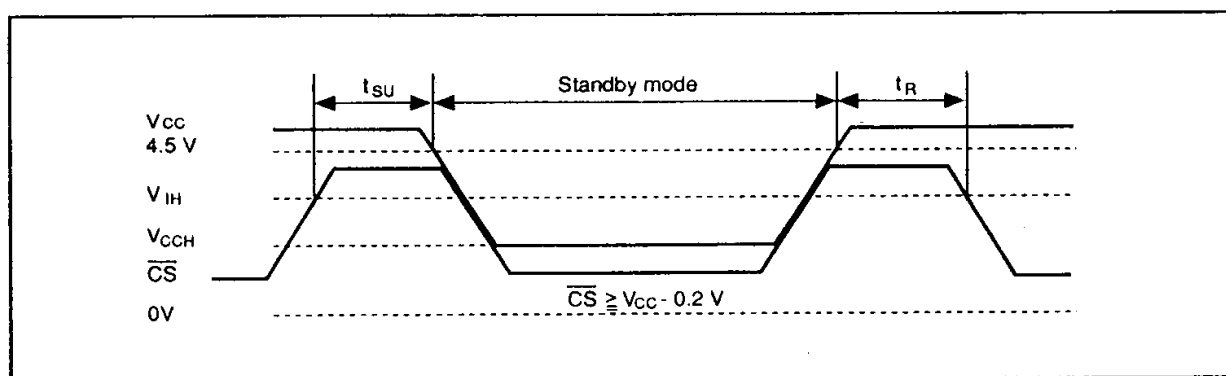
($T_a = 0 \sim +70^{\circ}\text{C}$, unless otherwise noted)

Parameter	Symbol	Conditions	Specified Value			Unit
			Min.	Typ.	Max.	
V_{CC} for Data Retention	V_{CCH}	$\overline{CS} \geq V_{CC} - 0.2\text{ V}$	2.0	—	5.5	V
Data Retention Current	I_{CCH}	$V_{CC} = 3\text{ V}$, $\overline{CS} \geq V_{CC} - 0.2\text{ V}$	—	1	50*	μA
CS to Data Retention Time	t_{SU}	—	0	—	—	ns
Operation Recovery Time	t_R	—	** t_{RC}	—	—	ns

* $T_a = 0$ to 40°C : $15\text{ }\mu\text{A}$ Max.

** t_{RC} = Read Cycle Time

$\overline{CS}$ CONTROL



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CAPACITANCE

($T_a = 25^{\circ}\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Conditions	Value		Unit
			Min.	Max.	
I/O Capacitance	$C_{I/O}$	—	—	10	pF
Input Capacitance	C_{IN}	—	—	10	pF

Note: This parameter is periodically sampled and not 100% tested.