OKI Semiconductor

MSM512805C

262,144-Word × 8-Bit DYNAMIC RAM : FAST PAGE MODE TYPE WITH EDO

DESCRIPTION

The MSM512805C is a 262,144-word × 8-bit dynamic RAM fabricated in Oki's silicon-gate CMOS technology. The MSM512805C achieves high integration, high-speed operation, and low-power consumption because Oki manufactures the device in a quadruple-layer polysilicon/single-layer metal CMOS process. The MSM512805C is available in a 26/24-pin plastic SOJ or 26/24-pin plastic TSOP.
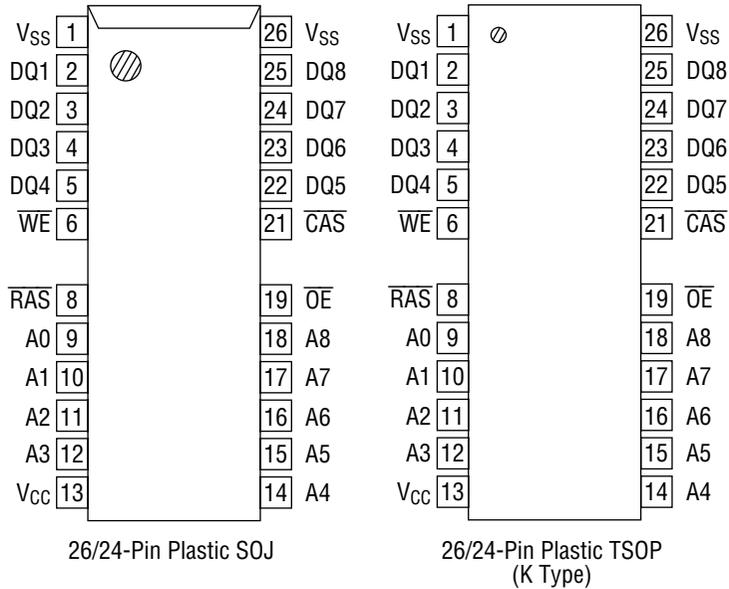
FEATURES

- 262,144-word × 8-bit configuration
- Single 5 V power supply, ±5% tolerance
- Input   : TTL compatible, low input capacitance
- Output   : TTL compatible, 3-state
- Refresh : 512 cycles/8 ms
- Fast page mode with EDO, read modify write capability
- $\overline{CAS}$ before $\overline{RAS}$ refresh, hidden refresh, $\overline{RAS}$-only refresh capability
- Package options:
  26/24-pin 300 mil plastic SOJ   (SOJ26/24-P-300-1.27)   (Product : MSM512805C-xxJS)
  26/24-pin 300 mil plastic TSOP (TSOPII26/24-P-300-1.27-K) (Product : MSM512805C-xxTS-K)
                                                              xx indicates speed rank.

PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}	t_{OEA}		Operating (Max.)	Standby (Max.)
MSM512805C-40	40 ns	20 ns	10 ns	10 ns	80 ns	735 mW	
MSM512805C-45	45 ns	24 ns	14 ns	14 ns	90 ns	682.5 mW	5.25 mW
MSM512805C-50	50 ns	26 ns	14 ns	14 ns	100 ns	630 mW	

PIN CONFIGURATION (TOP VIEW)

Vss	1		26	Vss
DQ1	2		25	DQ8
DQ2	3		24	DQ7
DQ3	4		23	DQ6
DQ4	5		22	DQ5
WE	6		21	CAS
RAS	8		19	OE
A0	9		18	A8
A1	10		17	A7
A2	11		16	A6
A3	12		15	A5
Vcc	13		14	A4

26/24-Pin Plastic SOJ

Vss	1		26	Vss
DQ1	2		25	DQ8
DQ2	3		24	DQ7
DQ3	4		23	DQ6
DQ4	5		22	DQ5
WE	6		21	CAS
RAS	8		19	OE
A0	9		18	A8
A1	10		17	A7
A2	11		16	A6
A3	12		15	A5
Vcc	13		14	A4

26/24-Pin Plastic TSOP
(K Type)

Pin Name	Function
A0 - A8	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
DQ1 - DQ8	Data Input/Data Output
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply (5 V)
V_{SS}	Ground (0 V)

Note: The same GND voltage level must be provided to every V_{SS} pin.

BLOCK DIAGRAM
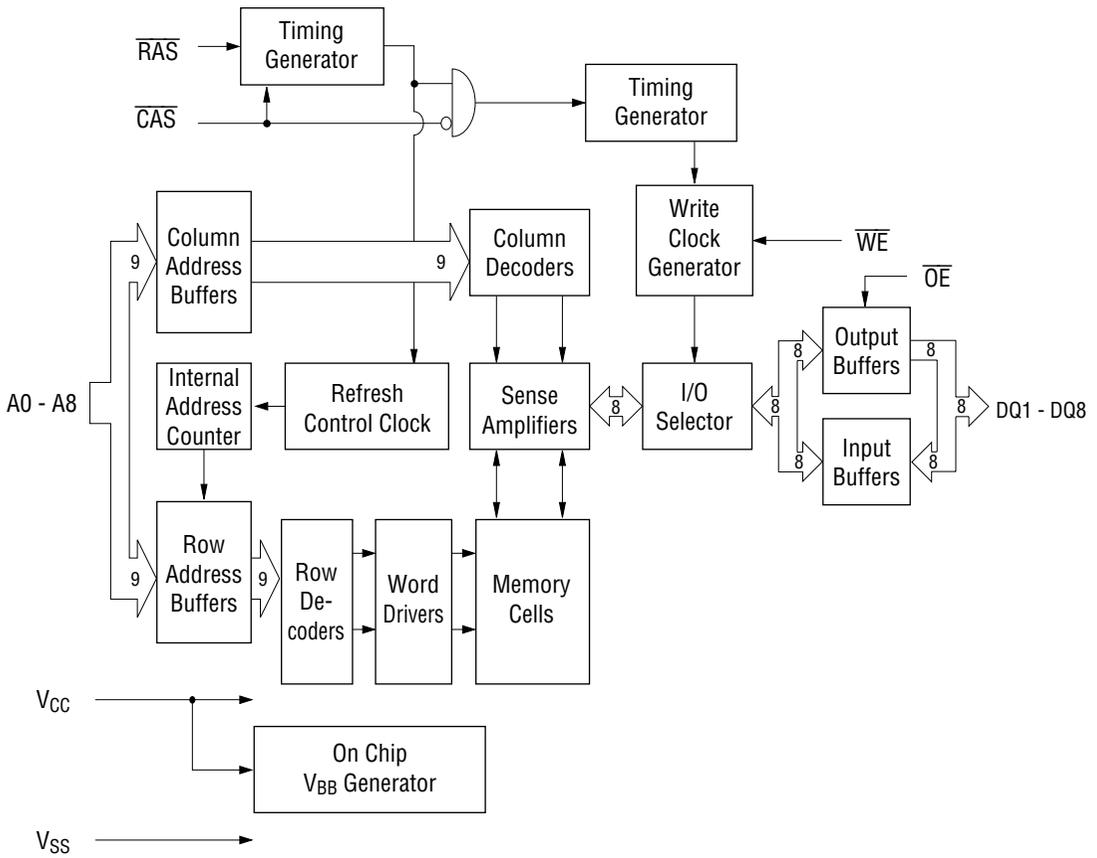
ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−1.0 to 7.0	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_D*	1	W
Operating Temperature	T_{opr}	0 to 70	°C
Storage Temperature	T_{stg}	−55 to 150	°C

*: Ta = 25°C

Recommended Operating Conditions

(Ta = 0°C to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	6.5	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

Capacitance

(V_{CC} = 5 V ±5%, Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A8)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ1 - DQ8)	$C_{I/O}$	—	7	pF

DC Characteristics

$(V_{CC} = 5 \text{ V} \pm 5\%, \text{Ta} = 0°\text{C to } 70°\text{C})$

Parameter	Symbol	Condition	MSM512805 C-40		MSM512805 C-45		MSM512805 C-50		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	V_{OH}	$I_{OH} = -5.0$ mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	$I_{OL} = 4.2$ mA	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	I_{LI}	$0 \text{ V} \leq V_I \leq 6.5 \text{ V}$; All other pins not under test = 0 V	−10	10	−10	10	−10	10	μA	
Output Leakage Current	I_{LO}	DQ disable $0 \text{ V} \leq V_O \leq 5.25 \text{ V}$	−10	10	−10	10	−10	10	μA	
Average Power Supply Current (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = Min.	—	140	—	130	—	120	mA	1, 2
Power Supply Current (Standby)	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	—	2	—	2	—	2	mA	1
		$\overline{RAS}$, $\overline{CAS}$ $\geq V_{CC} -0.2$ V	—	1	—	1	—	1		
Average Power Supply Current ($\overline{RAS}$-only Refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = Min.	—	140	—	130	—	120	mA	1, 2
Power Supply Current (Standby)	I_{CC5}	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, DQ = enable	—	5	—	5	—	5	mA	1
Average Power Supply Current ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	I_{CC6}	$\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$	—	140	—	130	—	120	mA	1, 2
Average Power Supply Current (Fast Page Mode)	I_{CC7}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{HPC} = Min.	—	110	—	100	—	90	mA	1, 3

Notes :   1. I_{CC} Max. is specified as I_{CC} for output open condition.
2. The address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. The address can be changed once or less while $\overline{CAS}$ = V_{IH}.

AC Characteristics (1/2)

(V$_{CC}$ = 5 V ±5%, Ta = 0°C to 70°C, Input Pulse Levels 0 V to 3 V) Note 1, 2, 3

| Parameter	Symbol	MSM512805 C-40		MSM512805 C-45		MSM512805 C-50		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t$_{RC}$	80	—	90	—	100	—	ns	
Read Modify Write Cycle Time	t$_{RWC}$	130	—	140	—	150	—	ns	
Fast Page Mode Cycle Time	t$_{HPC}$	20	—	20	—	20	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t$_{HPRWC}$	70	—	75	—	77	—	ns	
Access Time from $\overline{RAS}$	t$_{RAC}$	—	40	—	45	—	50	ns	4, 5, 6
Access Time from $\overline{CAS}$	t$_{CAC}$	—	10	—	14	—	14	ns	4, 5
Access Time from Column Address	t$_{AA}$	—	20	—	24	—	26	ns	4, 6
Access Time from $\overline{CAS}$ Precharge	t$_{CPA}$	—	25	—	28	—	30	ns	4
Access Time from $\overline{OE}$	t$_{OEA}$	—	10	—	14	—	14	ns	4
Output Low Impedance Time from $\overline{CAS}$	t$_{CLZ}$	0	—	0	—	0	—	ns	4
Data Output Hold After $\overline{CAS}$ Low	t$_{DOH}$	5	—	5	—	5	—	ns	
$\overline{CAS}$ to Data Output Buffer Turn-off Delay Time	t$_{CEZ}$	0	12	0	12	0	12	ns	7, 8
$\overline{RAS}$ to Data Output Buffer Turn-off Delay Time	t$_{REZ}$	0	12	0	12	0	12	ns	7, 8
$\overline{OE}$ to Data Output Buffer Turn-off Delay Time	t$_{OEZ}$	0	12	0	12	0	13	ns	7
$\overline{WE}$ to Data Output Buffer Turn-off Delay Time	t$_{WEZ}$	0	12	0	12	0	13	ns	7
Transition Time	t$_{T}$	2	50	2	50	2	50	ns	3
Refresh Period	t$_{REF}$	—	8	—	8	—	8	ms	
$\overline{RAS}$ Precharge Time	t$_{RP}$	30	—	35	—	40	—	ns	
$\overline{RAS}$ Pulse Width	t$_{RAS}$	40	10,000	45	10,000	50	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode with EDO)	t$_{RASP}$	40	100,000	45	100,000	50	100,000	ns	
$\overline{RAS}$ Hold Time	t$_{RSH}$	10	—	14	—	14	—	ns	
$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	t$_{ROH}$	10	—	10	—	10	—	ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode with EDO)	t$_{CP}$	10	—	10	—	10	—	ns	
$\overline{CAS}$ Pulse Width	t$_{CAS}$	10	10,000	10	10,000	10	10,000	ns	
$\overline{CAS}$ Hold Time	t$_{CSH}$	40	—	45	—	50	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t$_{CRP}$	5	—	5	—	5	—	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t$_{RHCP}$	25	—	28	—	30	—	ns	
$\overline{OE}$ Hold Time from $\overline{CAS}$ (DQ Disable)	t$_{CHO}$	5	—	5	—	5	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t$_{RCD}$	15	30	17	31	18	36	ns	5
$\overline{RAS}$ to Column Address Delay Time	t$_{RAD}$	10	20	12	21	13	24	ns	6
$\overline{RAS}$ to Second $\overline{CAS}$ Delay Time	t$_{RSCD}$	40	—	45	—	50	—	ns	
Row Address Set-up Time	t$_{ASR}$	0	—	0	—	0	—	ns	
Row Address Hold Time	t$_{RAH}$	5	—	7	—	8	—	ns	
Column Address Set-up Time	t$_{ASC}$	0	—	0	—	0	—	ns	
Column Address Hold Time	t$_{CAH}$	10	—	12	—	13	—	ns	
Column Address Hold Time from $\overline{RAS}$	t$_{AR}$	30	—	35	—	40	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t$_{RAL}$	20	—	24	—	26	—	ns	

AC Characteristics (2/2)

(V$_{CC}$ = 5 V ±5%, Ta = 0°C to 70°C, Input Pulse Levels 0 V to 3 V) Note 1, 2, 3

Parameter	Symbol	MSM512805 C-40		MSM512805 C-45		MSM512805 C-50		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Read Command Set-up Time	t$_{RCS}$	0	—	0	—	0	—	ns	
Read Command Hold Time	t$_{RCH}$	0	—	0	—	0	—	ns	9
Read Command Hold Time referenced to $\overline{RAS}$	t$_{RRH}$	0	—	0	—	0	—	ns	9
Write Command Set-up Time	t$_{WCS}$	0	—	0	—	0	—	ns	10
Write Command Hold Time	t$_{WCH}$	10	—	12	—	13	—	ns	
Write Command Hold Time from $\overline{RAS}$	t$_{WCR}$	30	—	35	—	40	—	ns	
Write Command Pulse Width	t$_{WP}$	10	—	10	—	10	—	ns	
$\overline{WE}$ Pulse Width (DQ Disable)	t$_{WPE}$	5	—	5	—	5	—	ns	
$\overline{OE}$ Command Hold Time	t$_{OEH}$	10	—	12	—	13	—	ns	
$\overline{OE}$ Precharge Time	t$_{OEP}$	7	—	7	—	7	—	ns	
$\overline{OE}$ Command Hold Time	t$_{OCH}$	7	—	7	—	7	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t$_{RWL}$	10	—	14	—	14	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t$_{CWL}$	10	—	14	—	14	—	ns	
Data-in Set-up Time	t$_{DS}$	0	—	0	—	0	—	ns	11
Data-in Hold Time	t$_{DH}$	10	—	12	—	13	—	ns	11
Data-in Hold Time from $\overline{RAS}$	t$_{DHR}$	30	—	35	—	40	—	ns	
$\overline{OE}$ to Data-in Delay Time	t$_{OED}$	10	—	12	—	13	—	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t$_{CWD}$	30	—	36	—	38	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t$_{AWD}$	40	—	48	—	52	—	ns	10
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t$_{RWD}$	60	—	70	—	75	—	ns	10
$\overline{CAS}$ Precharge $\overline{WE}$ Delay Time	t$_{CPWD}$	45	—	46	—	50	—	ns	10
$\overline{CAS}$ Active Delay Time from $\overline{RAS}$ Precharge	t$_{RPC}$	0	—	0	—	0	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$)	t$_{CSR}$	10	—	10	—	10	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$)	t$_{CHR}$	20	—	25	—	25	—	ns	

Notes: 1. A start-up delay of $200\,\mu s$ is required after power-up, followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh or $\overline{CAS}$ before $\overline{RAS}$ refresh) before proper device operation is achieved.

         2. The AC characteristics assume $t_T = 5$ ns.

         3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring input timing signals. Transition times (t_T) are measured between V_{IH} and V_{IL}.

         4. This parameter is measured with a load circuit equivalent to 2 TTL loads and 50 pF.

         5. Operation within the t_{RCD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then the access time is controlled by t_{CAC}.

         6. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, then the access time is controlled by t_{AA}.

         7. t_{CEZ} (Max.), t_{REZ} (Max.), t_{WEZ} (Max.) and t_{OEZ} (Max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.

         8. t_{CEZ} and t_{REZ} must be satisfied for open circuit condition.

         9. t_{RCH} or t_{RRH} must be satisfied for a read cycle.

       10. t_{WCS}, t_{CWD}, t_{RWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (Min.), then the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (Min.) , $t_{RWD} \geq t_{RWD}$ (Min.), $t_{AWD} \geq t_{AWD}$ (Min.) and $t_{CPWD} \geq t_{CPWD}$ (Min.), then the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, then the condition of the data out (at access time) is indeterminate.

       11. These parameters are referenced to the $\overline{CAS}$ leading edge in an early write cycle, and to the $\overline{WE}$ leading edge in an $\overline{OE}$ control write cycle, or a read modify write cycle.
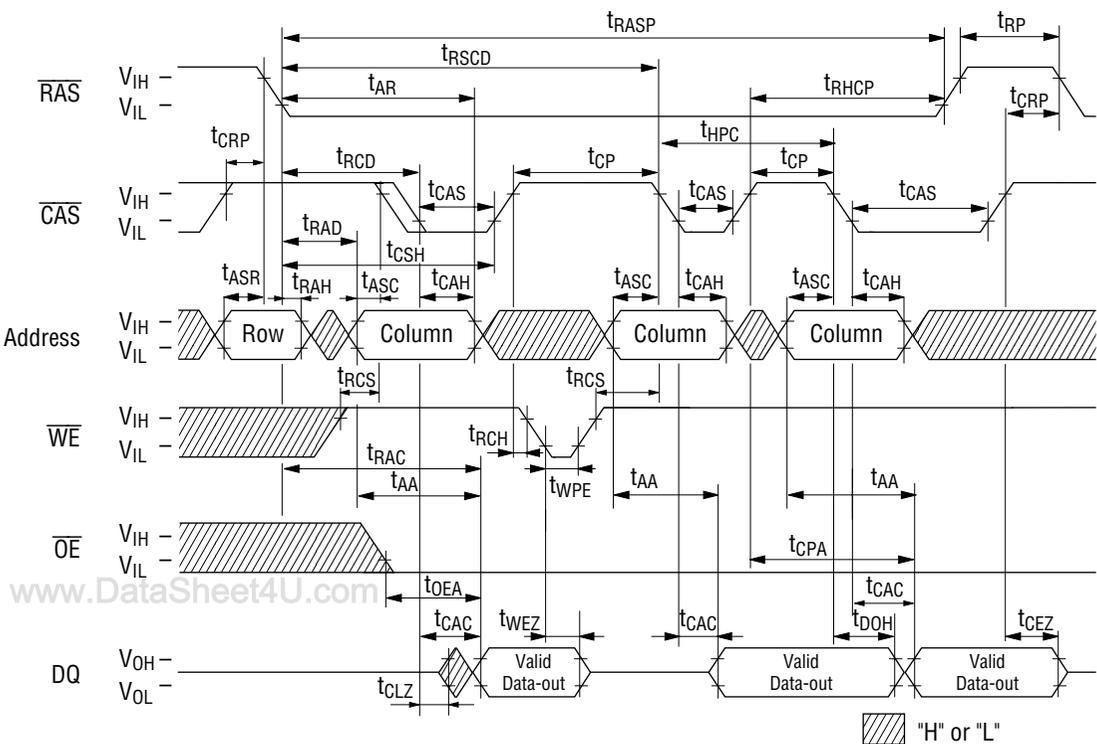
OKI Semiconductor   MSM512805C

TIMING WAVEFORM

Read Cycle

Write Cycle (Early Write)

Read Modify Write Cycle
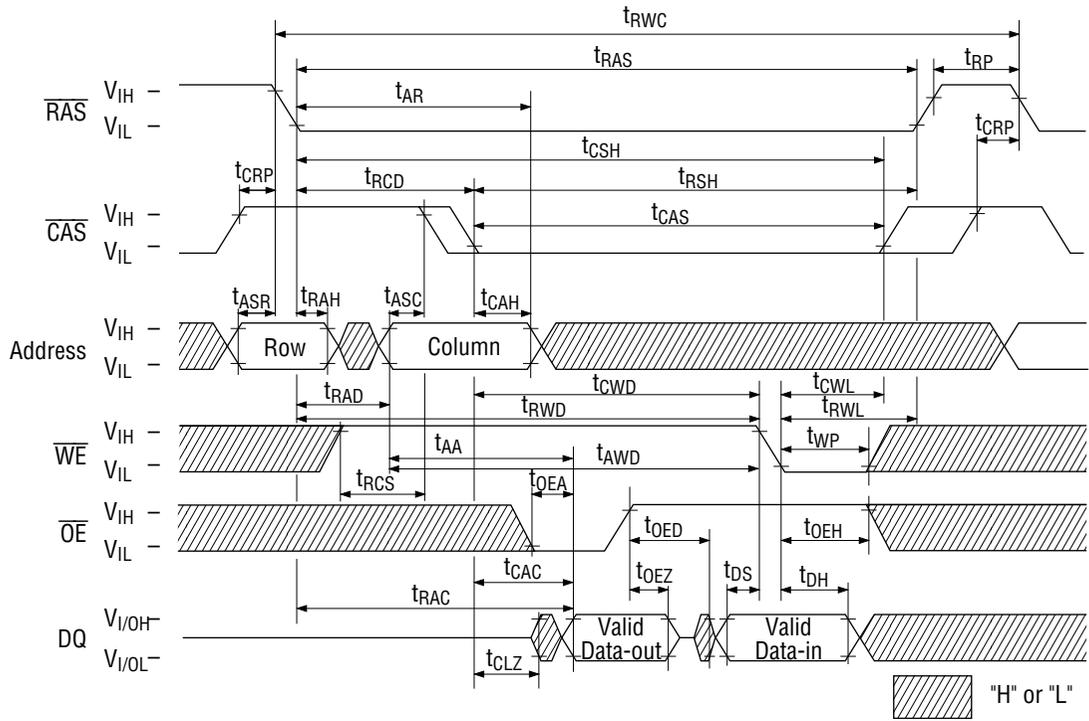
Fast Page Mode Read Cycle (Part-1)

* : Same Data, ▨ "H" or "L"
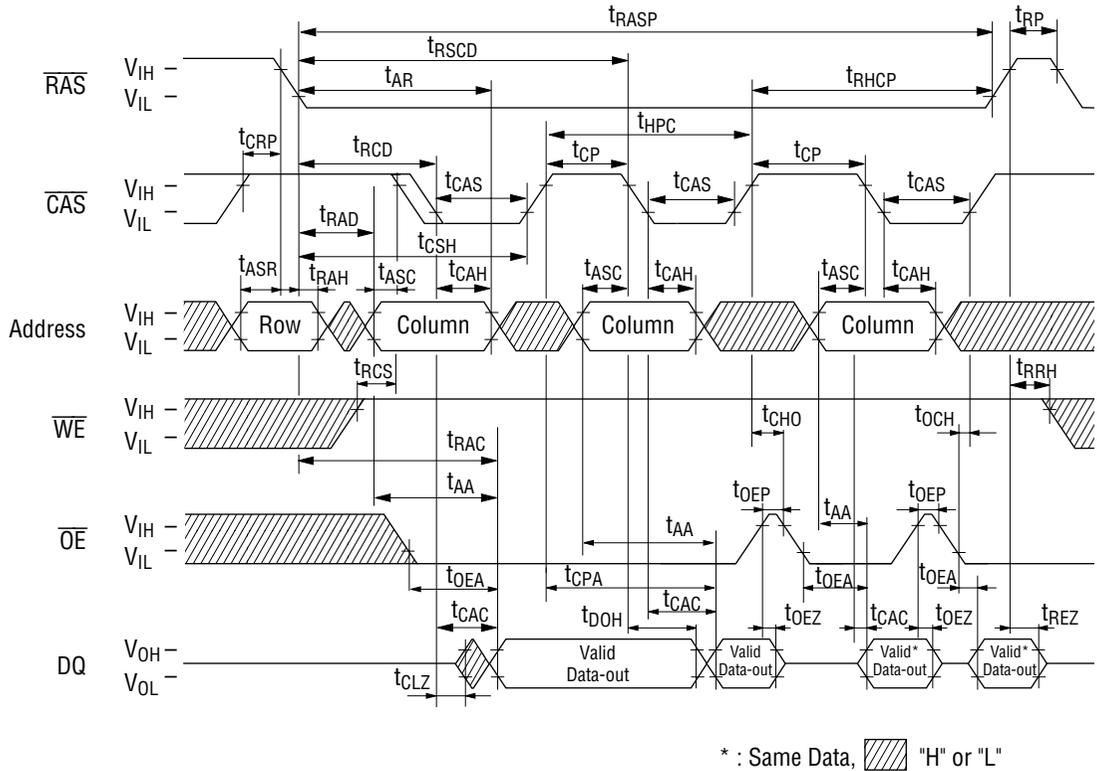
Fast Page Mode Read Cycle (Part-2)

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▨ "H" or "L"

Fast Page Mode Write Cycle (Early Write)

Fast Page Mode Read Modify Write Cycle

$\overline{\text{RAS}}$-Only Refresh Cycle

Note: $\overline{\text{WE}}$, $\overline{\text{OE}}$ = "H" or "L"   "H" or "L"

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle

Note: $\overline{\text{WE}}$, $\overline{\text{OE}}$, Address = "H" or "L"

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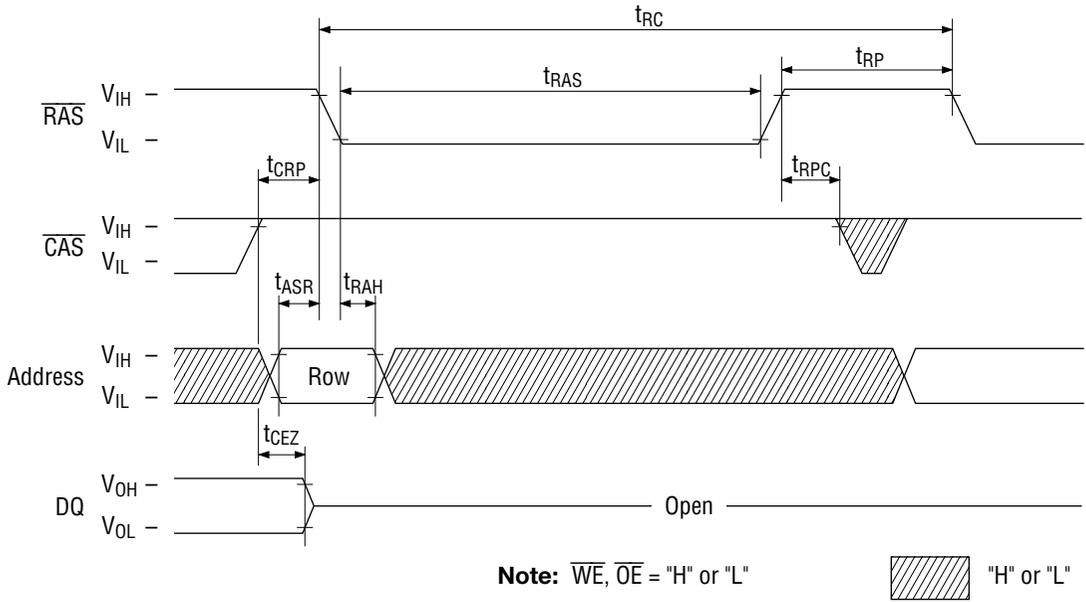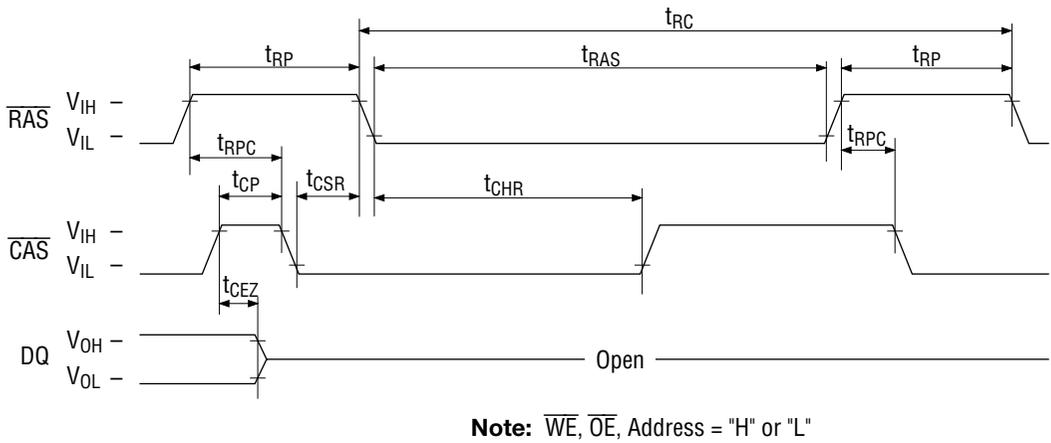
Hidden Refresh Read Cycle

"H" or "L"
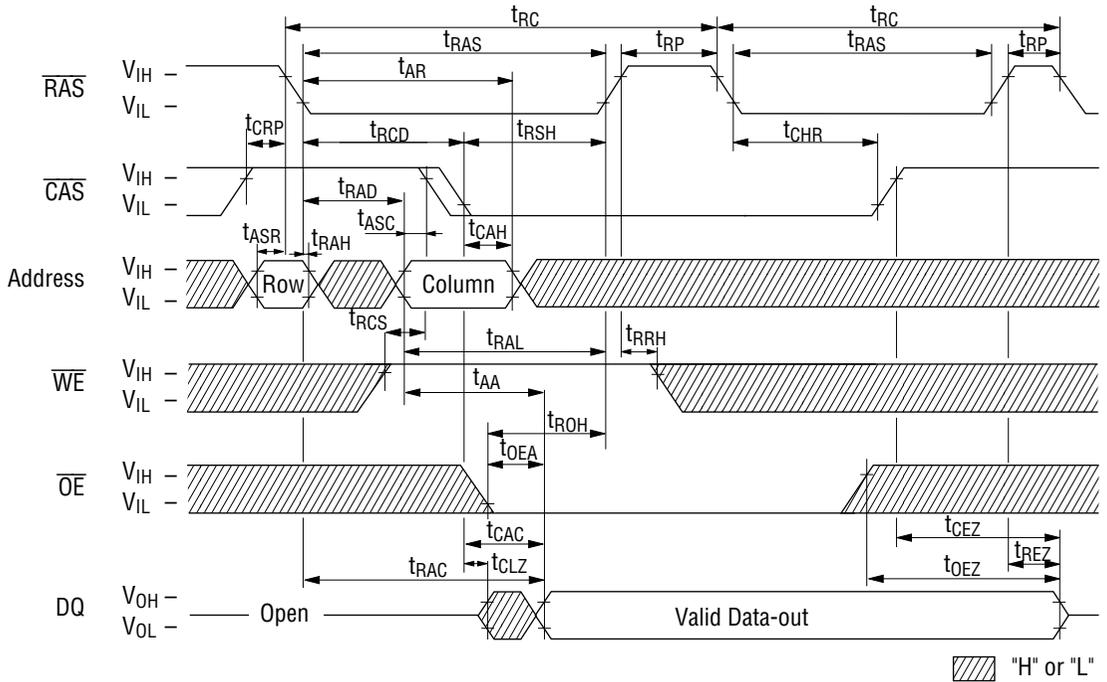
Hidden Refresh Write Cycle

www.DataSheet4U.com

"H" or "L"
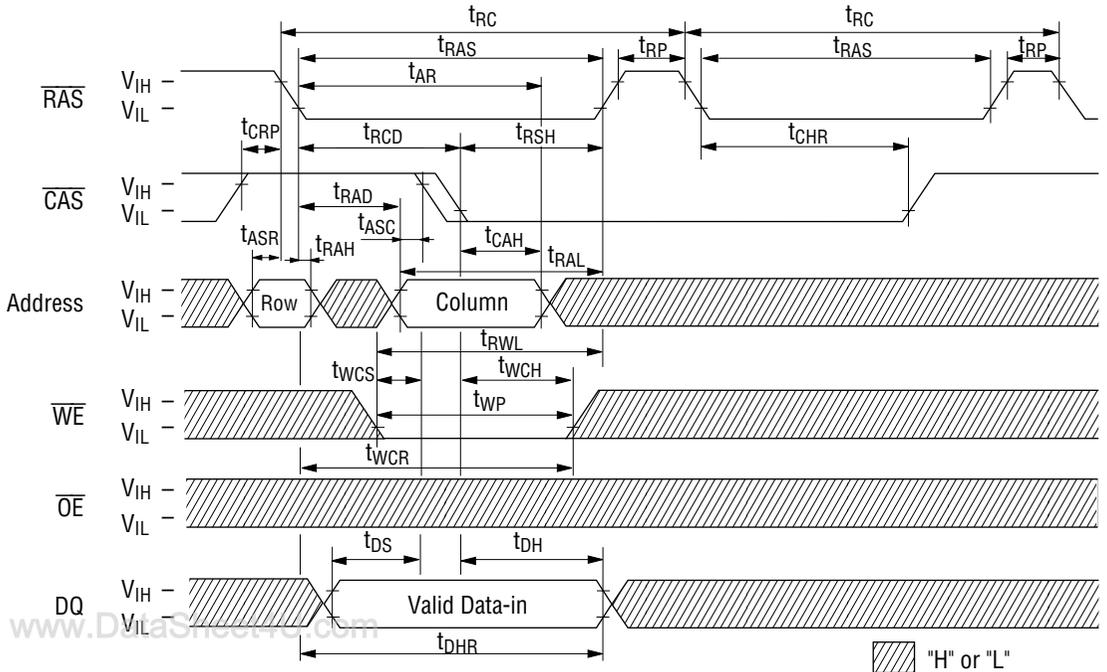
PACKAGE DIMENSIONS

(Unit : mm)
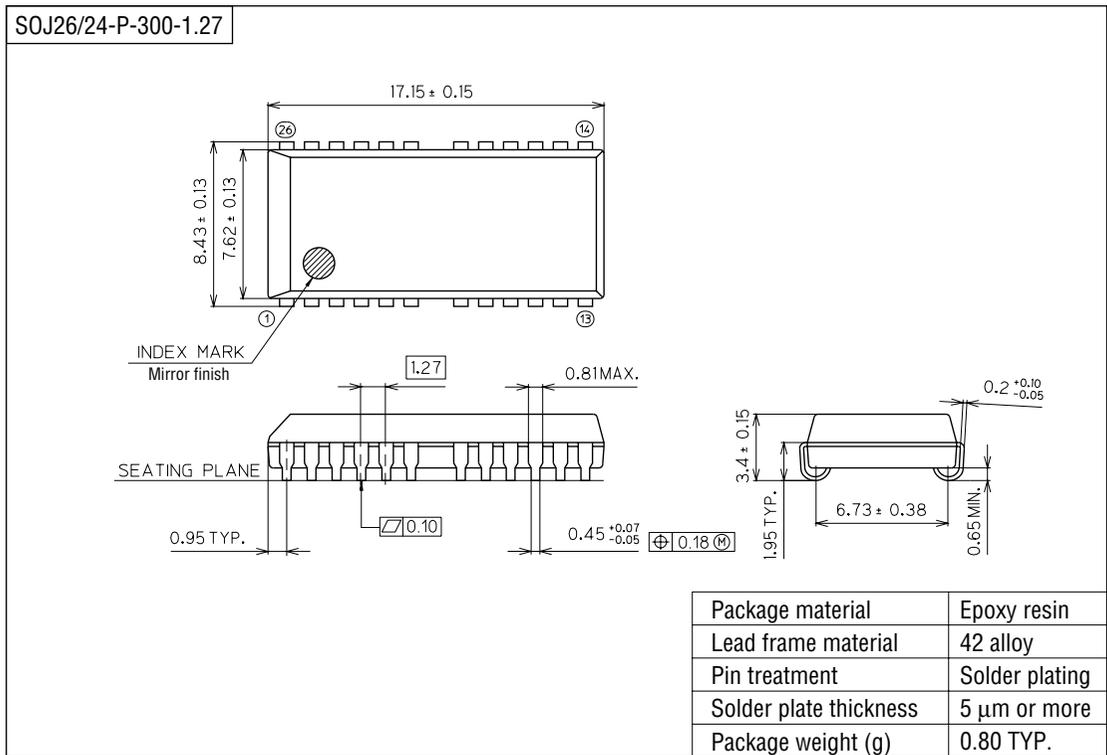
SOJ26/24-P-300-1.27

17.15 ± 0.15

8.43 ± 0.13
7.62 ± 0.13

INDEX MARK
Mirror finish

1.27   0.81MAX.

SEATING PLANE

0.95 TYP.   ⬜ 0.10   0.45 +0.07 −0.05   ⊕ 0.18 Ⓜ

3.4 ± 0.15
1.95 TYP.   6.73 ± 0.38   0.65 MIN.

0.2 +0.10 −0.05

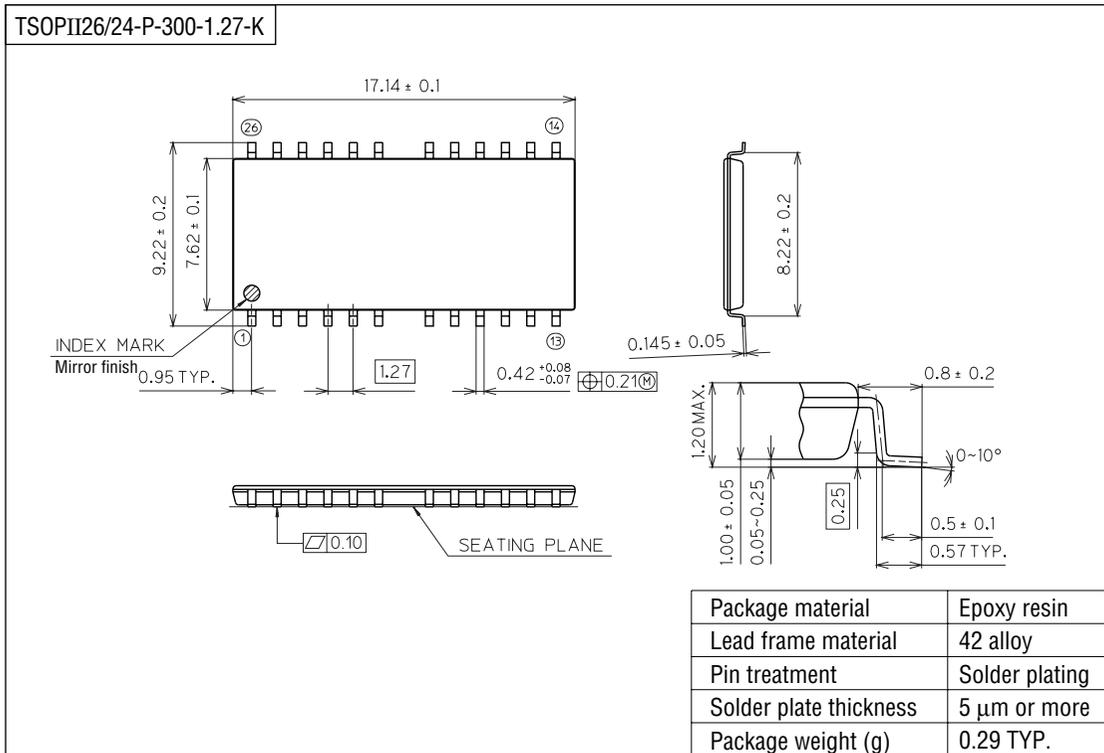| Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.80 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.29 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).