

M6MGB/T321S8TP

33,554,432-BIT (2,097,152 - WORD BY 16-BIT/4,194,304-WORD BY 8-BIT) CMOS
3.0V-ONLY FLASH MEMORY &
8,388,608-BIT (524,288-WORD BY 16-BIT/1,048,576-WORD BY 8-BIT) CMOS SRAM
Stacked - μ MCP (micro Multi Chip Package)

Description

The M6MGB/T321S8TP is a Stacked micro Multi Chip Package (S- μ MCP) that contents 32M-bit Flash memory and 8M-bit Static RAM in a 52-pin TSOP.

32M-bit Flash memory is a 4,194,304 bytes / 2,097,152 words, 3.0V-only, and high performance non-volatile memory fabricated by CMOS technology for the peripheral circuit and DINOR (Divided bit-line NOR) architecture for the memory cell.

8M-bit SRAM is a 1,048,576 bytes / 524,288 words asynchronous SRAM fabricated by silicon-gate CMOS technology.

M6MGB/T321S8TP is suitable for the application of the mobile-communication-system to reduce both the mount space and weight.

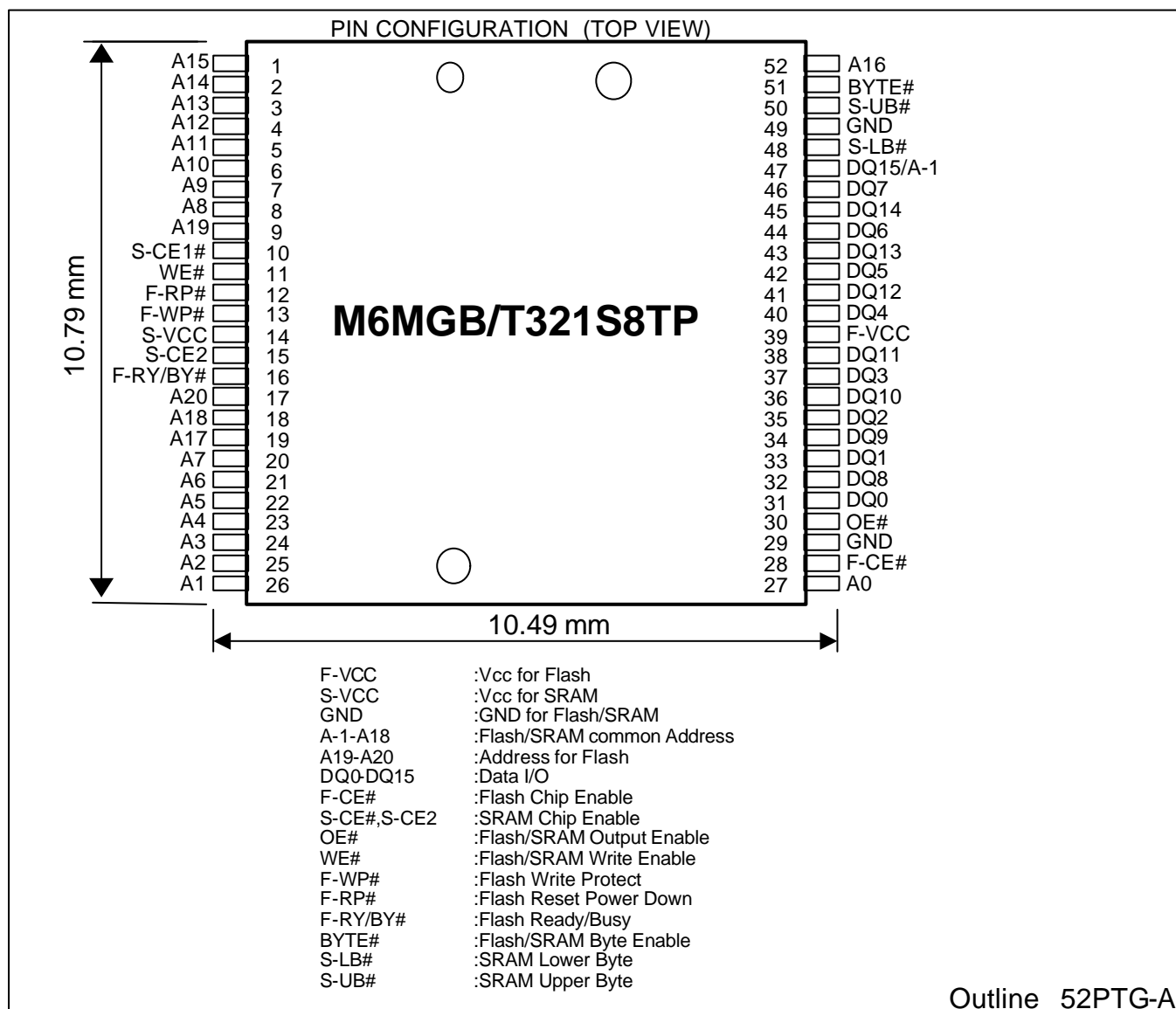
M6MGB/T321S8TP provides for Software Lock Release function. Usually, all memory blocks are locked and can not be programed or erased, when F-WP# is low. Using Software Lock Release function, program or erase operation can be excuted.

Features

Access Time	Flash	85ns (Max.)
	SRAM	85ns (Max.)
Supply Voltage		VCC=2.7 ~ 3.0V
Ambient Temperature		Ta=-20 ~ 85 °C
Package		52pin TSOP(Type-II), Lead pitch 0.4mm

Application

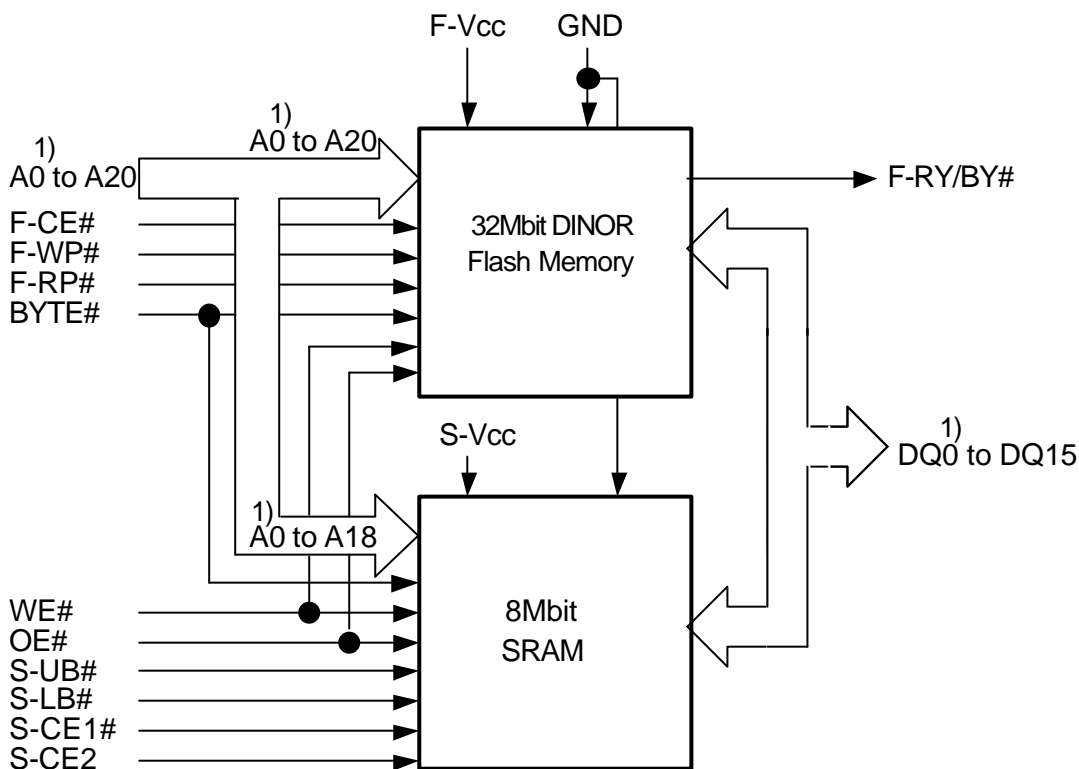
Mobile communication products



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MCP Block Diagram

Note 1): In case of x8 organization, A-1 is added, and only Lower Byte data(DQ0 to DQ7) are assigned to I/O and Upper Byte data(DQ8 to DQ15) are High-Z.

Note 2): In the data sheet there are "VCC"s which mean "F-VCC" or "S-VCC". In the SRAM part there are "UB#" and "LB#" which mean "S-UB#" and "S-LB#", respectively.

Capacitance

Symbol	Parameter		Conditions	Limits			Unit
				Min.	Typ.	Max.	
CIN	Input capacitance	A20-A0, OE#, WE#, F-CE#, F-WP#, F-RP#, S-CE1#, S-CE2, BYTE#, S-LB#, S-UB#	Ta=25°C, f=1MHz, Vin=Vout=0V			18	pF
COUT	Output Capacitance	DQ15-DQ0,F-RY/BY#				22	pF

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