Comlinear Corporation

Low Distortion Wideband Op Amp

CLC207

APPLICATIONS:
- fast, precision A/D conversion
- wide dynamic range IF amps
- test waveform generation
- VCO drivers
- DDS postamps
- radar/communication receivers
- line drivers

FEATURES (typical):
- −80/−85dBc 2nd/3rd harmonics at 20MHz
- −3dB bandwidth of 170 MHz
- 0.1% settling in 22ns
- 2400V/μs slew rate
- overdrive protection
- 3MΩ input resistance
- output may be current limited

3

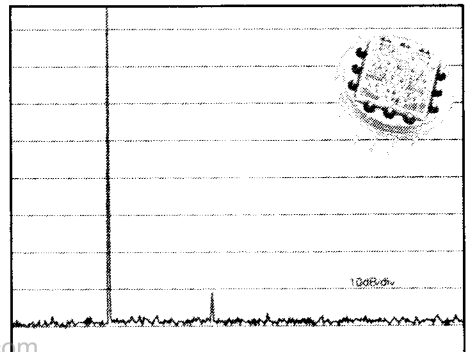
DESCRIPTION:
The CLC207 is a wideband, low distortion operational amplifier designed specifically for applications requiring both high speed and wide dynamic range. Utilizing Comlinear's proprietary current feedback architecture, the CLC207 offers performance far superior to that of conventional voltage feedback op amps.

The most attractive feature of the CLC207 is its extremely low distortion: −80/−85dBc 2nd/3rd harmonics at 20MHz ($2V_{pp}$, $R_L = 200\Omega$). The CLC207 also provides −3dB bandwidth of 170MHz at a gain of +20, settles to 0.1% in 22ns and slews at a rate of 2400V/μs, yet is unity-gain stable without external compensation. The combination of these features positions the CLC207 as the right choice for high speed applications requiring exceptional signal purity.

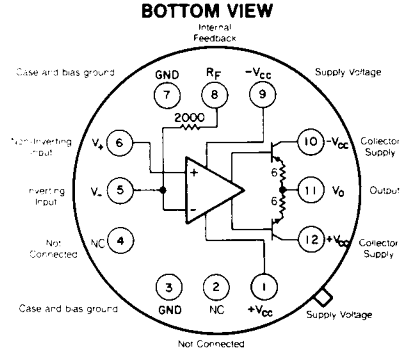
High speed, high resolution A/D and D/A converter systems requiring low distortion operation. will find the CLC207 an excellent choice. Wide dynamic range systems such as radar and communication receivers will find that the CLC207's low harmonic distortion and low noise make it an attractive high speed solution.

The addition of the CLC207 to the 205/206 Series of high speed operational amplifiers broadens the selection of features available from which to choose. The CLC205 offers low power operation, the CLC206 offers higher drive operation, and the CLC207 offers operation with extremely low distortion, all of which are pin compatible and overdrive protected.

The CLC207 is constructed using thin-film resistor/bipolar transistor technology and is available in three versions. The CLC207AI is specified over a temperature range of −25°C to +85°C. The CLC207AK, which features burn-in and tested hermeticity, is specified and tested over a temperature range of −55°C to +125°C. The CLC207A8C is specified and tested over a temperature range of −55°C to +125°C and is screened to MIL-STD-883 for high-reliability applications. All three versions come in 12-pin, TO-8 packages. The DESC SMD number is 5962-90977.

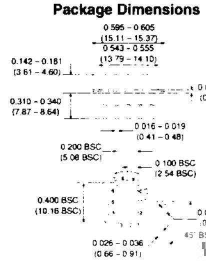


BOTTOM VIEW



Pin 8 provides access to a 2000Ω feedback resistor which can be connected to the output or left open if an external feedback resistor is desired.

Package Dimensions



Typical Performance

parameter	gain setting						units
	+7	+20	+50	−1	−20	−50	
−3dB bandwidth	220	170	80	220	130	80	MHz
rise time	1.7	2.2	4.7	1.7	2.9	4.7	ns
slew rate	2.4	2.4	2.4	2.4	2.4	2.4	V/ns
settling time (to 0.1%)	22	22	20	21	20	19	ns

Electrical Characteristics (A_v = +20; V_{CC} = ±15V; R_L = 200Ω; R_f = 2kΩ)

PARAMETERS	CONDITIONS	TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC207AI	+25°C	−25°C	+25°C	+ 85°C		
Ambient Temperature	CLC207A8/AK	+25°C	−55°C	+25°C	+125°C		
FREQUENCY DOMAIN RESPONSE							
* −3dB bandwidth	V_{out}<2V_{pp}	170	>140	>140	>125	MHz	SSBW
	V_{out}<10V_{pp}	100	>72	>80	>80	MHz	LSBW
gain flatness	V_{out}<2V_{pp}						
* peaking	0.1 to 35MHz	0	<0.3	<0.3	<0.5	dB	GFPL
* peaking	>35MHz	0	<0.5	<0.5	<0.8	dB	GFPH
* rolloff	at 70MHz	—	<0.8	<0.8	<0.8	dB	GFR
group delay	to 70MHz	3.0±.2	—	—	—	ns	GD
linear phase deviation	to 50MHz	0.8	<3.0	<2.0	<3.0	°	LPD
TIME DOMAIN RESPONSE							
rise and fall time	2V step	2.2	<2.6	<2.6	<3.0	ns	TRS
	10V step	4.8	<5.5	<5.5	<5.5	ns	TRL
settling time to 0.1%	10V step, note 2	22	<27	<27	<27	ns	TS
to 0.05%	10V step, note 2	24	<30	<30	<30	ns	TSP
overshoot	5V step	7	<14	<14	<14	%	OS
slew rate	20V_{pp} @ 50MHz	2400	>1800	>2000	>2000	V/µs	SR
DISTORTION AND NOISE RESPONSE, note 3							
*2nd harmonic distortion	2V_{pp}, 20MHz, R_L = 200Ω*	−80	<−68	<−76	<−76	dBc	HD2
	R_L = 100Ω	−69	<−64	<−64	<−64	dBc	HD2
*3rd harmonic distortion	2V_{pp}, 20MHz, R_L = 200Ω*	−85	<−76	<−76	<−76	dBc	HD3
	R_L = 100Ω	−69	<−64	<−64	<−64	dBc	HD3
equivalent noise input							
voltage	>100kHz	1.6	<1.8	<1.8	<1.8	nV/√Hz	VN
inverting current	>100kHz	20	<23	<23	<23	pA/√Hz	ICN
non-inverting current	>100kHz	2.2	<2.5	<2.5	<2.5	pA/√Hz	NCN
noise floor	>100kHz	−158	<−157	<−157	<−157	dBm_{1Hz}	SNF
integrated noise	1kHz to 150MHz	33	<38	<38	<38	µV	INV
integrated noise	5MHz to 150MHz	33	<38	<38	<38	µV	INV
STATIC DC PERFORMANCE							
*input offset voltage		3.5	<8.0	<8.0	<11.0	mV	VIO
average temperature coefficient		11	<25	<25	<25	µV/°C	DVIO
*input bias current	non-inverting	3.0	<25	<15	<15	µA	IBN
average temperature coefficient		15	<100	<100	<100	nA/°C	DIBN
*input bias current	inverting	2.0	<22	<10	<25	µA	IBI
average temperature coefficient		20	<150	<150	<150	nA/°C	DIBI
*power supply rejection ratio		69	>55	>55	>55	dB	PSRR
common mode rejection ratio		60	>50	>50	>50	dB	CMRR
*supply current	no load	25	<27	<27	<29	mA	ICC
MISCELLANEOUS PERFORMANCE							
non-inverting input resistance	DC	3.0	>1.0	>1.0	>1.0	MΩ	RIN
non-inverting input capacitance	70MHz	5.0	<7.0	<7.0	<7.0	pF	CIN
output impedance	DC	—	<0.1	<0.1	<0.1	Ω	RO
output voltage range	no load	±12	>±11	>±11	>±11	V	VO
internal feedback resistor		2.0	—	—	—	kΩ	RF
absolute tolerance		—	—	<0.2	—	%	RFA
temperature coefficient		—	—	−100±40	—	ppm/°C	RFTC
inverting input current self limit		2.2	<3.0	<3.0	<3.2	mA	ICL

V_{CC}		±20V
I_{out}		±150mA
V_{CM}, V_{out}	|V_{CC}|>15V	±(29−|V_{CC}|)V
	|V_{CC}|≤15V	±(|V_{CC}|−1)V
differential input voltage		±3V
junction temperature		+175°C
operating temperature range		
	AI:	−25°C to + 85°C
	A8/AK:	− 55°C to +125°C
storage temperature		−65°C to +150°C
lead temperature (soldering 10s)		+300°C

V_{CC}	±5V to ±15V
I_{out}	±100ma
V_{CM}	±(|V_{CC}|−5)V
gain range	+7 to +50, −1 to −50

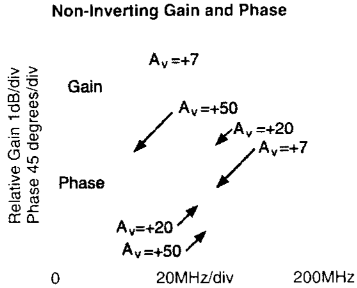
Notes:

note 1: Parameters preceded by an * are 100% tested. A8 and AK units are tested at −55°C, +25°C and +125°C. AI units are tested at +25°C, though performance at −25°C and +85°C is guaranteed as shown above.

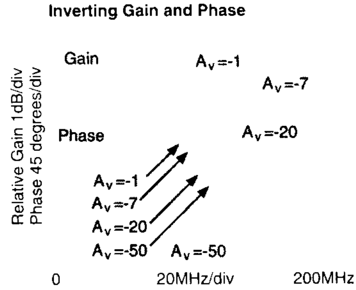
note 2: Settling time specifications require the use of an external feedback resistor (2kΩ).

note 3: In AI units, the noise specifications are guaranteed (but not tested) as shown above. A8 and AK units tested with R_L = 200Ω.

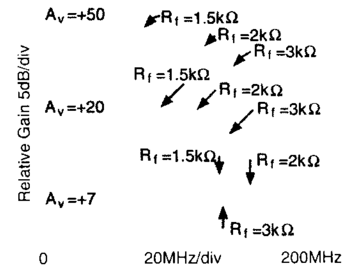
Non-Inverting Gain and Phase



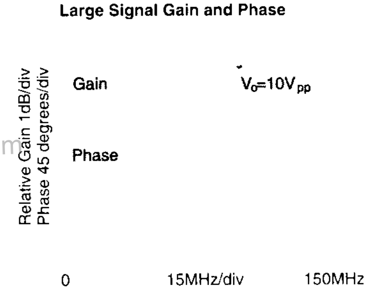
Inverting Gain and Phase



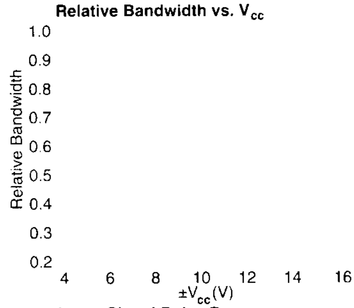
Response vs. External R_f



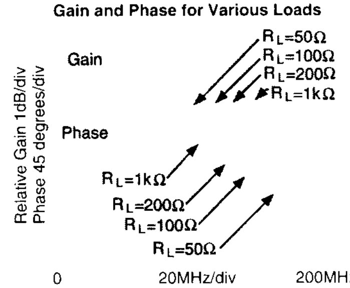
Large Signal Gain and Phase



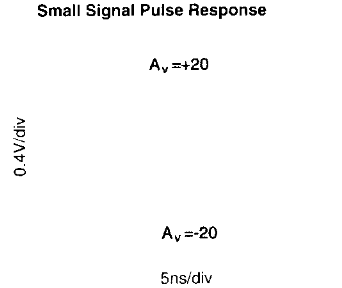
Relative Bandwidth vs. V_{cc}



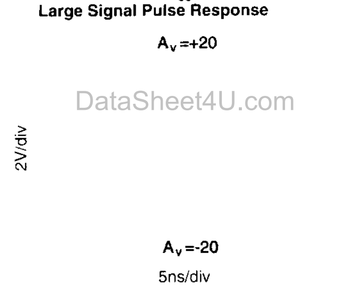
Gain and Phase for Various Loads



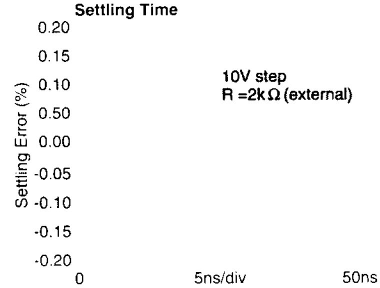
Small Signal Pulse Response



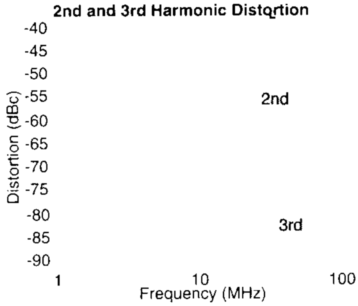
Large Signal Pulse Response



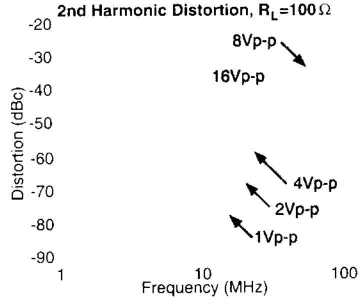
Settling Time



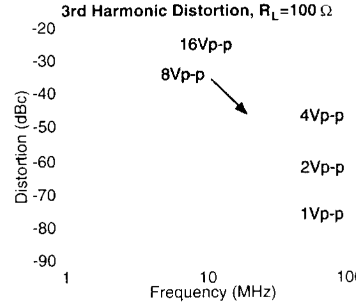
2nd and 3rd Harmonic Distortion



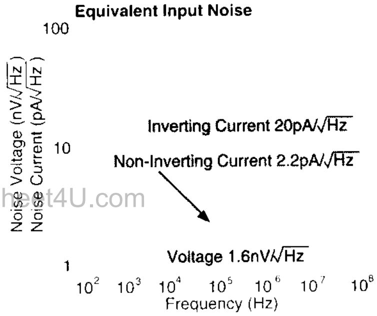
2nd Harmonic Distortion, R_L=100Ω



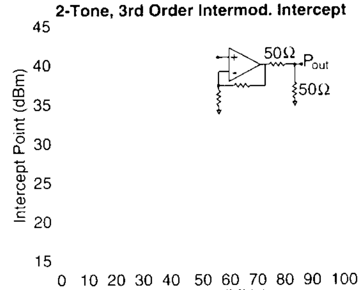
3rd Harmonic Distortion, R_L=100Ω



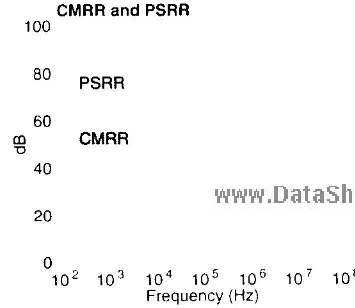
Equivalent Input Noise



2-Tone, 3rd Order Intermod. Intercept



CMRR and PSRR



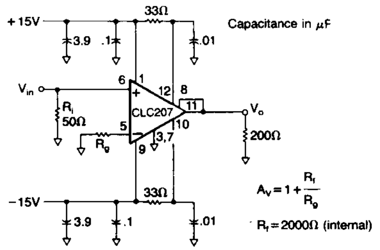


Figure 1: recommended non-inverting gain circuit

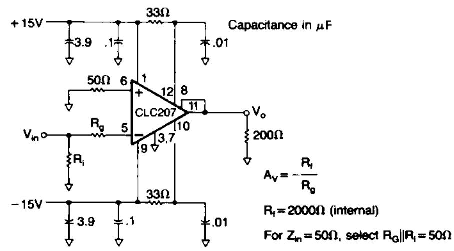


Figure 2: recommended inverting gain circuit

Test fixture schematics are available upon request.

Overdrive Protection

Unlike most other high-speed op amps, the CLC207 is not damaged by saturation caused by overdriving input signals (where $V_{in} \times gain > max.V_{out}$). The CLC207 self limits the current at the inverting input when the output is saturated (see the inverting input current self limit specification); this ensures that the amplifier will not be damaged due to excessive internal currents during overdrive. For protection against input signals which would exceed either the maximum differential or common mode input voltage, the diode clamp circuits below may be used.

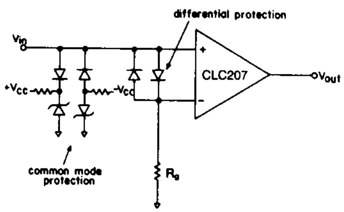


Figure 3: diode clamp circuits for common mode and differential mode protection

Short Circuit Protection

Damage caused by short circuits at the output may be prevented by limiting the output current to safe levels. The most simple current limit circuit calls for placing resistors between the output stage collector supplies and the output stage collectors (pins 12 and 10). The value of this resistor is determined by:

$$R_c = V_c / I_l - R_l$$

Where I_l is the desired limit current and R_l is the minimum expected load resistance (0Ω for a short to ground). Bypass capacitors of 0.01μF on should be used on the collectors as in Figures 1 and 2.

A more sophisticated current limit circuit which provides a limit current independent of R_l is shown below.

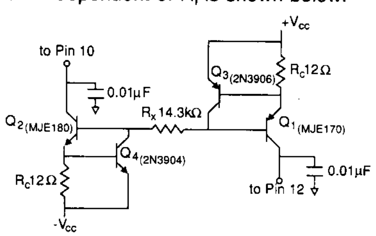


Figure 4: active current limit circuit (50mA)

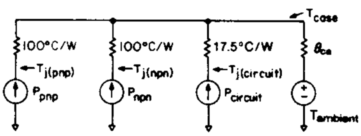
With the component values indicated, current limiting occurs at 50mA. For other values of current limit (I_l), select R_c to equal V_{be}/I_l. Where V_{be} is the base to emitter voltage drop of Q3 (or Q4) at a current of $[2V_{cc}-1.4]/R_x$, where $R_x \leq [(2V_{cc}-1.4)/I_l]\ B_{min}$. Also, B_{min} is the minimum beta of Q1 (or Q2) at a current of I_l. Since the limit current depends on V_{be}, which is temperature dependent, the limit current is likewise temperature dependent. If a temperature-independent current limit circuit is needed, contact Comlinear.

Controlling Bandwidth and Passband Response

In most applications, a feedback resistor value of 2kΩ will provide optimum performance; nonetheless, some applications may require a resistor of some other value. The response versus R_f plot on the previous page shows how decreasing R_f will increase bandwidth (and frequency response peaking, which may lead to instability). Conversely, large values of feedback resistance tend to roll off the response.

The best settling time performance requires the use of an external feedback resistor. (Use of the internal resistor results in 0.1% to 0.2% settling tail.) The settling performance may be improved slightly by adding a capacitance of 0.4pF in parallel with the feedback resistor. (Settling time specifications reflect performance with an external feedback resistor but with no external capacitance.)

Thermal Model



$P_{circuit} = [(+V_{cc}) - (-V_{cc})]^2 / 1.77k\Omega$

$P_{xxx} = [(\pm V_{cc}) - V_{out} - (I_{col})(R_{col}+6)]\ (I_{col})$ (% duty cycle)

(For positive V_o and V_{cc}, this is the power in the npn output stage.)
(For negative V_o and V_{cc}, this is the power in the pnp output stage.)

θ_{ca} = 65°C/W in still air without a heatsink
35°C/W in still air with a Thermalloy 2268B
15°C/W in 300ft/min air with a Thermalloy 2268B
(Thermalloy 2240 works equally well.)

$I_{col} = V_{out}/R_{load}$ or 3mA, whichever is greater. (Include feedback R in R_{load}.)

R_{col} is a resistor (33Ω recommended) between the xxx collector and $\pm V_{cc}$.

$T_{j\,(pnp)} = P_{pnp}(200 + \theta_{ca}) + (P_{cir} + P_{npn})\ \theta_{ca} + T_a$,
similar for $T_{j\,(npn)}$.

$T_{j\,(cir)} = P_{cir}(17.5 + \theta_{ca}) + (P_{pnp} + P_{npn})\ \theta_{ca} + T_a$.

Printed Circuit Layout

As with any high frequency device, a good PCB layout will enhance the performance of the CLC207. Good ground plane construction and power supply bypassing close to the package are critical to achieving full performance. In the non-inverting configuration, the amplifier is sensitive to stray capacitance to ground at the inverting input. Hence, the inverting node connections should be small with minimal stray capacitance to the ground plane or other nodes. Shunt capacitance across the feedback resistor should not be used to compensate for this effect.

Evaluation PC boards (part number 730008 for inverting, 730009 for non-inverting) for the CLC207 are available from Comlinear at minimal cost.